NXP Semiconductors
Application Note

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External Regulation Mode and Associated Low Power Handshakes and Considerations

by: NXP Semiconductors

Contents

1 Introduction

SAC57D5xx family is a multi-core architecture powered by ARM Cortex-M4® (for real time), Cortex-A5® (for application and HMI) and a powerful Cortex-M0+® (I/O) processors coupled with 2-D Graphics Accelerators, Heads-Up Display (HUD) Warping Engine, Dual TFT display drive and integrated Stepper Motor Controller (SMC).

2 Core supply management

The SAC57D5xx microcontroller's Power Management Controller (PMC) generates, monitors and controls the power supply and related resets in the device. If any 'essential' supply falls outside of its operating range, the voltage monitors take the device into a 'safe power on reset state'. Refer to device Reference Manual and Datasheet for further details.

The device provides modes to control the device performance and power consumption in the application lifetime. Power domains are logical divisions within the microcontroller that can be power gated to put the microcontroller in a reduced-power configuration. SAC57D5x has two power domains – High (PD2) and Low (PD0). All the high-performance blocks are enabled in PD2 domain, whereas PD0 domain retains the bare minimum to maintain device configuration as well as keep basic autonomous functionality with very low power. Application can also configure the microcontroller to work in any of the User operating modes, DRUN, RUNx, STOP or STANDBY mode. Per default, both power modes (PD0 and PD2) are powered in all modes other than STANDBY. Only PD0 mode is powered in STANDBY mode.

STANDBY mode is thus the one that offers maximum power saving. Since none of the three cores are active in STANDBY mode, the core supply VDD12 is recommended to be switched OFF in this mode to gain maximum power saving. For the core supply (VDD12), the device only supports external regulation. Further details on regulation are explained in the section below.

2.1 Core supply during power up/power down

The PORST pin must be controlled by the hardware. This can be accomplished by driving PORST pin such that when external VDD12 is not stable or outside operating range as defined in the datasheet, PORST is driven LOW externally, and once VDD12 is stable and within operating range, PORST is driven HIGH. PORST must be driven high during the course of RUN mode.

Alternatively, another option is to connect PORST pin to VDDE_A supply. In this case, multiple voltage monitor resets may be seen during power-up / power-down in presence of a non-monotonic or slow ramp VDD12 supply. Absence of PORST

handshake may result in multiple interrupts being seen when exiting from STANDBY mode. This may also result in device getting stuck in reset in certain mode transition cases from STANDBY to DRUN.

2.2 Core supply in STANDBY mode

Once STANDBY mode is entered, it can only be left via a system wakeup. Since the cores are not working in STANDBY mode, the VDD12 core supply can be disabled using external regulator control (PE9, PE14 or PM7) pin. External regulator control functionality on PE9, PE14 or PM7 pin can be enabled by configuring UTEST_MISC [EXTn_REG_SUPPLY]. Polarity of these pins can be further controlled by appropriately configuring UTEST_MISC [EXT_REG_POL]. The timing diagram below describes the required configuration.

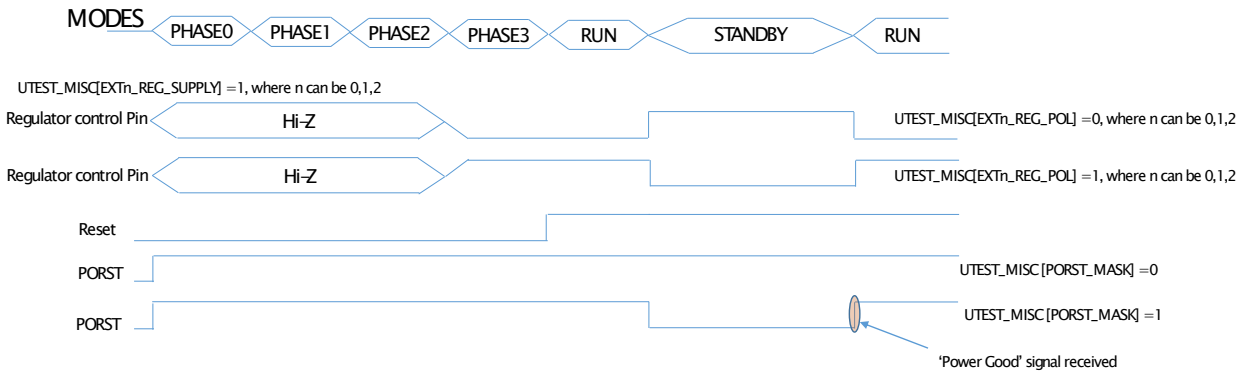

Figure 1. External regulator configurations

VDD12 supply is generated externally and can be gated/disabled when in STANDBY mode. External regulator control pins can be configured in UTEST_MISC DCF using EXTn_REG_SUPPLY field (for more details on DCF refer to 'UTEST_register_Bits' tab of the DCF sheet attached with device Reference Manual) to enable/disable the supply to the cores. The external regulator control pins can also be used to directly enable/disable the regulator if the external regulator supports such control (usually by means of enable pin). Figure 2. Example hardware block for external regulator control on page 2 shows one of the block level implementation of hardware. The hardware must be designed in such a way that electrical specs stated in the device are followed.

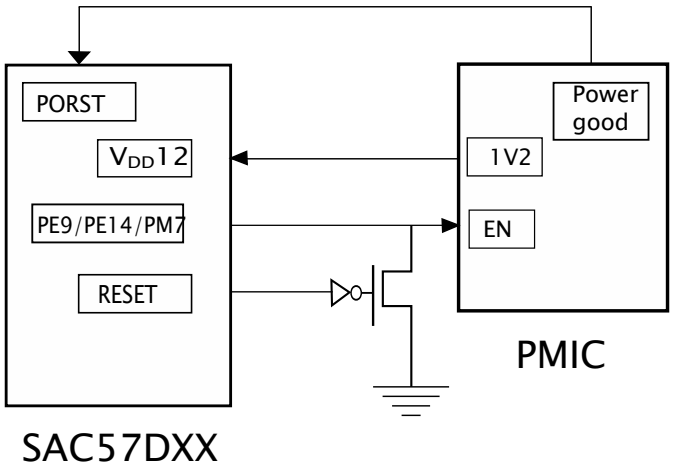

Figure 2. Example hardware block for external regulator control

2.2.1 PORST handshake between MCU and external regulator

During STANDBY mode, if UTEST_MISC [PORST_MASK] is set to 0 then PORST must be kept high even if VDD12 is supplied externally or not. Pulling PORST pin low in STANDBY mode will result in chip getting into RESET.

In case UTEST_MISC [PORST_MASK] is set to 1 then PORST pin can be used as a handshake signal between MCU and external regulator to indicate presence/absence of externally supplied VDD12. PORST must be driven low after external regulator control pins indicate STANDBY mode has been entered and as soon as the external regulator is disabled. The device will not exit STANDBY mode as long as the PORST pin is kept low.

3 Conclusion

PORST signal is recommended to be used for handshake between the Core supply regulator and the MCU in addition to all the recommended hardware design guidelines. For more information refer to AN5265.

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