



# LPC800: 32-Bit Arm® Cortex®-M0+-Based Low-Cost MCU

## LPC80X

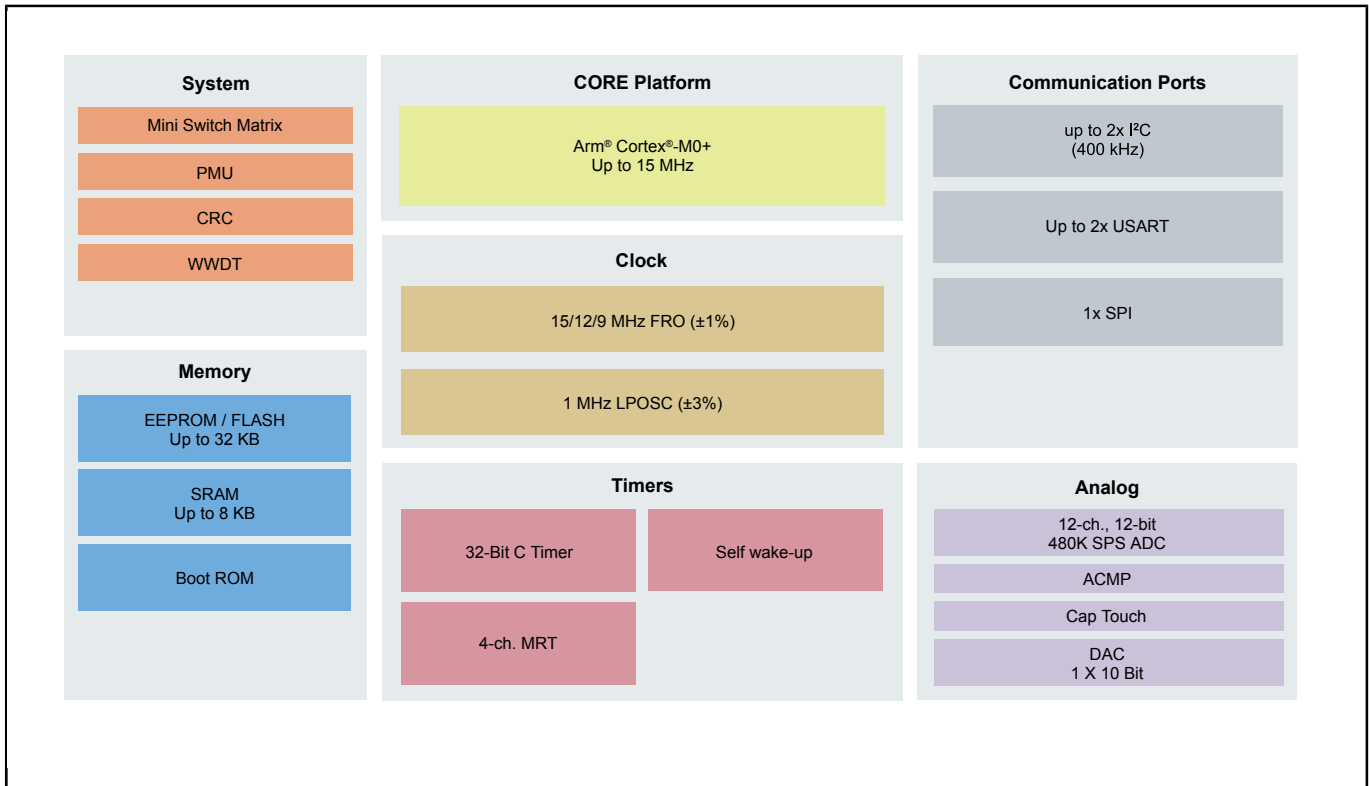
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LPC80x is a cost-effective Arm Cortex-M0+ based 32-bit MCU family operating at CPU frequencies of up to 15 MHz. The LPC80x MCU family supports up to 32 KB of flash memory and up to 4 KB of SRAM.

This family features a power-optimized core, small footprint in popular packages, and level shifting options thanks to its separate power rails. The peripheral complement of the LPC80x includes a CRC engine, I<sup>2</sup>C-bus interfaces, up to two USARTs, one SPI interface, capacitive touch interface (cap touch), one multi-rate timer, self-wake-up timer, one general purpose 32-bit counter/timer, one 12-bit ADC, one 10-bit DAC, one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, programmable logic unit (PLU), and up to 30 general-purpose I/O pins.

This device is fully supported by NXP's [MCUXpresso Software and Tools](#), a comprehensive and cohesive set of free software development tools for Kinetis, LPC and i.MX RT microcontrollers. MCUXpresso SDK also includes project files for Keil MDK and IAR EWARM.

# LPC80x MCU Block Diagram



View additional information for [LPC800: 32-Bit Arm® Cortex®-M0+-Based Low-Cost MCU](#).

**Note:** The information on this document is subject to change without notice.

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