AN10974

LPC176x/175x 12-bit ADC design guidelines

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Document information

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Abstract	PCB Layout Reference Design and Software for testing the LPC1768 12-bit ADC.

Revision history

Rev	Date	Description
1	20100901	Initial version.

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1. Introduction

The LPC175x/6x family is based on the ARM Cortex M3 core, and includes a 12-bit Analog-to-Digital (ADC) module with input multiplexing among eight pins, conversion rates up to 200 kHz, and multiple result registers. The 12-bit ADC can also be used with the GPDMA controller.

Designing a system with a 12-bit ADC requires more attention than the lower resolution ADC systems traditionally used in the NXP LPC family of products.

As a comparison, using a voltage reference of 3.3 V in a 10-bit ADC system, every converted value differs from the consecutive by 3.2 mV (3.3 V/1024). In the case of a 12-bit ADC, the LSB value goes down to 0.8 mV. So comparing 3.2 mV against 0.8 mV, it is apparent that noise reduction techniques will have a fundamental role in the system design, at both schematic and board layout level.

This application note provides general design guidelines that can be applied to the board layout design, as well as a reference design and a software project the user can utilize in order to test the LPC1700 12-bit ADC. Some test scenarios are also included, demonstrating the factors that can affect the conversion results.

2. Board reference design

A complete board reference design is provided with this Application Note. Customers can use this design as is, or as a starting point for their own designs.

Eagle Layout Editor Version 5.4.0 was used in this design, and the full project, including schematics, layout design and BOM, is attached with this document.

The main purpose of the board is for ADC testing; all ADC channels are available for test. Two BNC connectors, used to input external signal (or a fixed voltage from an external power supply) and two potentiometers, providing an adjustable voltage, can be connected to the analog input lines through a series of jumpers which select the input for each analog channel.

Different power supply schemes can be used with this board. Analog and Digital power domains can be supplied from a common source, as is the case when using the USB connector powered from a PC, or an external power supply providing the required 3.3 V externally. Another option is to provide separate power for each domain (Analog and Digital), and even the VREF (Voltage reference for the ADC) can be supplied from a separate power supply. A series of jumpers allow the user to select the desired configuration.

A JTAG/SWD debug port is available for both Debug and Flash programming. ISP can also be used for Flash programming though COM0 connector (selecting UART0 with the appropriate jumpers). UART1 can also be selected through jumpers. Two buttons for Reset and ISP are provided. A general purpose LED is available. All GPIO pins are available on the board.

The Design Guidelines provided in the Appendix section were adhered to in this layout design. In order to keep the costs low, a 2-layer design was chosen. The bottom layer is used as ground planes. Both analog and digital ground planes are used, and a couple of jumpers allow different configurations; both grounds tied together at just one point, or connected together through a choke, or totally separated. These different setup options allow the user to experiment with different scenarios and compare results.

The top layer is used mainly for power and signal traces. Digital signals (especially those with high-frequency or high-current components) are kept over the digital ground plane, and far from the analog portion. The analog-related components (BNC connectors, analog potentiometers, jumpers and connectors for analog voltages) were placed at the left side of the board, forming an “analog island”. The digital-related components were placed over the rest of the board. Fig 1 shows the final layout. As seen in the figure, all jumper settings are labeled on the board silkscreen.

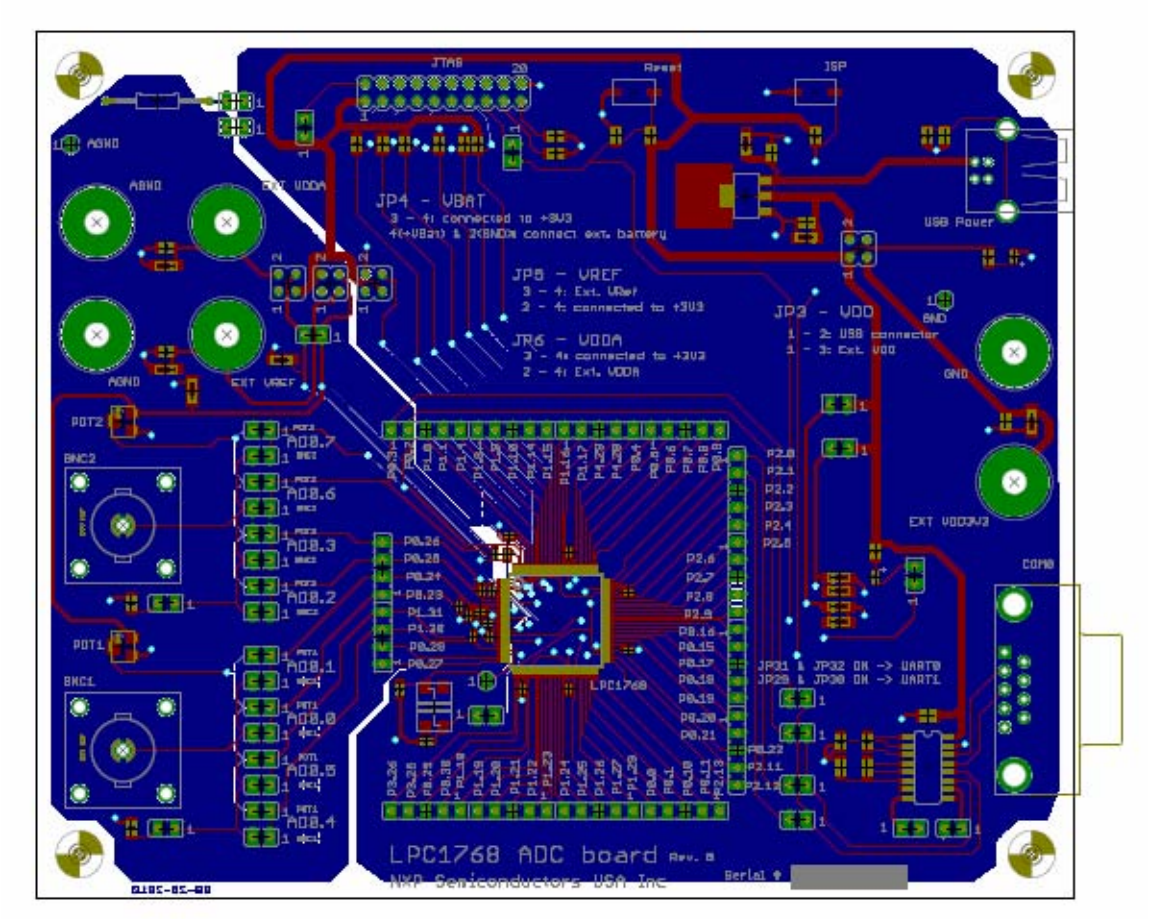


Fig 1. LPC1768 ADC board layout

3. Testing software

In order to test the board, software is provided. Keil MDK version 4.03 was used for this project (the free evaluation version can be used).

With the Test software, the user can select the ADC Channel to test, as well as the number of samples to run. Other parameters, like the ADC clock, can also be set.

Ideally, when supplying a fixed voltage to the selected channel input, all samples should return the same value. In practice, this rarely occurs as noise or power supply variations may skew the converted value from the expected one. As a result, a range of similar values are converted instead of only one. The range becomes narrower as the noise level is reduced and the power supply quality is improved.

As the software uses an array to keep the different conversion results, the dimension for this array should be defined. In the software the parameter named “Maximum variation expected” provides an initial value for this array, and its default value of 20 is adequate for most cases. Two additional variables keep track of out-of-range values (for the Lower and Higher limits), so the user knows this parameter should be adjusted.

Another parameter defines Print options. All these parameters are found in the *config.h* file, and can be edited using the Keil Configuration Wizard, as shown in Fig 2.

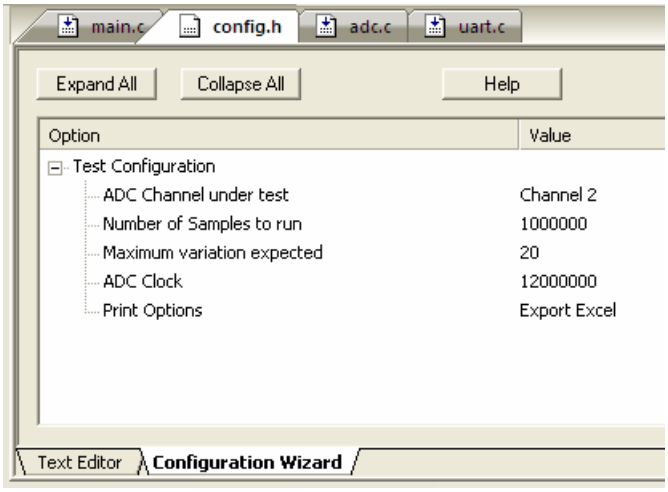


Fig 2. Software configuration parameters

Once the board is programmed with the executable, the HyperTerminal program can be used in order to view the program’s messages. To use HyperTerminal, connect a serial cable between the ADC board (COM0) and the PC serial port, and start HyperTerminal using 9600,8,N,1,N parameters. After initialization, the program will start with the ADC sampling and once finished, the results will be shown in the terminal program’s screen. If the “Export Excel” option was selected in the configuration wizard, then the sampled values and their number of occurrences will be shown in the screen. See Fig 3.

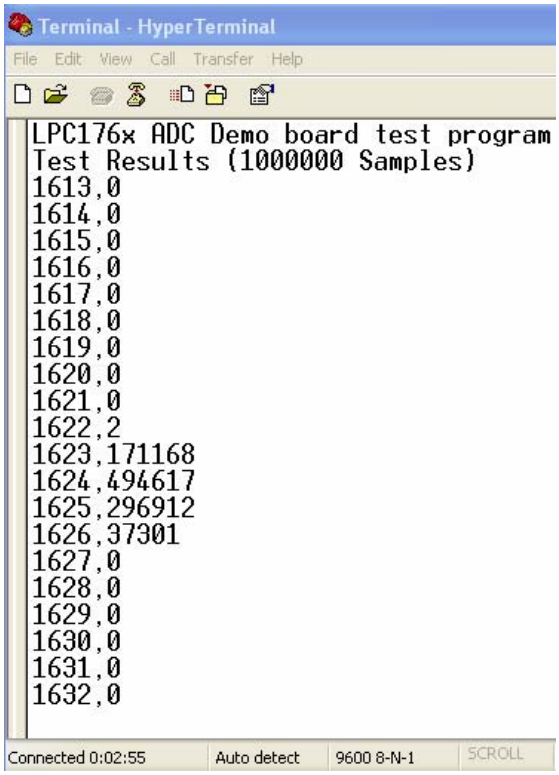
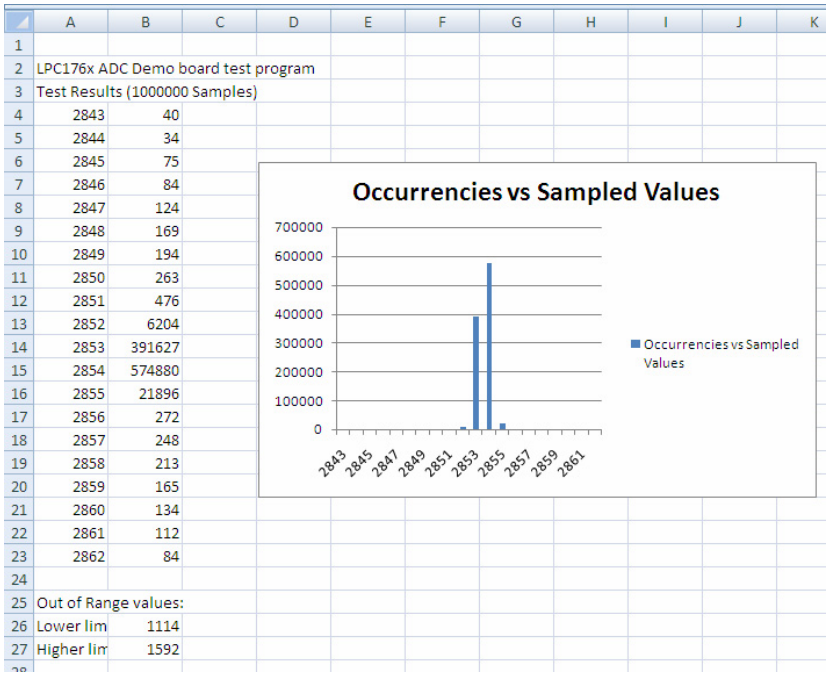


Fig 3. HyperTerminal showing results as exported values

After capturing this information and saving it as a file with “csv” extension, the file can be opened using Microsoft Excel and the values exported will be presented in two columns. From this point, it’s very easy to create a Column Chart representing the number of occurrences for each sampled value. See Fig 4.



	A	B	C	D	E	F	G	H	I	J	K
1											
2	LPC176x ADC Demo board test program										
3	Test Results (1000000 Samples)										
4	2843	40									
5	2844	34									
6	2845	75									
7	2846	84									
8	2847	124									
9	2848	169									
10	2849	194									
11	2850	263									
12	2851	476									
13	2852	6204									
14	2853	391627									
15	2854	574880									
16	2855	21896									
17	2856	272									
18	2857	248									
19	2858	213									
20	2859	165									
21	2860	134									
22	2861	112									
23	2862	84									
24											
25	Out of Range values:										
26	Lower lim	1114									
27	Higher lim	1592									

Fig 4. Test results exported to Excel

The other Print option available in the program configuration is “Plot Values”, which displays a graph with the results directly in the HyperTerminal screen, allowing the user to quickly evaluate the test results without the need of additional steps to export the values in other programs. See Fig 5.

Note: Be aware that using JTAG for debug could affect results, as stated in Section 4.2.

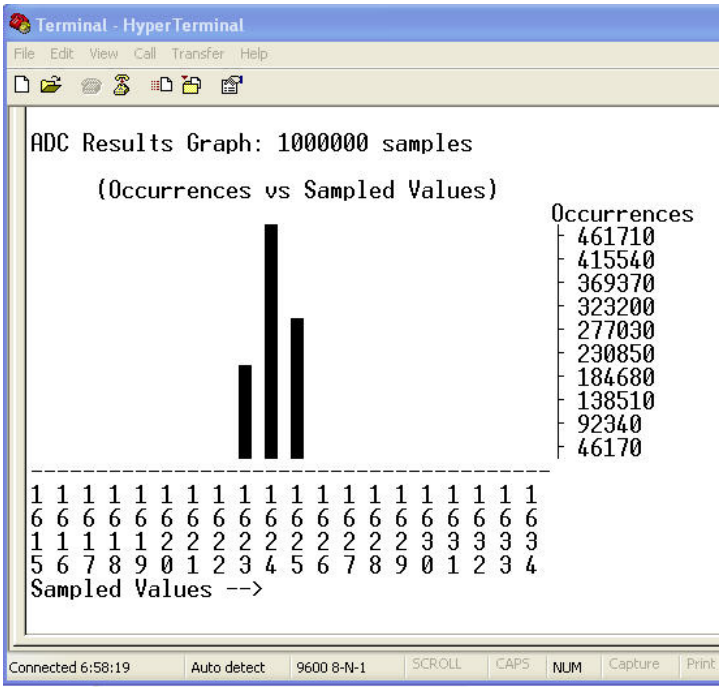


Fig 5. HyperTerminal showing results as a column's graph

4. Running tests

In this section, different tests scenarios are provided and their corresponding results shown.

4.1 Keil MCB1700 and LPC1768 ADC Demo boards comparison

Benchmark tests were carried out on a MCB1700 Keil board and a LPC1768 ADC demo board, and the results are compared. Fig 6 shows the tests results.

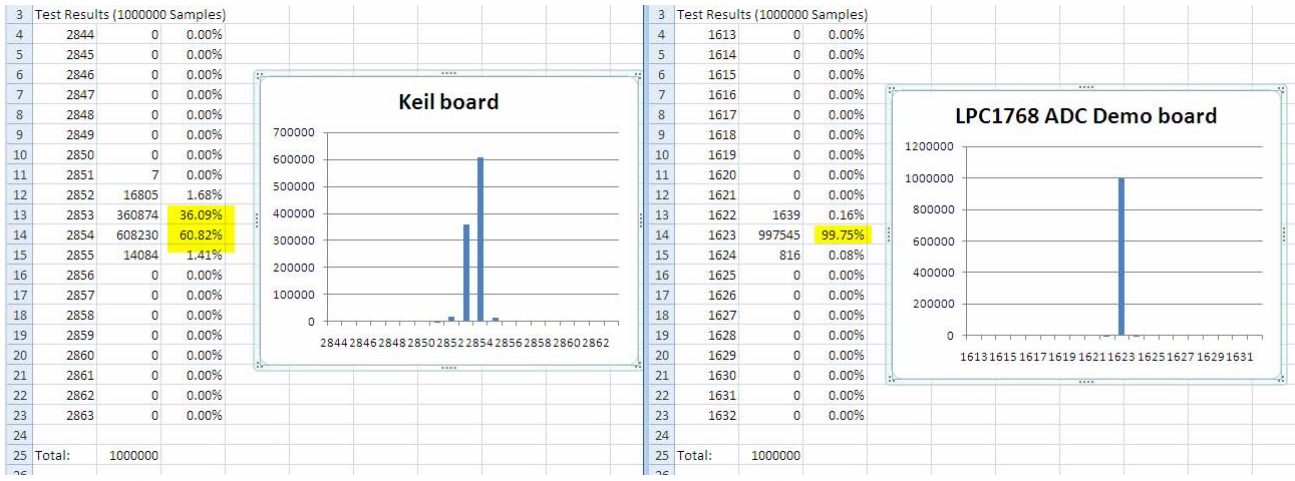


Fig 6. Test results showing better performance for the LPC1768 ADC demo board

As seen in the above figure, the LPC1768 ADC Demo board converts 99.75% of the samples to the same value, meaning the noise is minimal, and thus, the ADC performance is higher compared to the Keil board. This demonstrates better results for the LPC1768 ADC Demo board layout design.

4.2 The effect of JTAG during a Debug session

The user should be warned that on some occasions, the JTAG used for a Debug session could negatively affect the test results and, in some cases, introduce additional noise causing the appearance of “glitches” (values far away from the expected range, including peak values such 0x000 and 0xfff). Fig 7 shows the effect of the JTAG used in a Debug session.

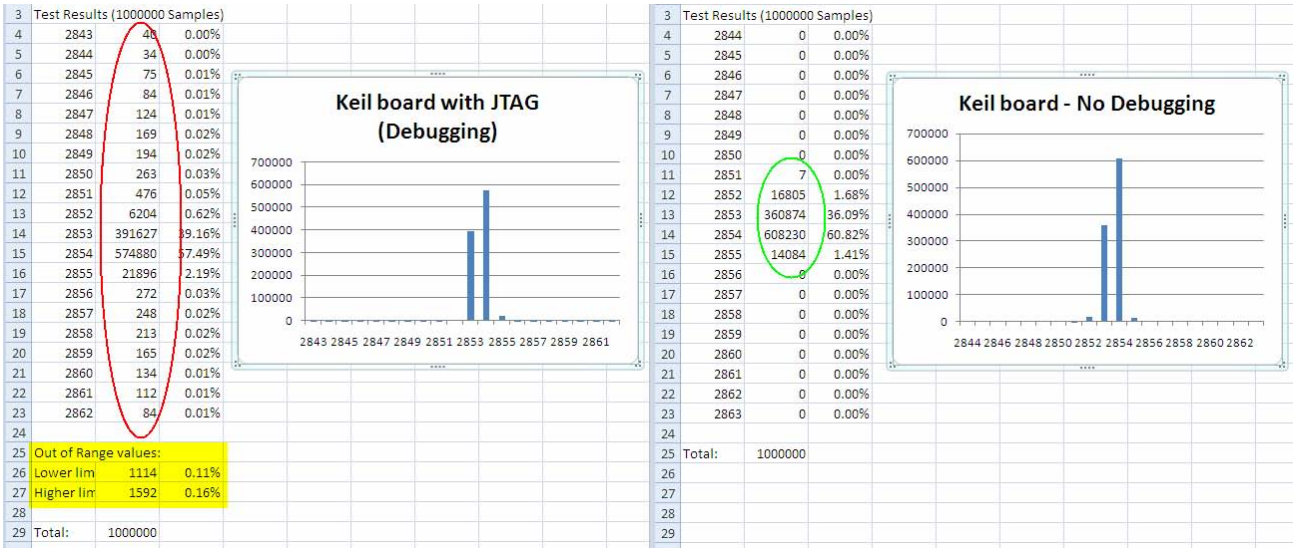


Fig 7. The effect of JTAG in a debug session

As illustrated in Fig 7, the JTAG device can introduce additional noise causing sampled values to spread over a wider range.

4.3 The effect of the ground planes

The board layout provides two different ground planes; one for the Analog domain and one for the Digital domain. In most cases, it’s necessary to have only one system-wide ground as a reference, so at some point, both ground planes should be related in some way.

A direct connection between both grounds can cause the Digital plane to introduce additional noise to the Analog domain. Using an inductor or a choke to interconnect both grounds allows a system-wide reference while the Digital noise is minimized due the inductor filter effect. See Fig 8.

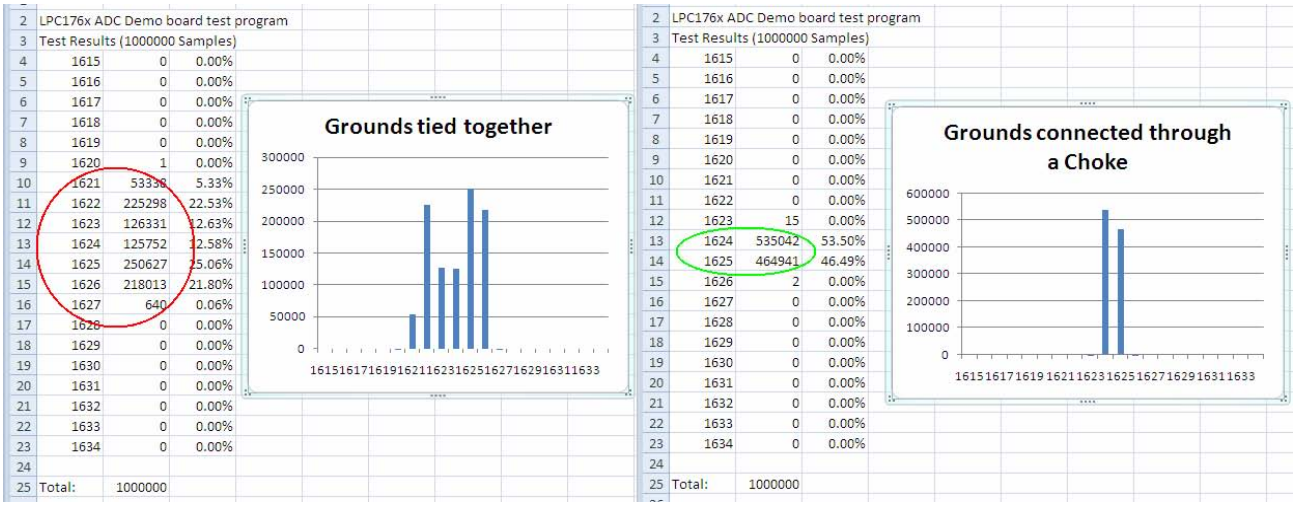


Fig 8. The effect of the ground planes

4.4 The effect of the power supply quality

Another source of noise is the power supply. Voltage fluctuations from the power supply will introduce noise which ultimately affects the ADC performance. In some cases, separate power supplies for each domain (Analog and Digital) could provide better results. See Fig 9.

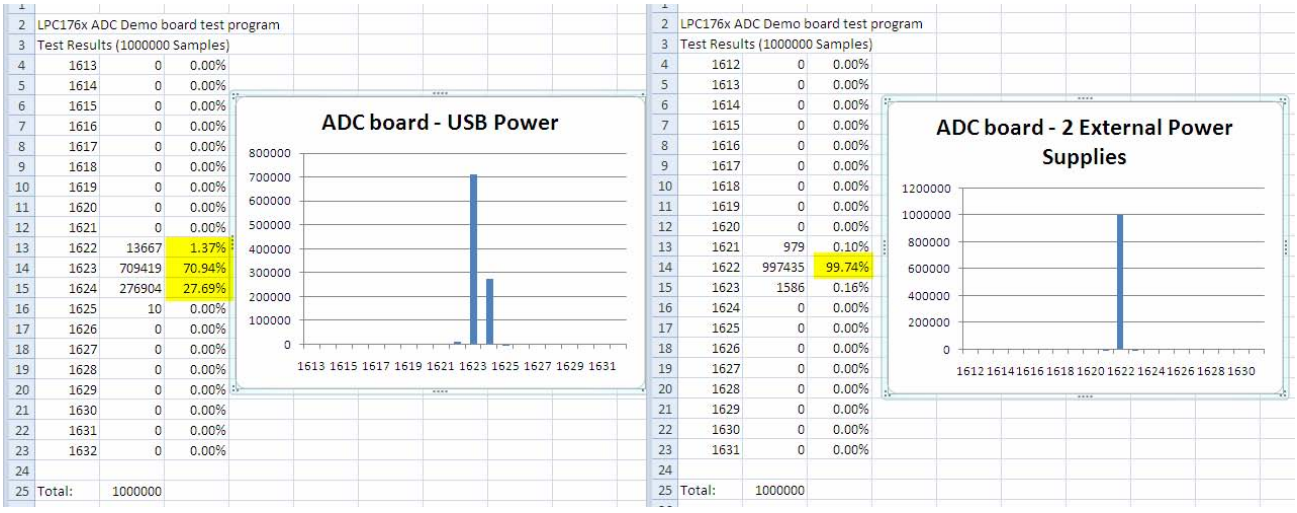


Fig 9. The quality of the power supplies improves the results

4.5 The effect of filtering the ADC channel input

A low-pass filter can dramatically improve the results, as Fig 10 shows. The LPC1768 ADC demo board includes capacitors implementing a low-pass filter on each of the ADC channel inputs. As not all these filters where populated in the board, this test shows how the response improves when the filter is present. In other cases, using Anti-Aliasing filters (with active components) will further improve the conversion response.

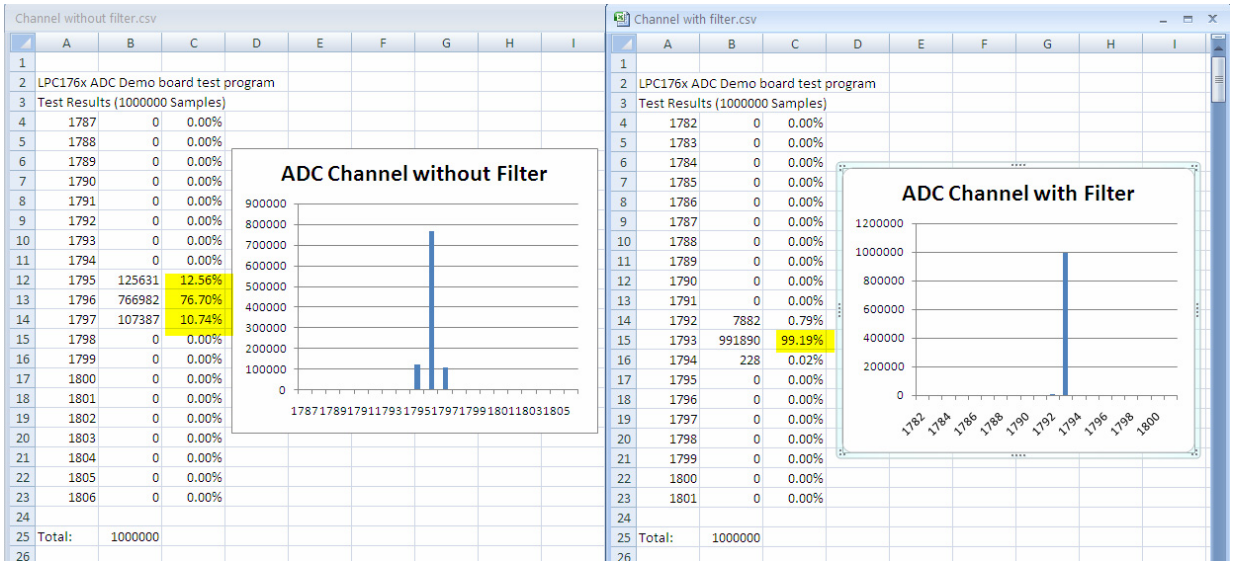


Fig 10. The use of low-pass filters will dramatically improve the results

5. Conclusion

Designing an accurate and reliable 12-bit ADC requires careful attention to board layout, power supply design and decoupling. The board trace layout should follow the design rules presented in this application note to help keep noise effects to a minimum. The use of two separate ground planes for each domain plays a fundamental role in the design. When possible, the use of separate power supplies for analog and digital domains will also contribute for successful results. Finally, filtering is an essential component in these cases.

6. Appendix A: Design guidelines

The following Design Guidelines provide common best practice for board layout required when Analog circuits (which are sensitive to digital noise) are combined with Digital circuits particularly when high-frequency or high-current circuits are involved.

6.1 Component placement

- Analog circuits should be separated from digital circuits to isolate them from switching noise.
- Noisy and high-frequency components should be located closer to the connectors/power supply.

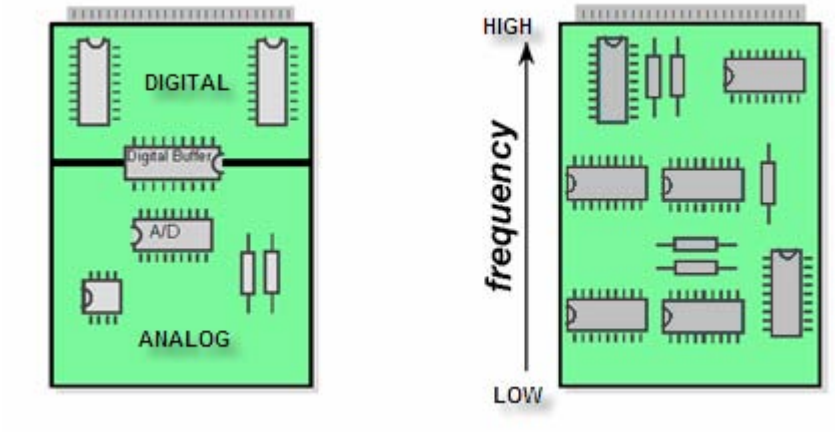


Fig 11. Recommended component placement

6.2 Ground strategy

- Use separate grounds for each domain (analog and digital)
- Use ground planes when possible
- If no ground plane is possible, use a “star” layout strategy for ground connections:
  - Provide independent ground current returns when possible.
  - Return paths can be shared (see U1 & U2) for low current/slow speed signals devices.
  - Make traces as wide as possible (the thinnest width will be the “effective” width for this trace, from this point to the end.
  - Avoid ground loops.
  - Digital currents should not pass across analog devices.
  - High-currents and High-speed currents should not pass across analog and lower speed parts.
  - In all cases, traces should be as short as possible, so effective inductance and resistance is low.

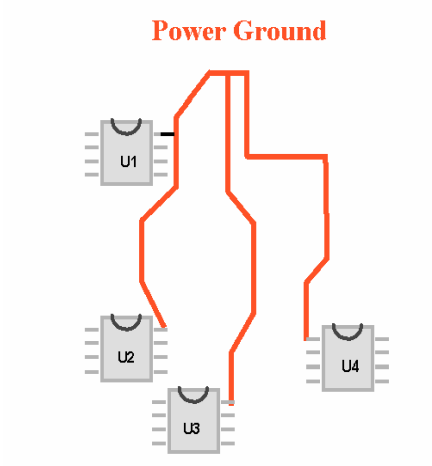


Fig 12. Star grounding layout

- When ground planes are used, use this as a current return path as much as possible.
- Create a separate ground plane for the analog parts, and have both analog and digital ground planes separated with a break.
- Avoid possible loops created between traces for ground return paths on the top-side and the ground plane at the bottom-side of the board.
- In the ground plane, ground currents will flow using the shortest path; if signal traces need to be inserted on the ground plane side of the board, they should be as short as possible and perpendicular to the ground current return paths.
- Even when separate grounds are used for analog and digital domains, only one electrical point should be referred to as the system-wide ground, i.e., both grounds should be connected together at a single point; this is commonly referred to as the chassis. A ferrite bead or inductor would work well for this connection while it will also decouple both circuits.

6.3 Bypass and decoupling capacitors

- A Bypass Capacitor offers a low impedance path to high frequency current flow, reducing the noise current on power supply lines. Usually, a 0.1 uF capacitor will suffice and it should be as close to the device as possible.
- A Decoupling Capacitor provides isolation of two circuits; this will prevent noise from being transmitted from one circuit to the other. It can be used with an inductor, forming a low pass filter. A 10 uF works well in these cases, and it should be connected close to the power supply.

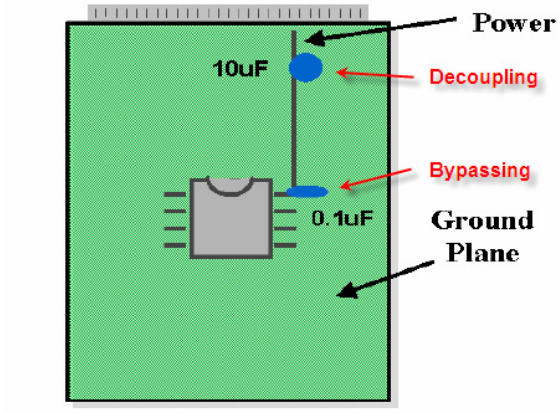


Fig 13. Bypass and decoupling capacitors

6.4 Power planes

- A Power plane is desirable although is not as critical as a ground plane.
- For two-layer boards, the power plane can be replaced by wider traces (two or three times wider than other traces on the board).

6.5 Multi-layer boards

- Critical and/or complex designs would require Multi-Layer boards.
- In this case, it's highly recommended to use different layers for ground and power planes.
- As many components are SMD (Surface Mounted Device), their connections need to be exposed on one of the external sides of the board (usually the top side), so internal layers can be dedicated to the power and ground planes, thus taking advantage from of the distributed capacitance.
- If more than four layers are used, higher speed signals can be shielded between the ground and power planes. Slower signals can be routed on the outer layers.

6.6 Routing signals

- Do not overlap signals/power/ground from different domains (analog and digital). Otherwise, the distributed capacitance between the overlapping portions will couple high-speed digital noise into the analog circuitry.

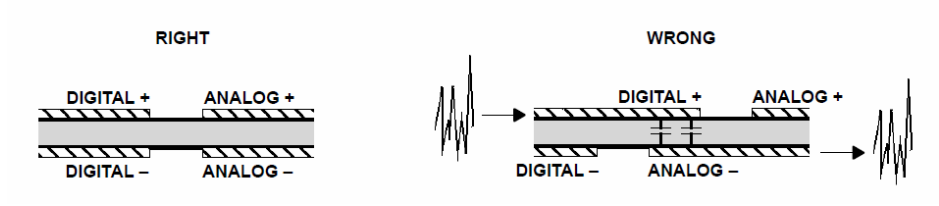


Fig 14. Routing signals

- Keep digital signals (especially high-frequency, noisy I/O or high-current) away from the analog signals. Even small capacitances between traces and planes could couple enough noise, not only for the fundamental frequency but also for the higher harmonics.
- High-impedance lines are the most sensitive to injected noise coupled through capacitance formed with close traces which have fast-changing voltages, such as digital clocks. In order to minimize this capacitance, the distance between the two traces should be increased, and both the length and thickness of the trace should be decreased.

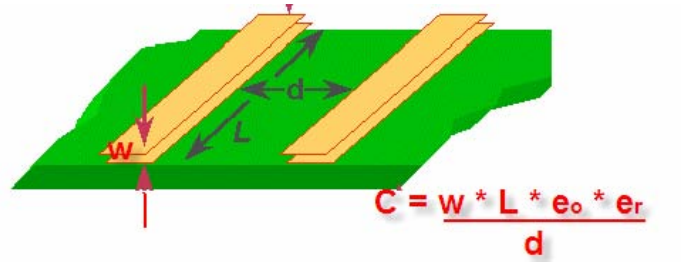


Fig 15. Recommended distance between traces

- Signal traces (in general) should be as short as possible, in order to minimize both parasitic inductance and capacitance.
- Avoid routing signal lines parallel to each other, in order to minimize crosstalk. If this is necessary, keep them separated by a gap of at least three times the signal trace width.
- Minimize loops between power and ground traces (when no ground plane is used), avoiding the “loop antenna” effect.

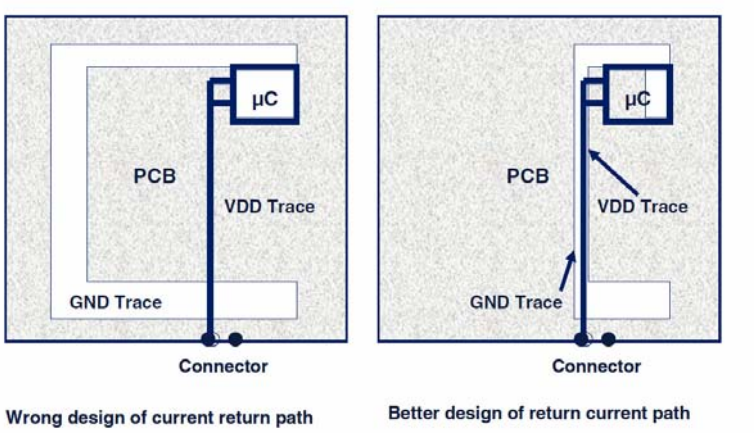


Fig 16. Recommended return current path

- Minimize reflection effect by rounding trace corners.

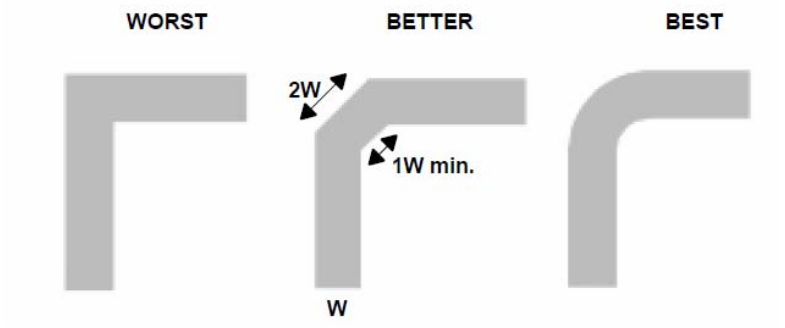


Fig 17. Minimize reflections by rounding the corners

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