AN11065

UHF Transmitter OL2300

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Document information

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Abstract	Provides application related information for the UHF transmitter OL2300. It focuses on schematic and layout recommendations for an application board and methods for enhancing the quality of the RF output signal.

Revision history

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1. Introduction

This application note provides application related information for the UHF transmitter OL2300. It focuses on schematic and layout recommendations for an application board and methods for enhancing the quality of the RF output signal.

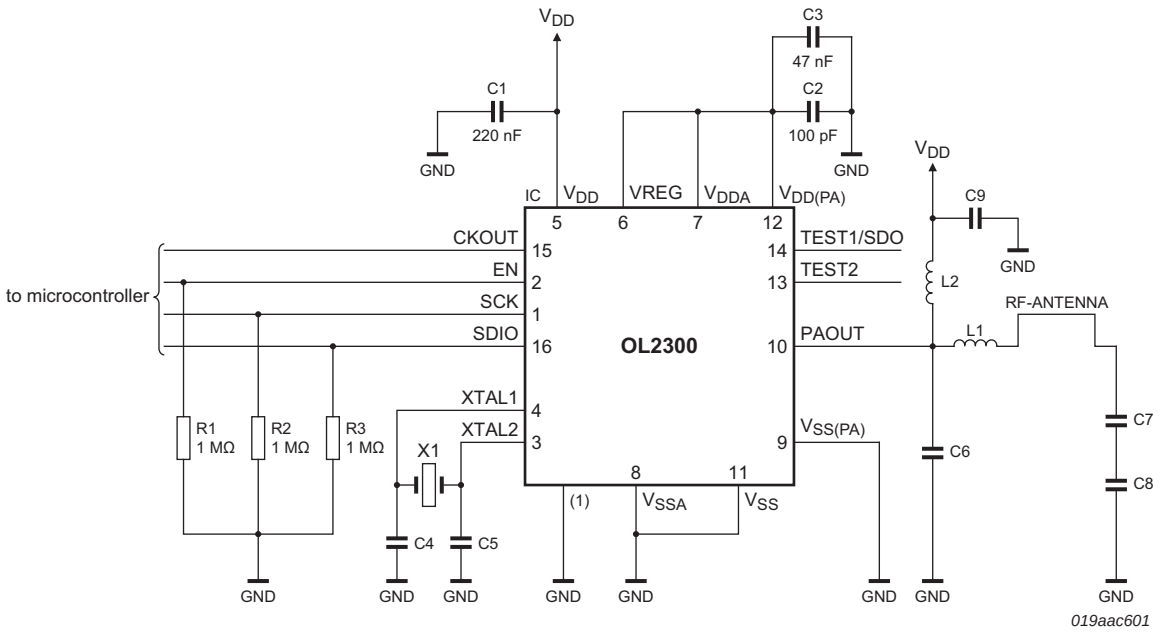
A note about the CKOUT signal is given in Section 6 on page 12.

Power measurements which are dependent on the output impedance are provided in Section 7 on page 19.

2. Board design

2.1 Schematic

The highly integrated design of the OL2300 requires only a few external components to build an RF transmitter. Figure 1 shows the OL2300 in a typical application.



(1) Exposed die pad.

Fig 1. Typical application schematic

The components used in this schematic are described in detail in Table 1. All parts marked with an asterisk are relevant to UHF performance and should be selected carefully. Special attention should be given to Self-Resonant Frequency (SRF) and quality factor Q.

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Table 1. Typical application component descriptions

Component	Description
R1, R2, R3	Pull resistors are required to avoid floating voltage levels at input ports EN, SCK, and SDIO. Undefined input ports leads to increased current consumption. External resistors must be applied if the connected SPI controller does not have internal ones.
X1, C4, C5	These three components form the external crystal resonator. The values of C4 and C5 should be chosen according to the load capacitance of the crystal. Both capacitors must have identical values.
C2[1], C3	C3 is used as a filter capacitor for the output of the on-chip voltage regulator. The value must be at least 47 nF. In addition, capacitor C2 with a value of 100 pF is inserted to inhibit output frequency feedback into the regulated voltage.
C1	The main supply filter capacitor value of C1 must be at least twice the value of C3.
L2[1], C9[1]	Choke inductance L2 provides the DC supply to the power amplifier. L2 and C9 decouple the RF signal from the DC supply V_{DD}. Value of L2 should be as high as possible, but in reality SRF and the quality factor limits the usable values of the coil. For an output frequency of 315 MHz it is recommended to select a value of 100 nH or 120 nH. The corresponding values are 82 nH for 434 MHz and 68 nH for 868 MHz. The inductor must be able to deliver up to 30 mA. For C9 a value of about 100 pF should be considered.
L1[1], C6[1], C7[1], C8[1]	Together with the RF-antenna, these elements form a low-pass Pi network that transforms the impedance of the antenna to the power amplifier input impedance. Capacitor C7 and C8 are connected in series, since the network output impedance is very sensitive to the capacitance provided by these components. L1 enables adjustment of antenna inductance and therefore the network quality factor. Capacitor C6 mainly sets the input impedance reactance. The OL2300 internal tuning capacitor is in parallel with C6.
Test1/SDO, Test2	Both port lines are outputs. Pin Test1/SDO can be configured by register settings as SPI data output. If not used, both pins must be left unconnected.

[1] Relevant to UHF performance, its value must be selected carefully.

2.2 Layout

An example of a two-layer PCB layout is shown in Figure 2.

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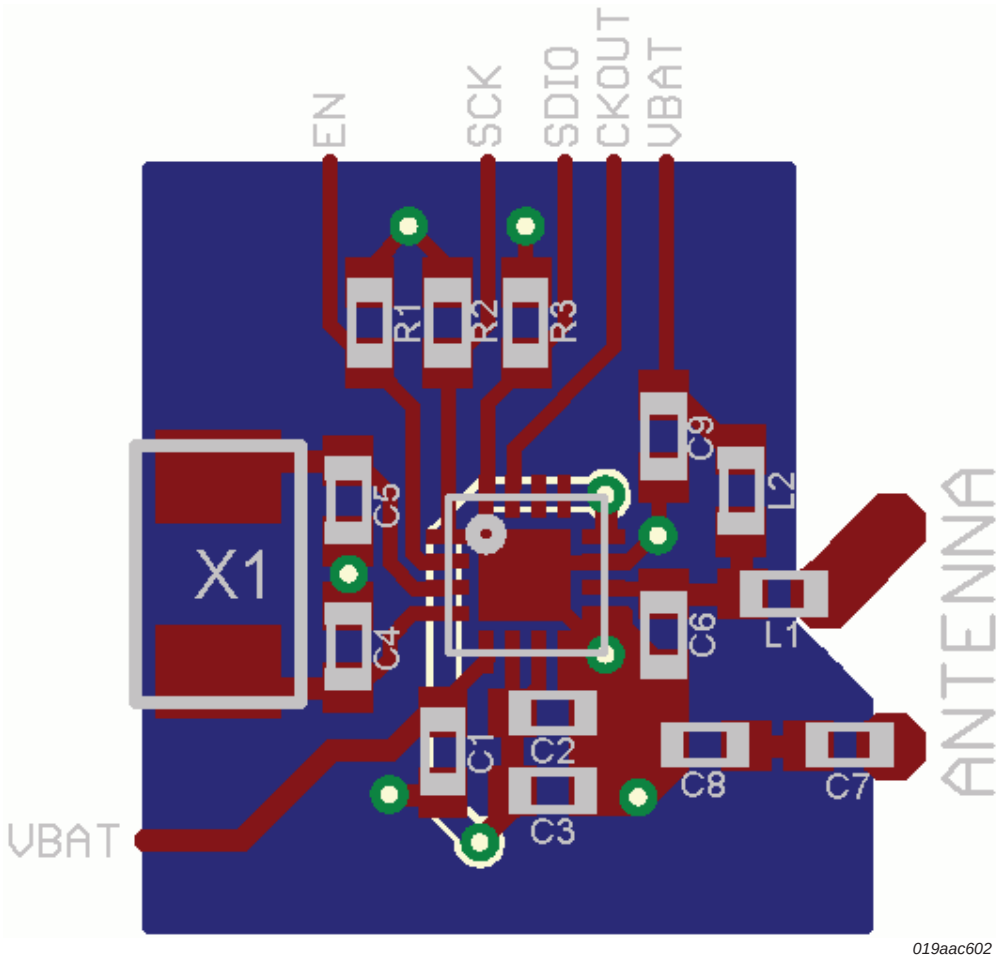

Blue: bottom layer; Red: top layer; Green: vias.

Fig 2. Two-layer PCB layout; HVQFN package

Table 2 gives guidelines for designing an appropriate layout.

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Table 2. Application PCB layout guidelines

Item	Guideline
Ground plane	A ground plane below the active RF-part and the crystal resonator is recommended for correct RF-power transmission and high frequency stability. In the given design, the ground plane is only discontinued by the connection VREG to VDDP. There must not be a ground plane below the antenna loop.
Antenna matching components	Antenna matching components must be placed with the shortest distance to the power amplifier output pin. Capacitor C6 is able to filter most harmonics. Therefore, C6 must be placed very close to PAOUT and VSSPA. L1 and L2 must be placed perpendicular to each other to avoid magnetic coupling. C7 and C8 must be placed close to each other. There must be a direct connection from C8 and C6 to VSSPA. Distance between the different components must be kept small. Also valid for VSSPA (GND) connection of C6, C8, and C9. Long ground connection lines on top must be shortened by placing vias to the bottom ground layer. This improves filtering and reduces spurious emissions.
L2 and C9	The choke should be applied directly to PAOUT. C9 must be grounded by a via.
Pad below the HVQFN package	The middle pad of the OL2300 HVQFN package must be connected to ground to improve output signal behavior. The via at pin 11 (VSS) can alternatively be placed directly in the middle of the pad below the package.
C2	C2 must be placed directly at VDDA and VSSA, to suppress the RF signal at the RF module supply.
Crystal resonator	The crystal and load capacitors must be placed close to XTAL1 and XTAL2 to minimize the influence of PCB parasitics.

3. Phase noise

The OL2300 uses a fractional-N based PLL to synthesize the output frequency.

Such a PLL consists of a programmable frequency divider stage. The frequency divider of the OL2300 is controlled by a 3-bit value which is used to divide the VCO-frequency by any integer value between 64 and 71. A non-integer (fractional) division of the VCO-frequency is feasible since the frequency divider control value changes with time.

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For this reason the control value consists of a fixed part and a time-dependent value provided by a 2-bit-sigma delta-modulator as shown in the OL2300 data sheet. The fixed part is given by the 3 MSBits of frequency control register FC, the frequency control value of the PLL. The 2-bit time-dependent value is defined by the remaining 15 LSBits of FC. The sigma-delta-modulator converts the 15-bit input to a time-dependent 2-bit output so that the mean value of the output signal equals the input.

The phase noise of the output frequency is slightly worse compared to an integer PLL due to the time-variant frequency divider. The FC value needs to be set carefully, as the variation in phase and amplitude of the output frequency of the OL2300 depends on this value.

3.1 Frequency modulation

The period of the time-dependent frequency divider control value provided by the sigma-delta-modulator depends on its input value. A short period leads to an increased phase noise at offset frequencies higher than 100 kHz. The modulator outputs a short period, in particular, if the input value FC is a multiple of the exponential function with base 2:

$FC = N \times 2^p$

The phase noise of the output frequency increases with the exponent p.

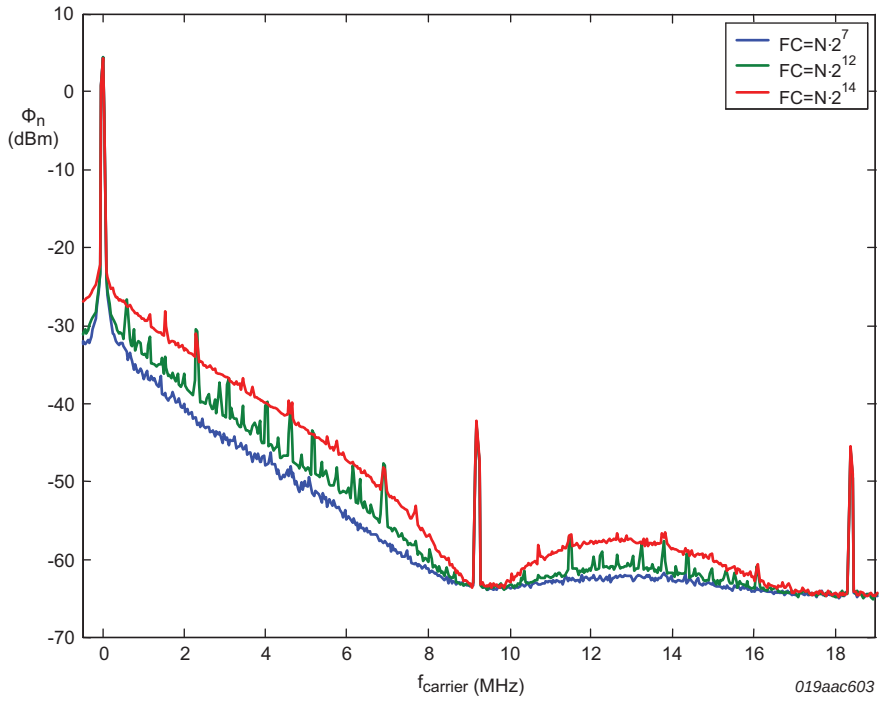

Fig 3. Phase noise as a function of carrier frequency

Figure 3 shows the output spectrum measured with different settings of FC. Factor N is an odd number of types:

$N = 2 \times k + 1$ for $k \geq 0$

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The spectrum has been measured in peak detection mode with a span of twice the reference frequency starting at the carrier.

Phase noise below an offset frequency of 100 kHz is constant and independent of the FC settings. For offsets greater than 100 kHz, the phase noise becomes an important parameter for applications with high data rates or FSK applications with a high modulation index. In such cases it is recommended to omit frequency control values (FC) in the range of ±50 around:

$FC = N \times 2^9$ for $0 \leq N \leq 320$

3.2 Amplitude modulation

Fractional-N based spurious emission appears in addition to reference spurs and harmonic emissions in the output spectrum of the transmitter. The distance (f_D) to the carrier frequency depends on the reference frequency and the input value of the sigma-delta-modulator, the 15 least significant bits of FC. Furthermore there is a dependency on the 3rd MSB of FC that doubles the distance as given in Equation 1 and Equation 2.

$$f_D = f_{REF} \times \frac{FC(14:0) + 0.5}{2^{16}} \quad (1)$$

for: $2^{14} < FC[15:0] \leq 3 \times 2^{14}$

$$f_D = f_{REF} \times \frac{FC(14:0) + 0.5}{2^{15}} \quad (2)$$

for the remaining values.

The amplitude of the emission increases as the distance to the carrier decreases. Figure 4 shows the output spectrum, measured with FC set to 103304d = 19388h (Equation 1 applies and FC[14:0] = 5000d = 1388h).

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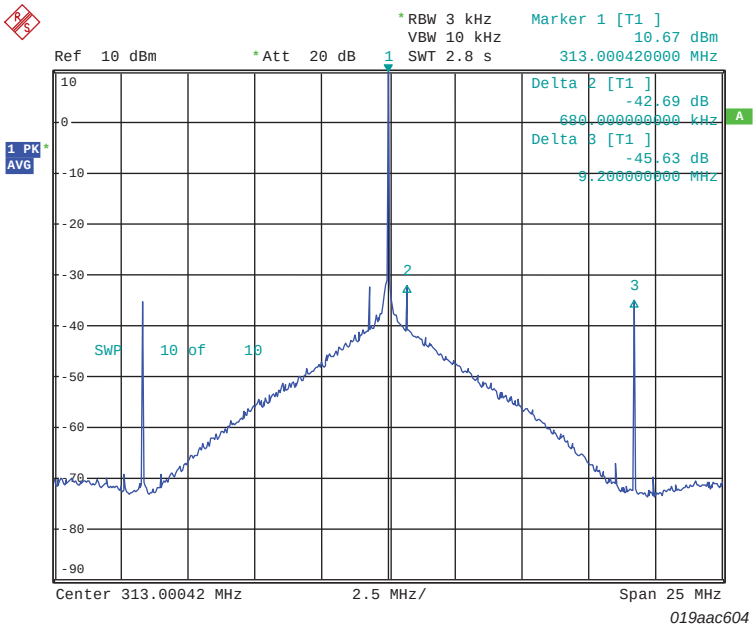

Marker 2 = fractional spurious.

Marker 3 = reference spurious emission.

Fig 4. Output spectrum FC set to 103304d = 19388h

To limit the amplitude of the fractional spurious emission to about −40 dBc it is recommended to avoid the following FC settings.

A range of ±8000 should be avoided around:

$FC = (2N + 1) \times 2^{15}$ for $0 \leq N \leq 2$

and a range of ±2000 should be avoided around:

$FC = 2N \times 2^{15}$ for $0 \leq N \leq 2$.

3.3 Inappropriate FC settings

Figure 5 shows the FC values that should be avoided according to the formulae above.

- The black marked values belong to the AM fractional spurs and should be avoided for all applications
- The blue values belong to the FM phase noise and should be avoided for applications using either a high data rate or a high FSK modulation index. Only the phase noise above an offset frequency of 100 kHz is affected by FM phase noise.

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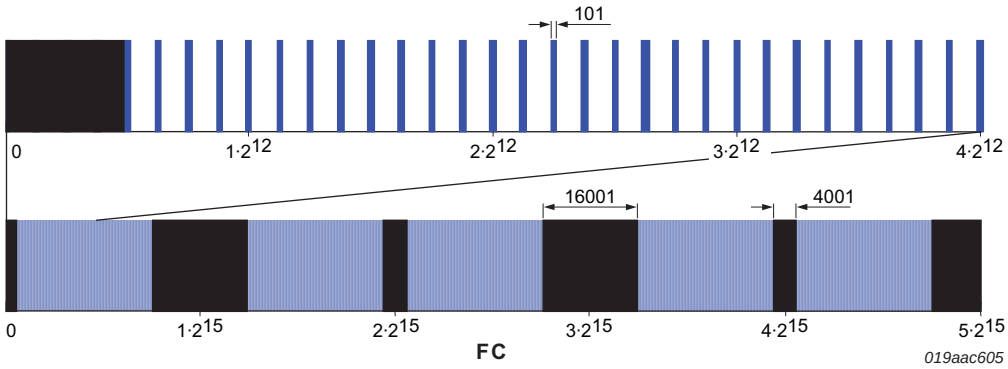

Fig 5. FC values to be avoided

The upper part of the diagram magnifies the first section of the available data range to make the blue marked values more visible. The lower diagram is scaled to the usable data range of FC.

For ASK, the FC value is constant and depends on the settings of the frequency control register FCxL, FCxH, and FCA. For FSK and Soft-FSK, the actual value of FC is time variable, according to the content of registers FCON and MRCON.

The given inappropriate settings of FC should be avoided according to the application requirements.

4. Reset conditions

Table 3 shows the reset condition of the special function register set. The device is reset and put in Power-down mode if pin EN is kept LOW for at least 2^{16} reference clock cycles or bit PD is set in register TXCON.

Table 3. Special function registers reset conditions

Name	Description	Address	Bit[1]							
			7	6	5	4	3	2	1	0
FC1H	frequency configuration 1, high byte	00h	X	X	X	X	X	X	X	X
FC1L	frequency configuration 1, low byte	01h	X	X	X	X	X	X	X	X
FC2H	frequency configuration 2, high byte	02h	X	X	X	X	X	X	X	X
FC2L	frequency configuration 2, low byte	03h	X	X	X	X	X	X	X	X
FC3H	frequency configuration 3, high byte	04h	X	X	X	X	X	X	X	X
FC3L	frequency configuration 3, low byte	05h	X	X	X	X	X	X	X	X
FC4H	frequency configuration 4, high byte	06h	X	X	X	X	X	X	X	X
FC4L	frequency configuration 4, low byte	07h	X	X	X	X	X	X	X	X
FCA	MSB for all frequency configurations	08h	X	X	X	X	X	X	X	X
FCON	FSK modulation control	09h	X	X	X	X	X	X	X	X
ACON0	ASK modulation control 0	0Ah	X	X	X	X	X	X	X	X
ACON1	ASK modulation control 1	0Bh	X	X	X	X	X	X	X	X
ACON2	ASK modulation control 2	0Ch	X	0	X	X	X	X	X	X
MRCON	modulation ramp control	0Dh	X	X	X	X	X	X	X	X

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Table 3. Special function registers reset conditions *...continued*

Name	Description	Address	Bit[1]							
			7	6	5	4	3	2	1	0
TXCON	transmitter control	0Eh	0	0[2]	X	X	X	X	X	0
BDSEL	baud rate selection	0Fh	X	X	X	X	X	X	X	X
SCSEL	scaler selection	10h	1[2]	0[2]	1[2]	1[2]	0[2]	0[2]	X	X
X	X	11h	X	X	X	X	X	X	X	X
TEST1	test1	12h	0	0	0	0	0	0	0	0
TEST2	test2	13h	0	0	0	0	0	0	0	0

[1] X = no reset condition, content stays unchanged during power-down.

[2] Only reset if SDIO = 0 otherwise X.

5. RF power trimming

Some applications require a very low spread of output power, independent of supply voltage and temperature.

It is mandatory for such applications to set bit CASC in register ACON2. A further reduction of the power dependency is achievable by adapting ACON according to changes in temperature and supply voltage. For this reason both parameters need be sensed. An adaptation of the output power leads to reduced current consumption over the lifetime of the system. Only the minimum required power is transmitted at any time.

The lifetime of battery-supplied systems can be increased if the ACON value is reduced at low temperatures. Typically, a battery's internal resistance increases over its lifetime. At low temperatures, the output voltage can reduce dramatically when the transmitter draws a high current from the battery. The OL2300 shows a negative dependency of the output power versus temperature. If the power is reduced to the minimum required value, the supply current is reduced too and thus the voltage drop over the battery. Hence the supply voltage is higher compared to unregulated use.

The ACON value can be used to trim the output power in the end-of-line test. If the value of ACON = 12 is used as standard for nominal power, a deviation of ±3 enables the actual output power in the range of ±2 dB to be adapted for a final precision of ±1 dB. Figure 6 shows the output power as a function of ACON for different power modes.

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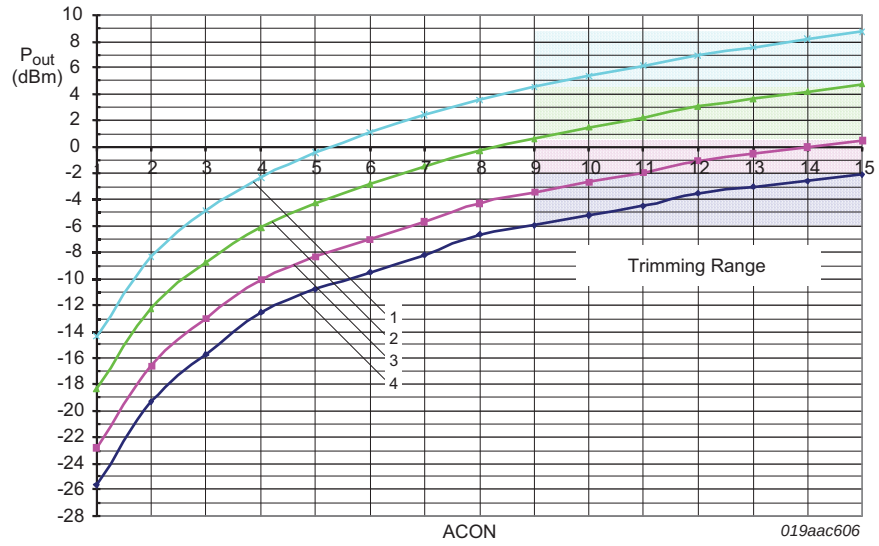

P_{out} = f (ACON, PAM).

V_{DD} = 2.7 V, CASC = 1, load impedance = 180 Ω.

(1) PAM 3.

(2) PAM 2.

(3) PAM 1.

(4) PAM 0.

Fig 6. Output power as a function of ACON

The colored areas in Figure 6 are addressable by ACON values 9d to 15d.

Due to a logarithmic dependency of the output power versus ACON setting, the best accuracy can be achieved for high ACON values. If lower output power is needed, the power mode should be reduced instead of reducing the ACON value.

6. XO Supply options

The OL2300 operationally supports the crystal oscillator with the regulated supply voltage VREG. In this mode the oscillator frequency shows virtually no dependency of the supply voltage. The regulated supply mode is activated if bit ENXR in register TXCON is set and the device is in the transmit state. It is possible to set bit ENXR during device initialization, but there will be no effect until the power amplifier is enabled by a transmit command. The oscillator supply automatically returns to unregulated mode if the transmit state is left.

The regulated supply voltage on pin VREG is either derived from an internal reference (fixed mode) or by the VCO supply voltage (adaptive mode). In the second case the actual voltage level depends on the PLL frequency. This mode is the regulator adaptive mode and is selected by flag ENRAD in register ACON2. In the adaptive mode, the OL2300 analog circuitry is supplied with the lowest possible voltage. This mode is the most power effective.

If the oscillator is operated in regulated supply mode and VREG is set to regulator adaptive mode, ENRAD must not be set before the power amplifier is activated. In unregulated mode, ENRAD can be set directly after PLL startup (after t_{acq}).

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Remark: Dropouts in clock output signal (CKOUT) might occur at the moment the oscillator supply switches from unregulated to regulated mode. It mainly occurs if the supply voltage is above 3.3 V. The behavior is caused by the internal time-constant of the clock-buffer reference. This reference is derived from the signal amplitude at pin XTAL1. The amplitude changes by switching to the regulated mode, and the clock-buffer reference voltage settles to a new value. While settling, the clock signal might be absent.

6.1 Sequence for fixed low mode

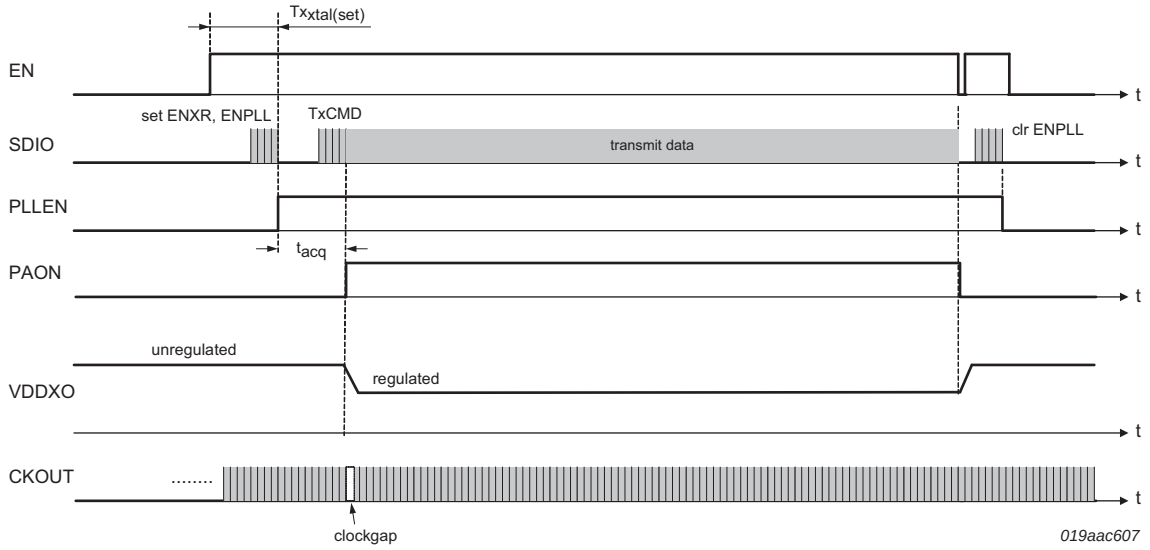

Fig 7. Fixed low mode sequence

How long the clock is missing (clock gap time) depends on supply voltage, crystal oscillator frequency, the value of the crystal load capacitors, temperature, and also on process parameters. The worst case was found for high crystal frequency, high temperature, and if the process shows high p-channel thresholds. A maximum gap time of 4 μs appears under worst-case conditions at 3.6 V and 125 °C. This value was measured and simulated using an 18.37 MHz crystal (Nx5032GA). The gap time needs to be considered if the external controller uses the clock signal.

Remark: If the nominal crystal frequencies can only be reached by unsymmetrical load capacitances, the capacitor with the highest value should be applied to pin XTAL1. This reduces the amplitude at pin XTAL1 and thus the settling time of the clock-buffer reference voltage.

Example:

Crystal: Nx5032GA

Nominal frequency: 18.37 MHz

Load capacitance: 12 pF

Pin XTAL2 → 18 pF

Pin XTAL1 → 22 pF

Without pin capacitance of pins XTAL1 and XTAL2 and PCB parasitic.

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6.2 Sequence for adaptive mode

To use the regulator adaptive mode in conjunction with the regulated supply mode of the oscillator (bit ENXR = logic 1, bit ENRAD = logic 1), the power amplifier should be activated first in fixed low mode and then the ENRAD bit can be set.

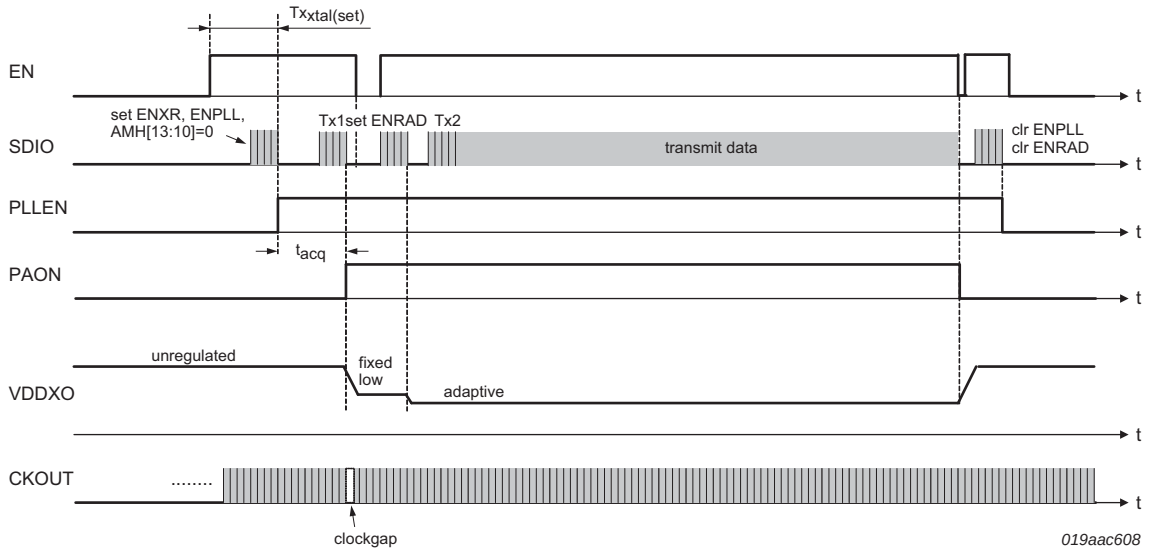

Fig 8. Adaptive mode sequence

Tx1: transmit command: bit B = logic 0, bit C = logic 0, bit D = logic 1: PA is switched on, no output power as AMH[13:10] = 0.

Tx2: transmit command: bit B = logic 1, bit D = logic 0 actual output power depends on AMH[03:00].

After Tx1, pin EN goes LOW and the actual value on pin SDIO is latched (in this case pin SDIO needs to be LOW to have an unmodulated output signal) the PA is activated and the ACON1 setting is used (no output power).

With the Tx2 command the data is transmitted at an output power according to ACON0.

Remark: Bit ENRAD needs to be cleared before the PLL is enabled again; see Section 4 on page 10.

6.3 Application advice

The device supports a second fixed mode, the fixed high mode. The regulator operation is similar to the fixed low mode; the regulator output is stabilized to a fixed value. In fixed high mode the regulated voltage is about 200 mV higher compared to fixed low mode.

This mode is only available via test register TEST1. Fixed high mode is activated by writing 0x08 to TEST1 and is deactivated by writing 0x00. This mode can be used to reduce the voltage drop of the crystal oscillator supply in regulated supply mode.

Using fixed high mode as shown in Figure 9 avoids gaps in the clock signal at pin CKOUT.

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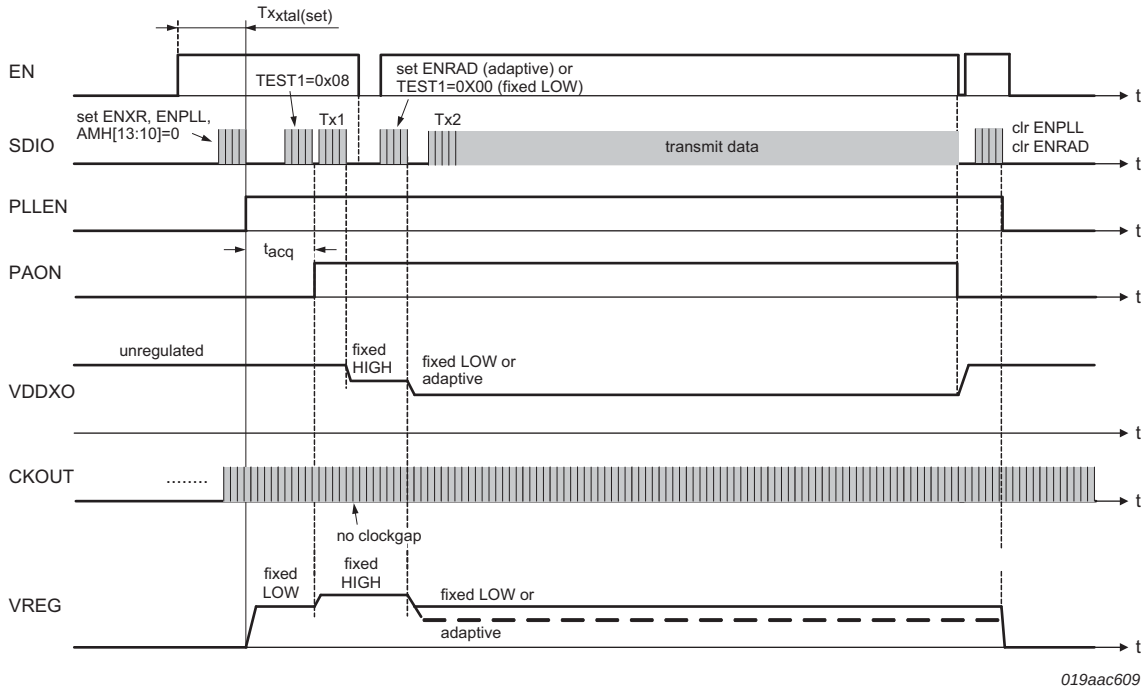

Fig 9. Fixed high mode sequence

Tx1: transmit command: B = 0, D = 1, PA is switched on, no output power as AMH[13:10] = 0.

Tx2: transmit command: B = 1, D = 0, actual output power depends on AMH[03:00].

The PLL startup should be performed in fixed low mode. The fixed high mode is activated after t_{ACQ}. Tx1 (B = 0, D = 1) enables the power amplifier with no output power (after falling edge of pin EN while pin SDIO is LOW). An additional command activates the adaptive mode or fixed low mode. After selecting the supply condition, the data transmission can be started (Tx2 command). In Figure 9, the transparent mode is selected but synchronized data transmission is also possible.

6.4 Soft modulation schemes

The OL2300 supports bandwidth-reducing modulation schemes for ASK and for FSK. In both cases the required bandwidth of the emitted RF signal is reduced by low-pass filtering of the baseband signal. The low-pass characteristic of the filter is flexible and can be adjusted according to the requirements of the application.

Filtering is implemented by linear interpolation of intermediate steps in each transition. This transforms the rectangular shape of the baseband data signal to a trapezoid shape. The slope is adjustable by defining the transition time via special function register MRCON.

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6.5 ASK

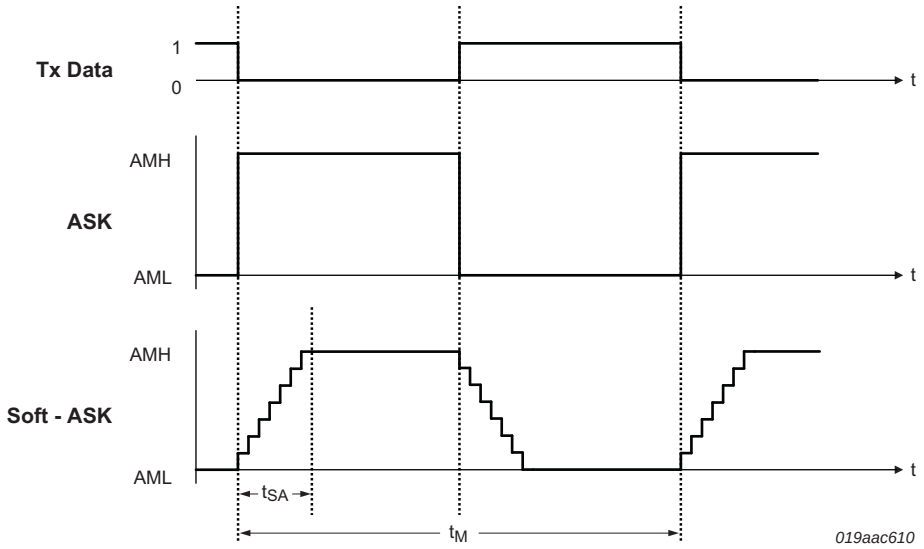

Fig 10. ASK soft modulation

The number of intermediate steps for ASK is limited according to the driver stage of the power amplifier. A staircase replaces each transition. The actual number of steps depends on the settings of the ACON registers.

n = AMH − AML[3:0].

The slope time t_{SA} is defined by the value of RMP[6:0] in register MRCON.

$$t_{SA} = n \times \frac{RMP}{f_{REF}} \tag{3}$$

$$t_{SA} \leq \frac{t_M}{2} \tag{4}$$

The slope time needs to be limited in relation to the modulation frequency. If the timing exceeds the limit, the modulation index will be scaled down.

The ASK baseband filter function is a number of Dirac pulses.

$$S_{ASK}(t) = \frac{1}{n}\left(\sum_{i=0}^{n-1} \delta\right)\left(t - t_{SA} \times \frac{i}{n}\right) \tag{5}$$

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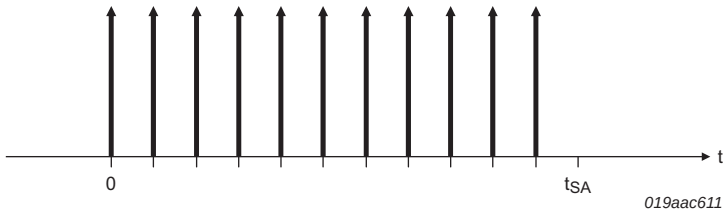


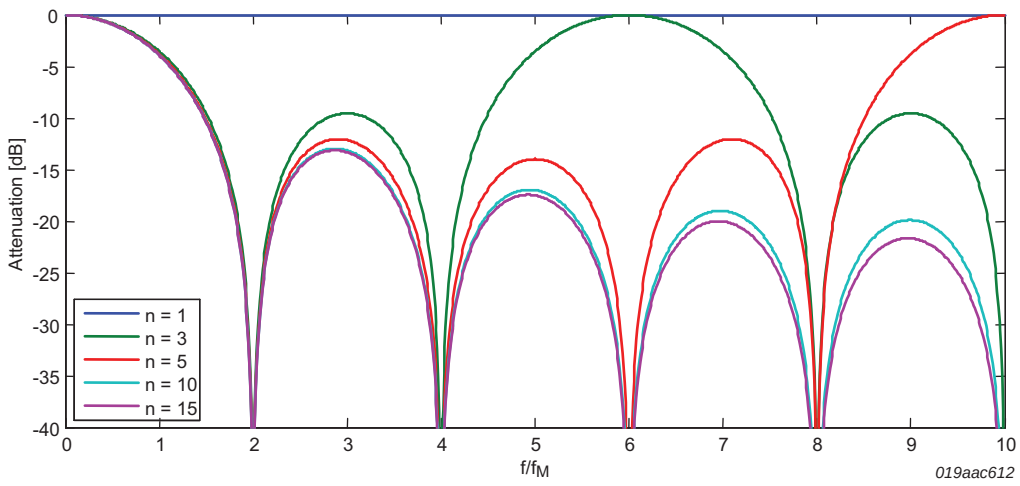
$s_{ASK}(t)$, shown for n = 11.

Fig 11. ASK baseband filter function

The capability of the filter function to limit the bandwidth strongly depends on the number n. In general, the required bandwidth will decrease for high n and a long slope time.

Equation 6 shows the power-related filter function in the frequency domain.

$$S_{ASK}(f) = \left| \frac{1}{n} \left(\sum_{i=0}^{n-1} e^{-j2\pi f \cdot t_{SA} \cdot \frac{i}{n}} \right) \right|^2 \quad (6)$$



ASK filter function $S_{ASK}(f)$, shown for $t_{SA} = t_M/2$.

Fig 12. ASK filter function in the frequency domain

6.6 FSK

Due to the capability of the PLL, the number of intermediate steps is usually much higher and for FSK a smooth transition is achieved.

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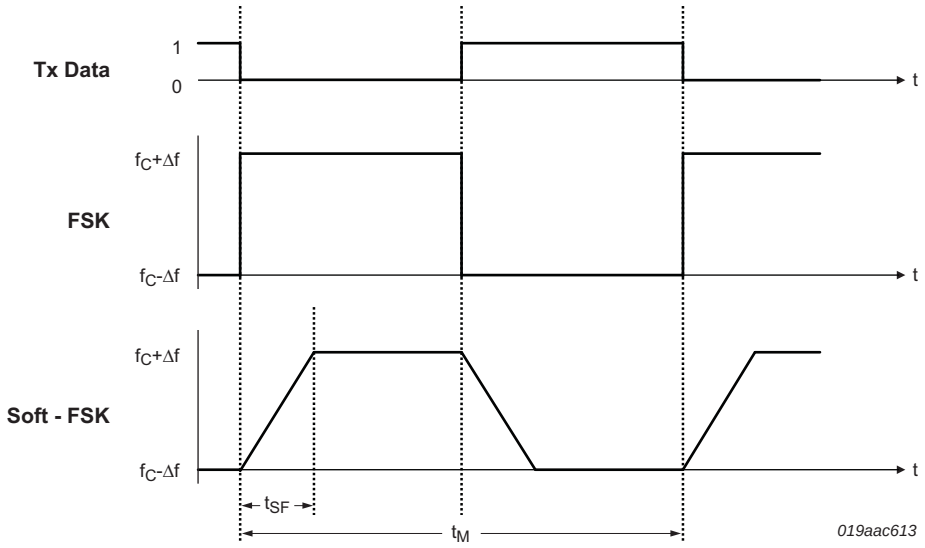


Fig 13. FSK soft modulation

For FSK, the slope time t_{SF} is defined too by the value RMP in register MRCON.

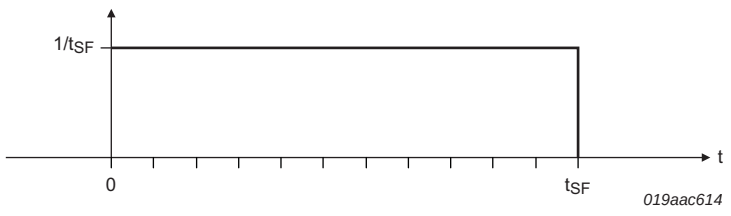
$$t_{SF} = (2 - FBSL) \times \frac{2 \times FSK \times RMP}{f_{REF}} \quad (7)$$

$$t_{SF} \leq \frac{t_M}{2} \quad (8)$$

The slope time needs to be limited in relation to the modulation frequency. If the timing exceeds the limit, the frequency deviation is reduced. The FSK value in register FCON sets the frequency deviation. The flag FBSL is part of the transmitter control register TXCON.

According to the increased number of intermediate steps, the FSK baseband filter function can be assumed to be a rectangular pulse.

$$S_{FSK}(t) = \frac{1}{t_{SF}} \begin{bmatrix} 1, & 0 \leq t < t_{SF} \\ 0, & t < 0 \\ 0, & t \geq t_{SF} \end{bmatrix} \quad (9)$$



FSK baseband filter function $S_{FSK}(t)$.

Fig 14. FSK baseband filter function

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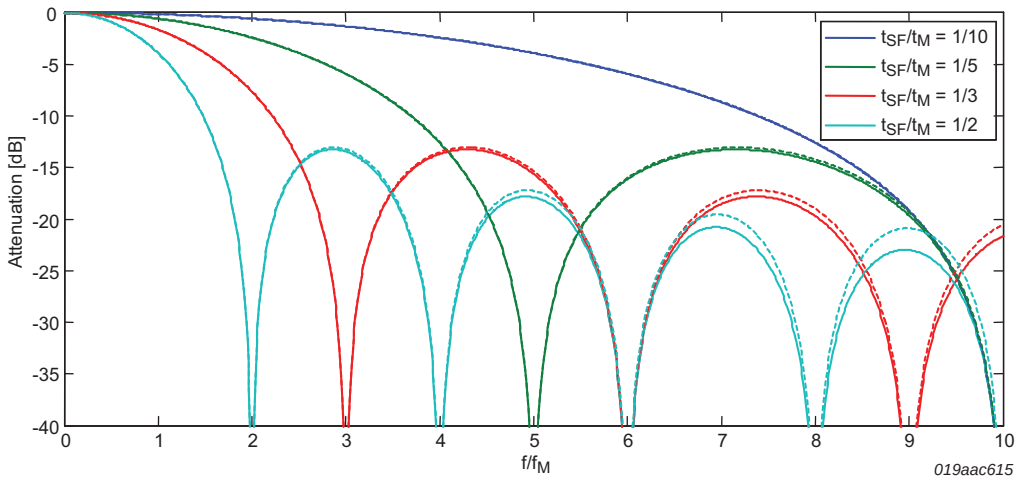
Equation 10 shows the power-related filter function in the frequency domain.

$$S_{FSK}(f) = \left|\frac{sin(\pi f t_{SF})}{\pi f t_{SF}}\right|^2 \quad (10)$$



$S_{FSK}(f)$ in relation to $S_{ASK}(f)$ with n = 12 (dashed).

Fig 15. Different FSK filter functions related to ASK filter function

7. Optimum output impedance

Output power and supply current were measured at different output impedances.

Two power setups were investigated at different output frequencies for the following parameters:

Temperature T = [–40, 25, 85] °C

Supply voltage V_{DD} = [2.1, 2.4, 2.7, 3.0, 3.3, 3.6] V

Measurements were performed on one part. Depending on the output frequency, either a device variant VHN or NHN was chosen. As the investigations were limited to one part, only the typical performance of the OL2300 is shown here.

Two consecutive measurements were applied for each frequency setup.

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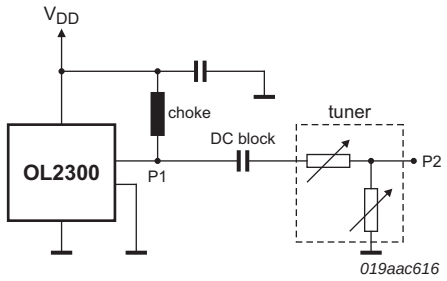

Fig 16. Measurement setup

In the first measurement, P1 and P2 were connected to a network analyzer to determine the impedance applied to the power amplifier and the power loss inside the tuner for specific tuner settings. At the same tuner settings the output power at P2 was measured in a second step. For this the network analyzer was removed from P1, P2 and then connected to a spectrum analyzer. In both measurements, the OL2300 was initialized output frequency dependent, with the parameters shown in Table 4. The PLL was always switched on. The power amplifier was enabled for the second measurement.

Measurement point P1 corresponds to the position of capacitor C6 in the layout recommendations given in Section 2.2 on page 4.

The following information is represented in Smith charts based on 50 Ω in the sections below.

- effective output power provided by the OL2300 and the corresponding supply current dependent on the applied impedance
- dependency of temperature and supply voltage on output power and supply current

Table 4. Frequency setup with corresponding parameter set

Parameter	Frequency			
	315 MHz	434 MHz	868 MHz	915 MHz
f_{osc}:	18.37036 MHz	13.28963 MHz	13.28963 MHz	13.28963 MHz
Bit XOSL:	1b	0b	0b	0b
Bit FBSL:	0b	0b	1b	1b
ACON[23:0]:	15d	15d	15d	15d
Bit ENXR:	1b	1b	1b	1b

Table 5. Power setups

Parameter	Power setup	
	1	2
PAM (power amplifier mode)	2	3
Bit CASC	1b	0b
Bit ENRAD	1b	0b

Power setup 1:

PAM2 (power mode 2)

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- High power
- Low stability

CASC1, ENRAD1

- Further stabilized and regulated output power
- Slightly reduced power

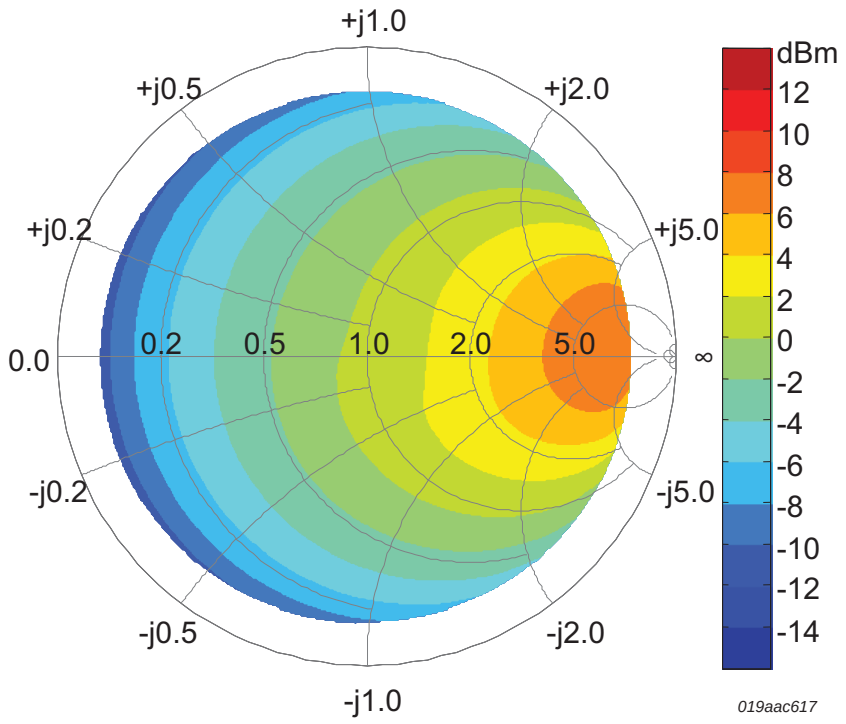
Power setup 2:

PAM3 (power mode 3)

- Maximum power
- No stabilization

7.1 Optimum output impedance measured at 315 MHz

7.1.1 Power setup 1



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 17. Output power with applied impedance at 315 MHz; power setup 1

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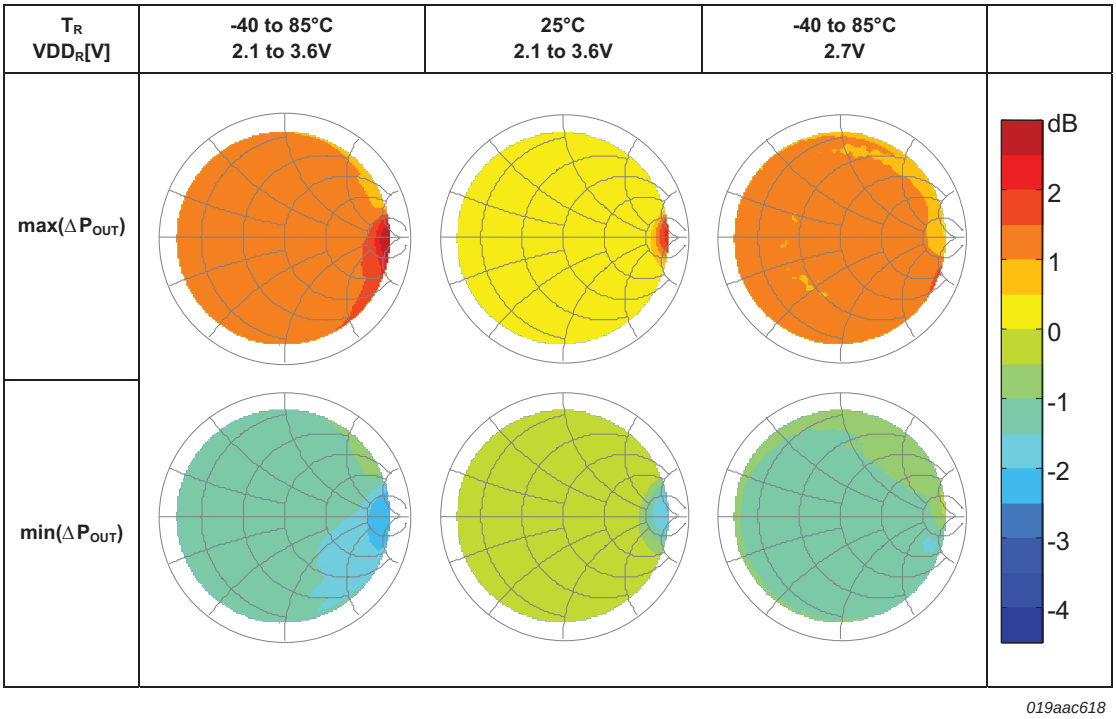

Output power deviation: $\Delta P_{OUT} = P_{OUT}(T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 18. Output power deviation at 315 MHz; power setup 1

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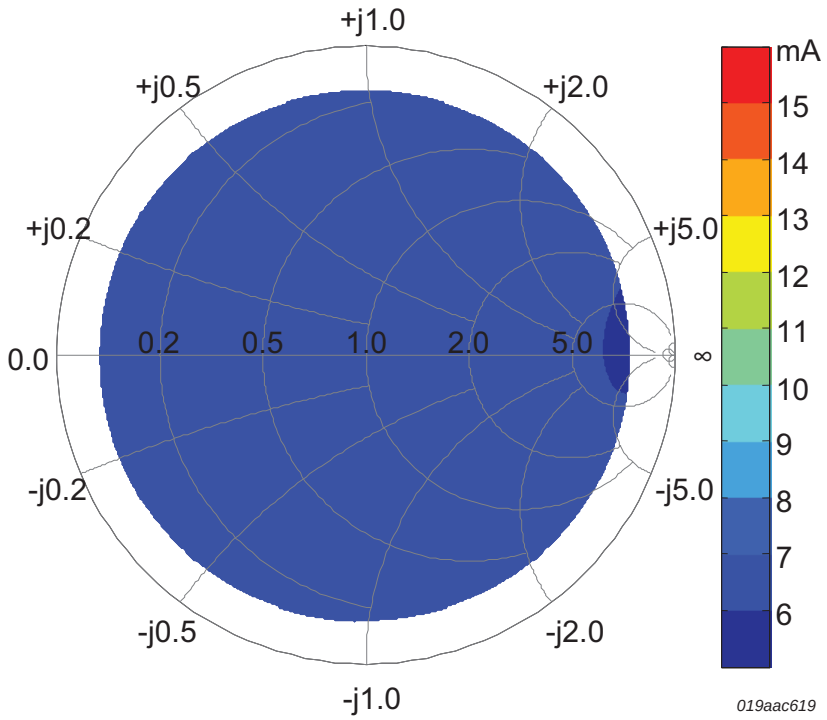

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 19. Supply current with applied impedance at 315 MHz; power setup 1

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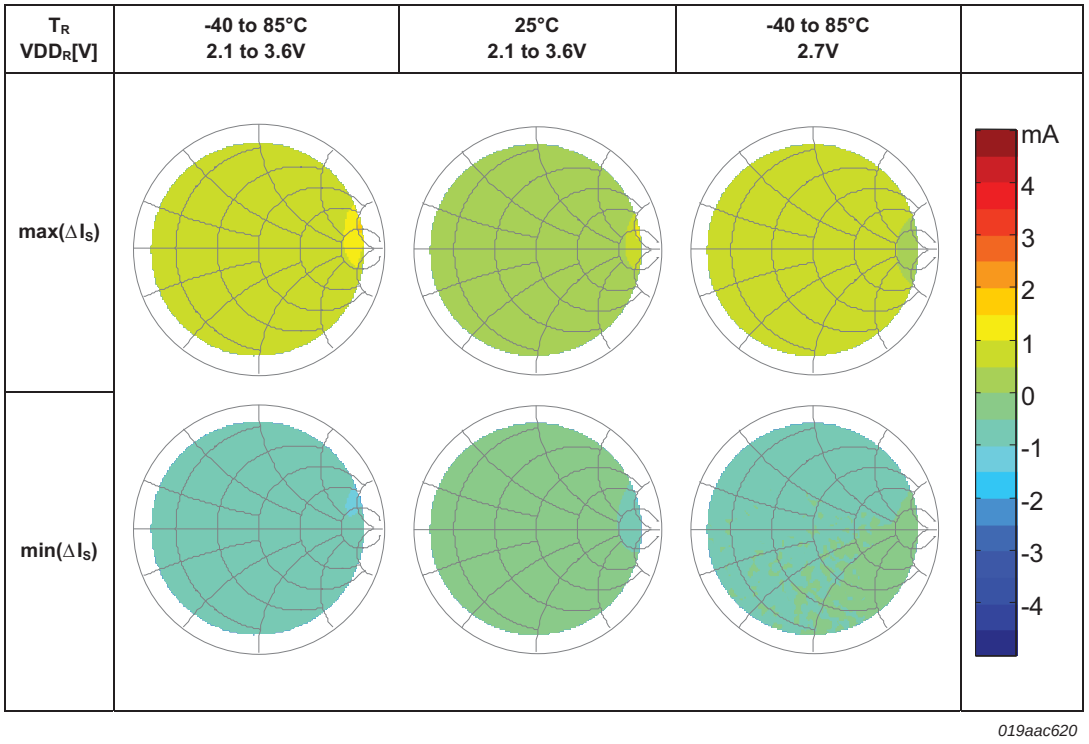

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 20. Supply current deviation at 315 MHz; power setup 1

This setup provides excellent performance for an output power of about 5 dBm. The output impedance should be chosen to be 250+j0 Ω. At this point the output power at pin PAOUT is about 7 dBm; assuming a power loss of about 1 dB in the matching network provides an available power of 6 dBm. By trimming parameter ACON, an output power of 5 dBm can be reached.

The overall stability of the output power is about ±1.5 dB at this matching point.

With increased impedance, the temperature stability increases but the supply voltage stability decreases.

The imaginary part of the impedance should be about 0 Ω. For mass production it may be better to choose a small imaginary part of about +50 Ω. Depending on the variation in values of the components comprising the matching network, the actual matching impedance can differ between devices. Adding a small imaginary part to the optimum output impedance ensures that all devices will have an imaginary part that is not less than 0 Ω. The output power deviation figure shows a slightly worse temperature stability behavior in this area. The current supply is about 6.5 mA ± 1 mA at this point.

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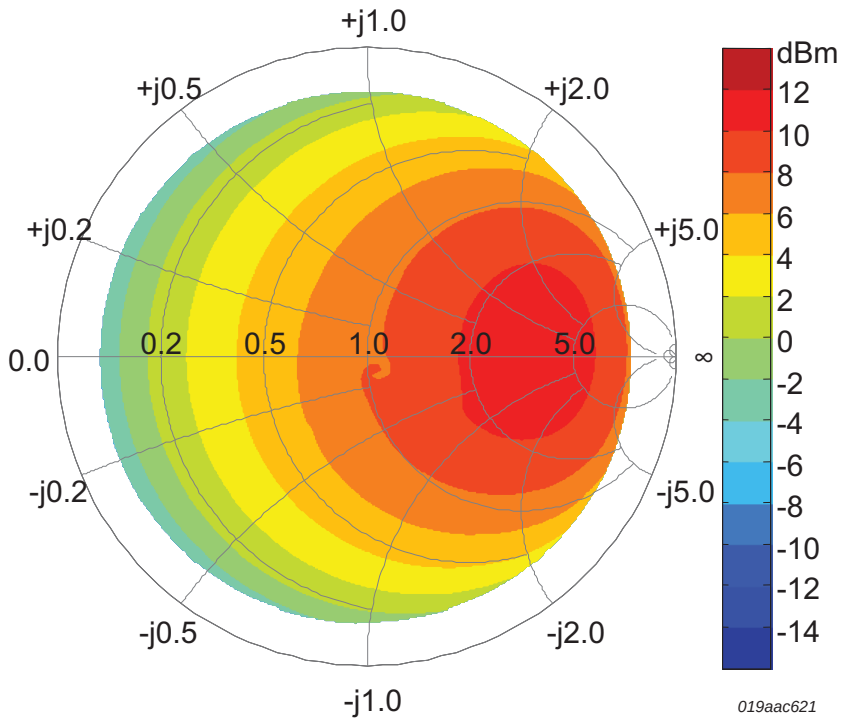
7.1.2 Power setup 2



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 21. Output power with applied impedance at 315 MHz; power setup 2

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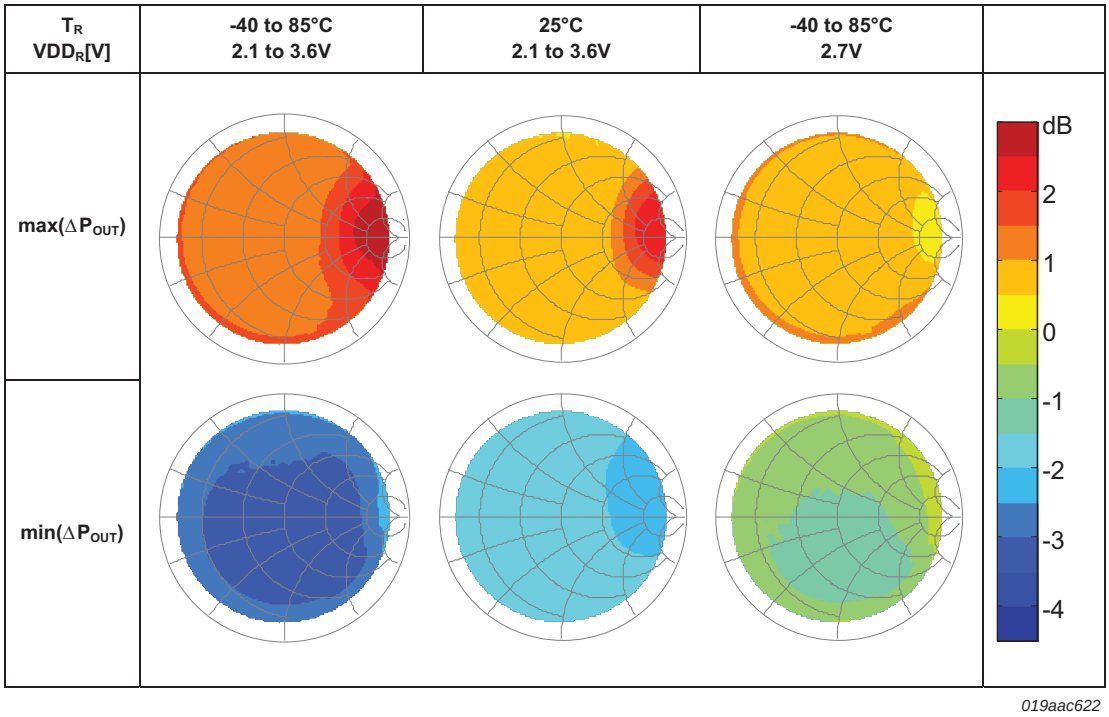

Output power deviation: $\Delta P_{OUT} = P_{OUT}(T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 22. Output power deviation at 315 MHz; power setup 2

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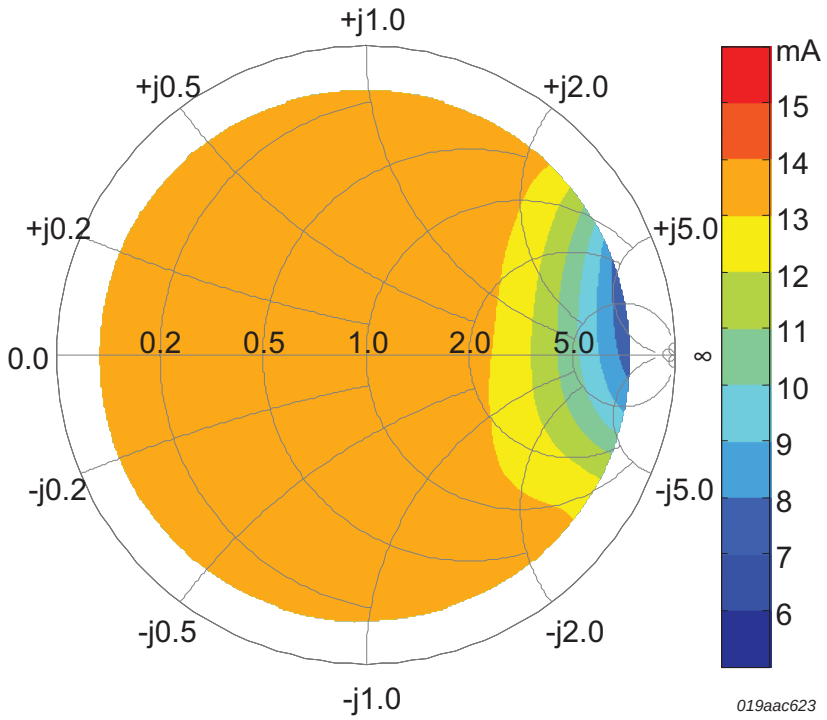

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 23. Supply current with applied impedance at 315 MHz; power setup 2

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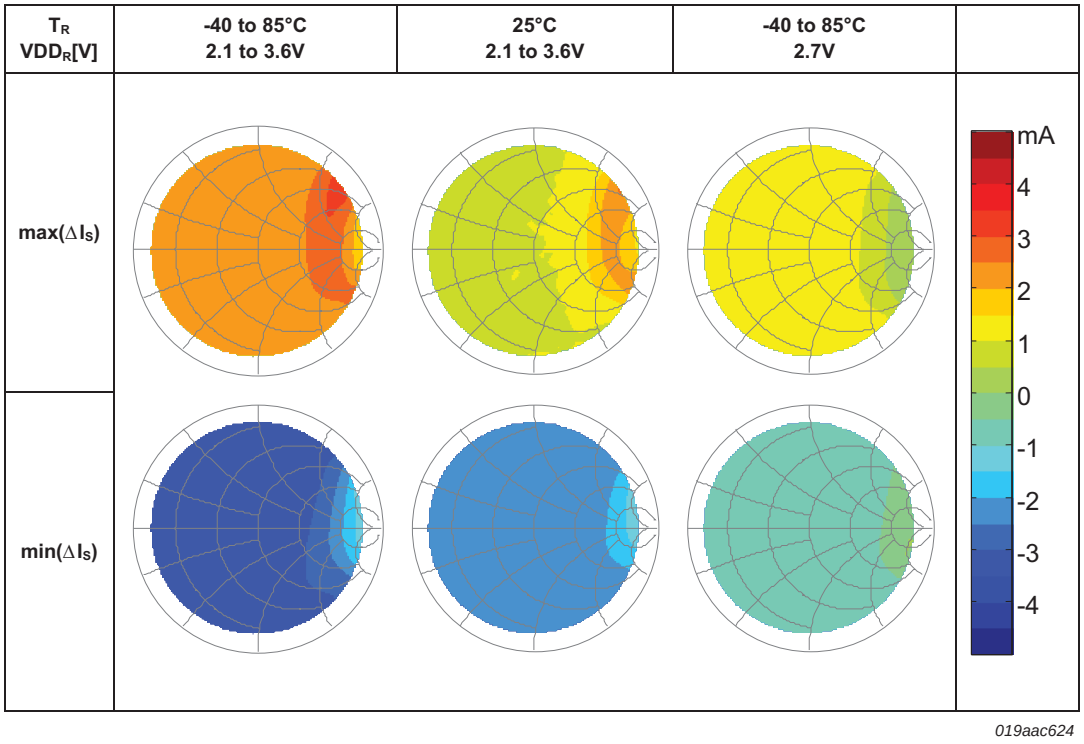

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 24. Supply current deviation at 315 MHz; power setup 2

Power setup 2 provides a maximum output power at pin PAOUT of 11 dBm at 25 °C with a 2.7 V supply. This value is reached with an output impedance of 160 + j10 Ω.

The optimum impedance varies with supply voltage and temperature. The real part of the optimum impedance increases with an increase in supply voltage and decreases with an increase in temperature.

At the given output impedance of 160 + j10 Ω, the output power shows a deviation of +2 dB/–3 dB with temperature and supply voltage. The output power is more unstable with changes in supply voltage than it is with changes in temperature.

The current supply is about 12 mA ± 2.5 mA for optimum output impedance.

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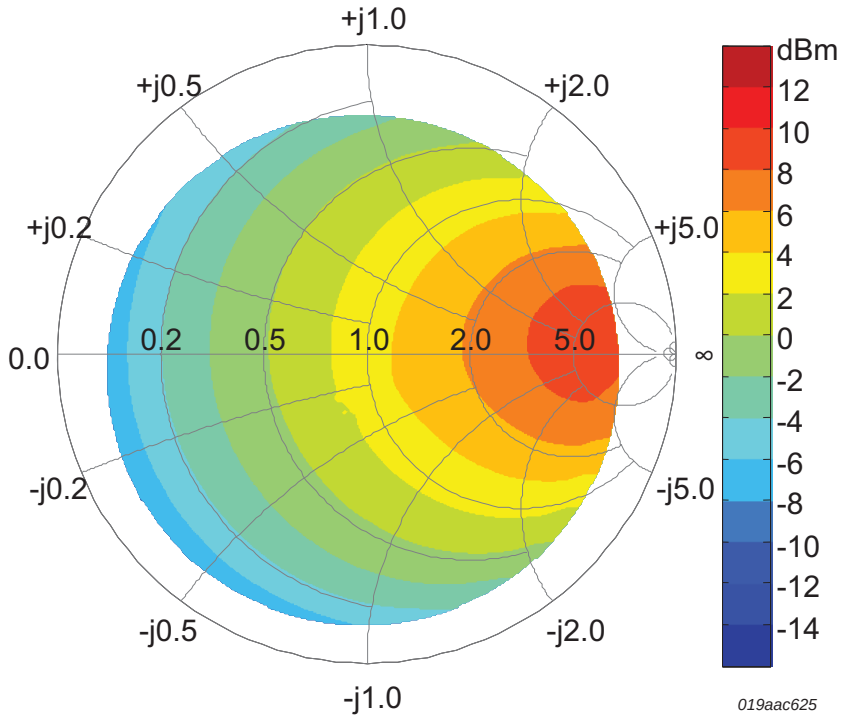
7.2 Optimum output impedance measured at 434 MHz

7.2.1 Power setup 1



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 25. Output power with applied impedance at 434 MHz; power setup 1

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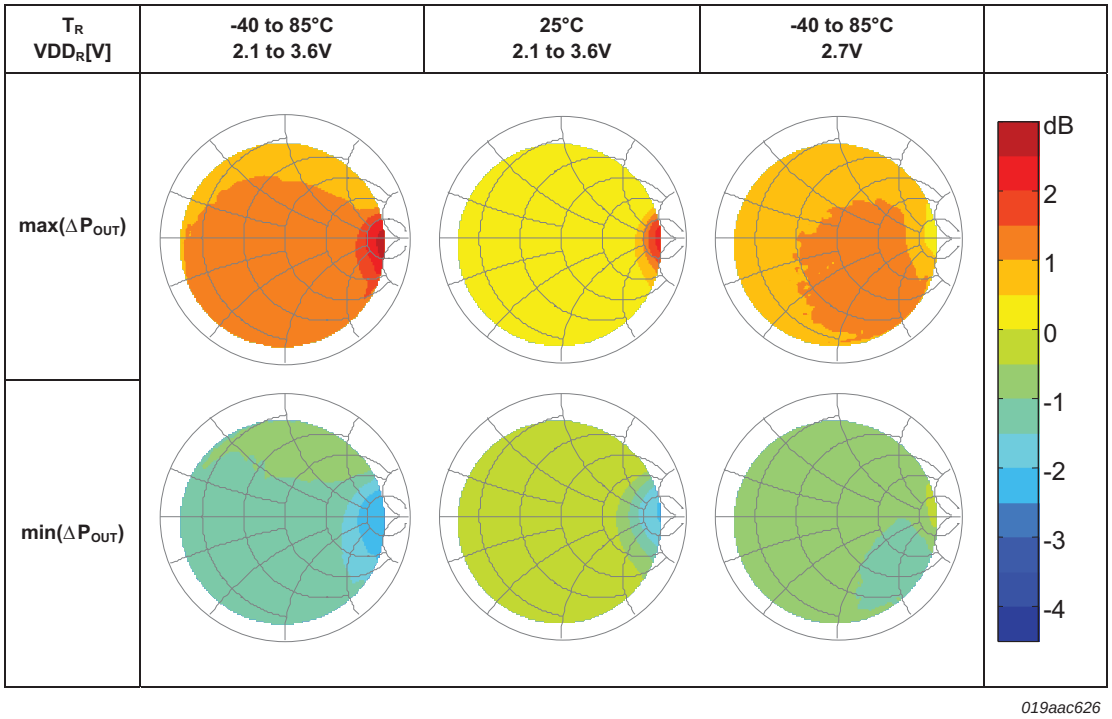

Output power deviation: $\Delta P_{OUT} = P_{OUT}(T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 26. Output power deviation at 434 MHz; power setup 1

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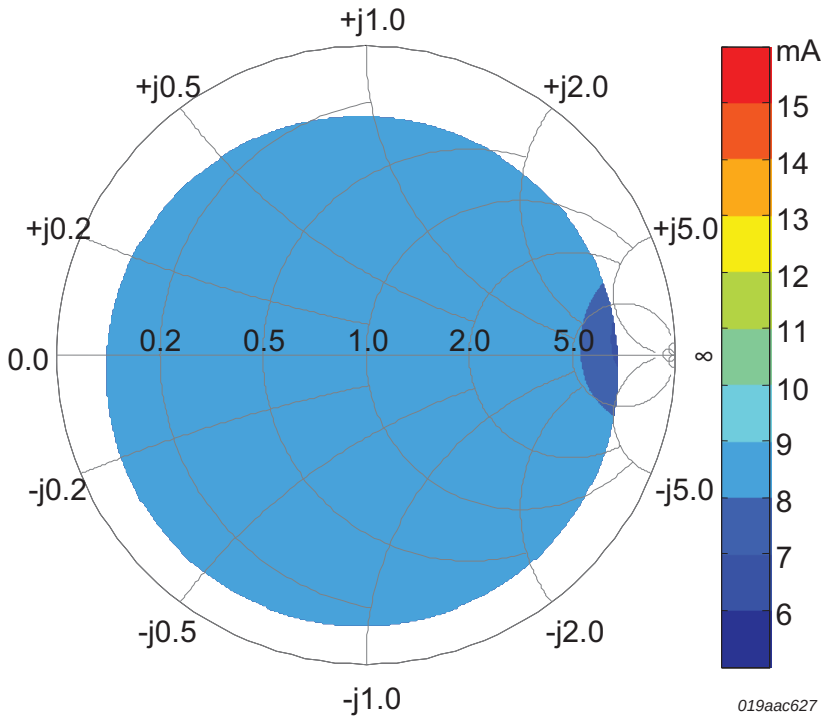

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 27. Supply current with applied impedance at 434 MHz; power setup 1

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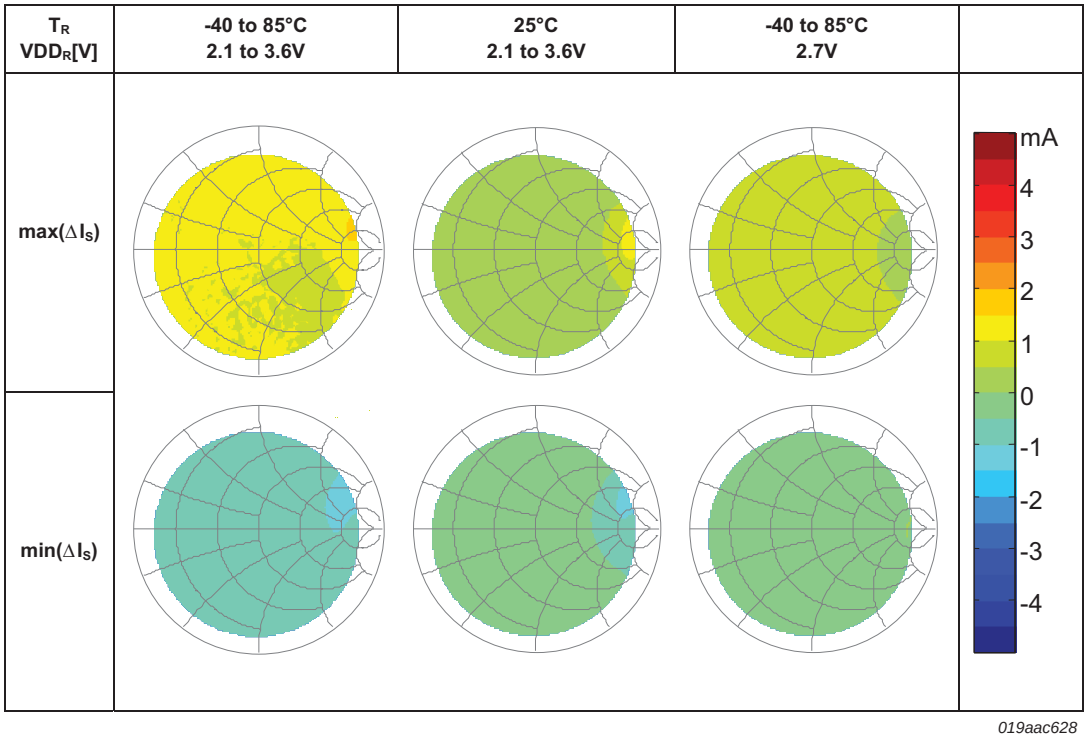

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 28. Supply current deviation at 434 MHz; power setup 1

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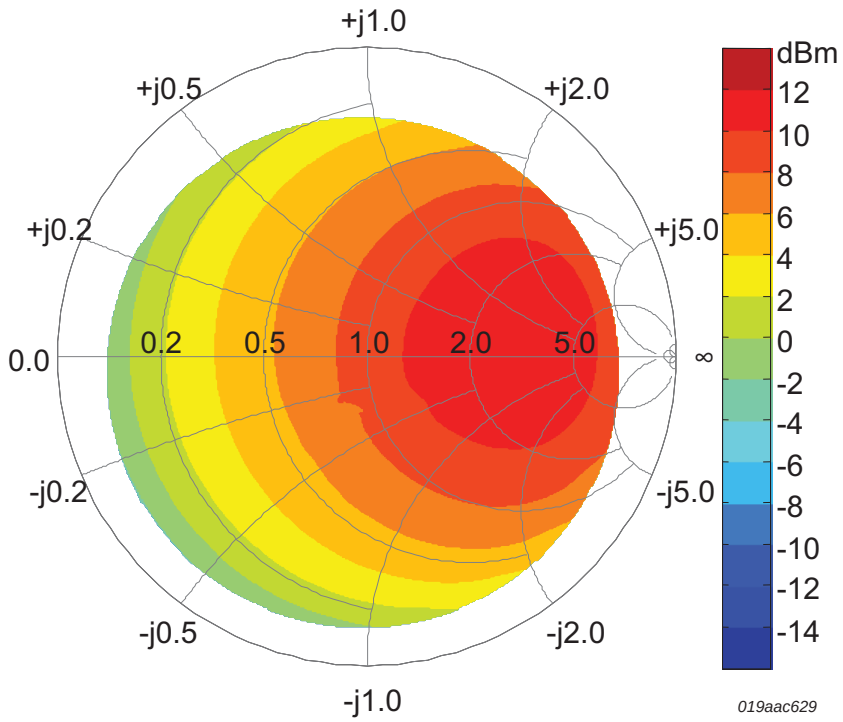
7.2.2 Power setup 2



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 29. Output power with applied impedance at 434 MHz; power setup 2

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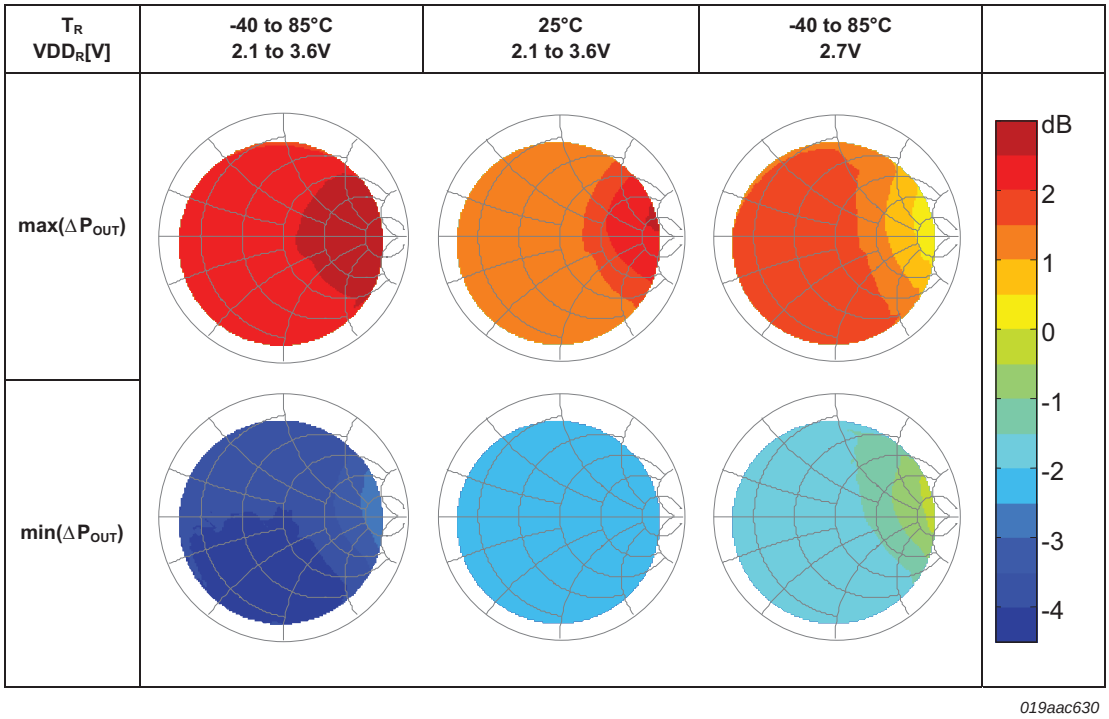

Output power deviation: $\Delta P_{OUT} = P_{OUT} (T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 30. Output power deviation at 434 MHz; power setup 2

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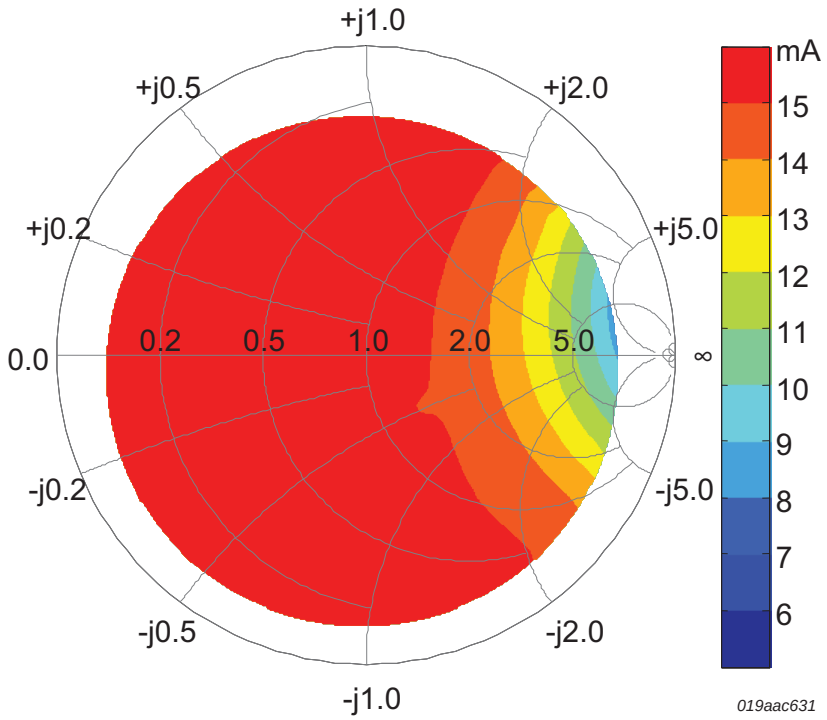

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 31. Supply current with applied impedance at 434 MHz; power setup 2

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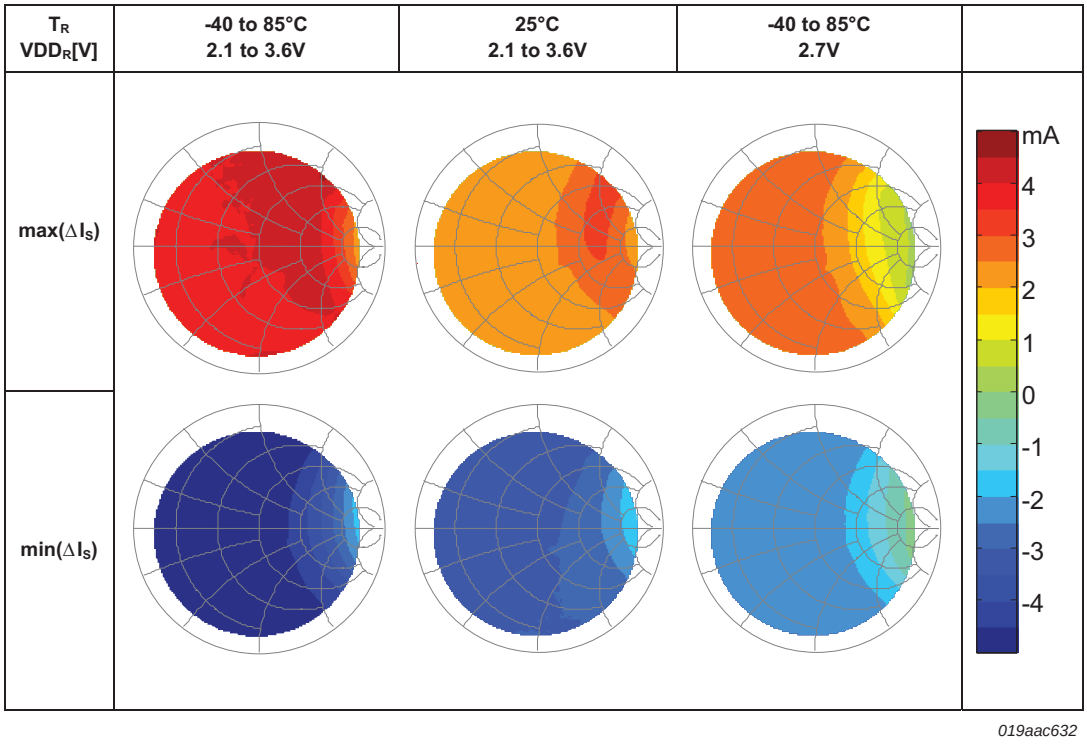

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 32. Supply current deviation at 434 MHz; power setup 2

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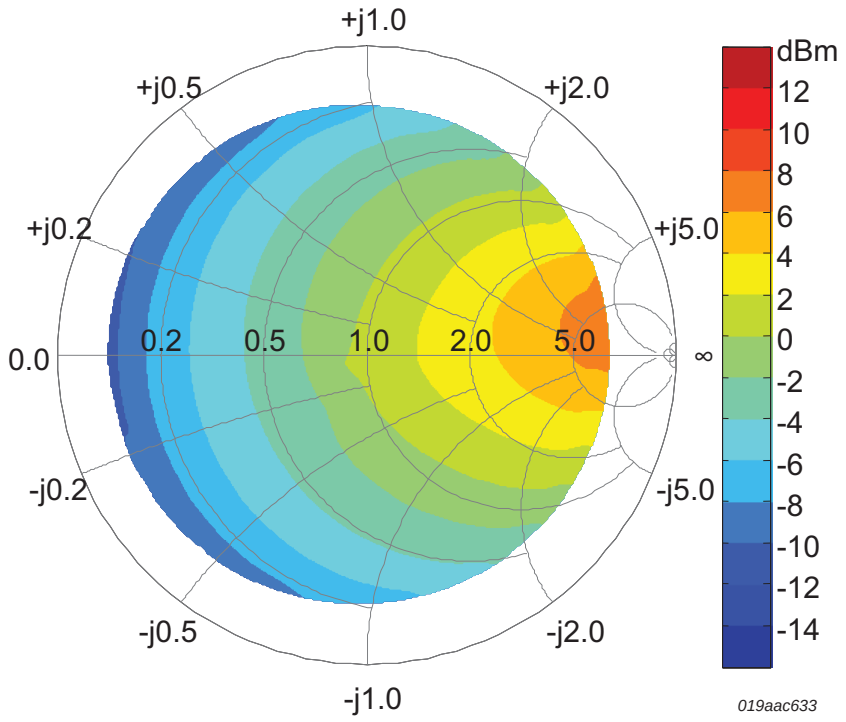
7.2.3 Optimum output impedance measured at 868 MHz

7.2.3.1 Power setup 1



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 33. Output power with applied impedance at 868 MHz; power setup 1

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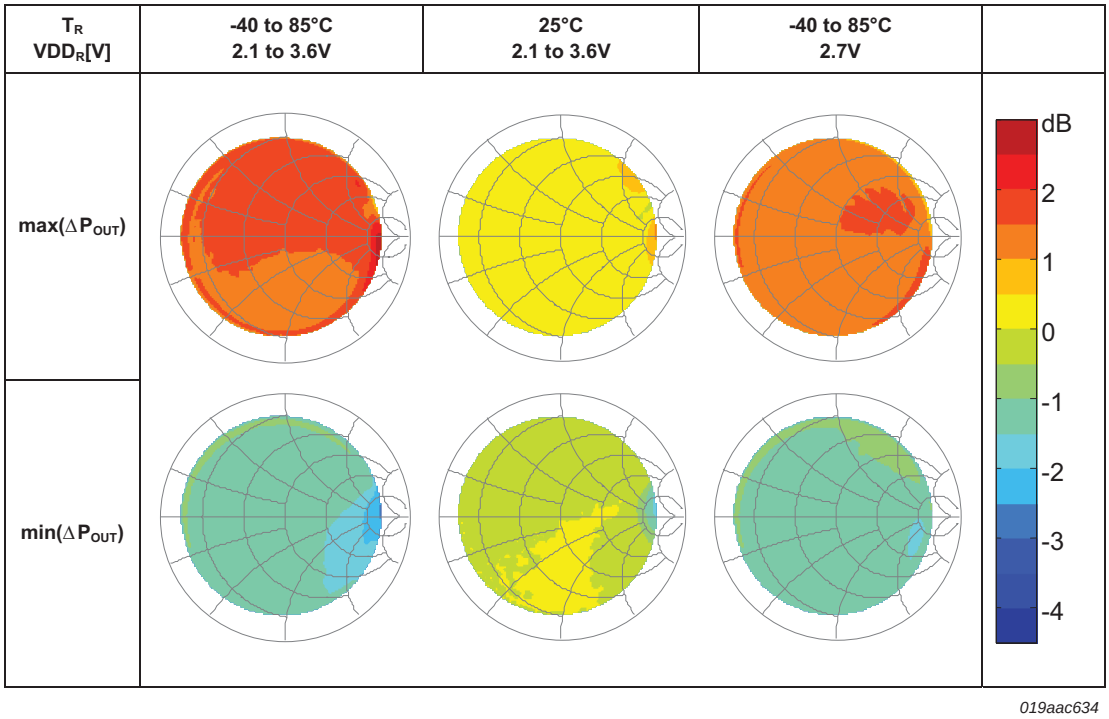

Output power deviation: $\Delta P_{OUT} = P_{OUT}(T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 34. Output power deviation at 868 MHz; power setup 1

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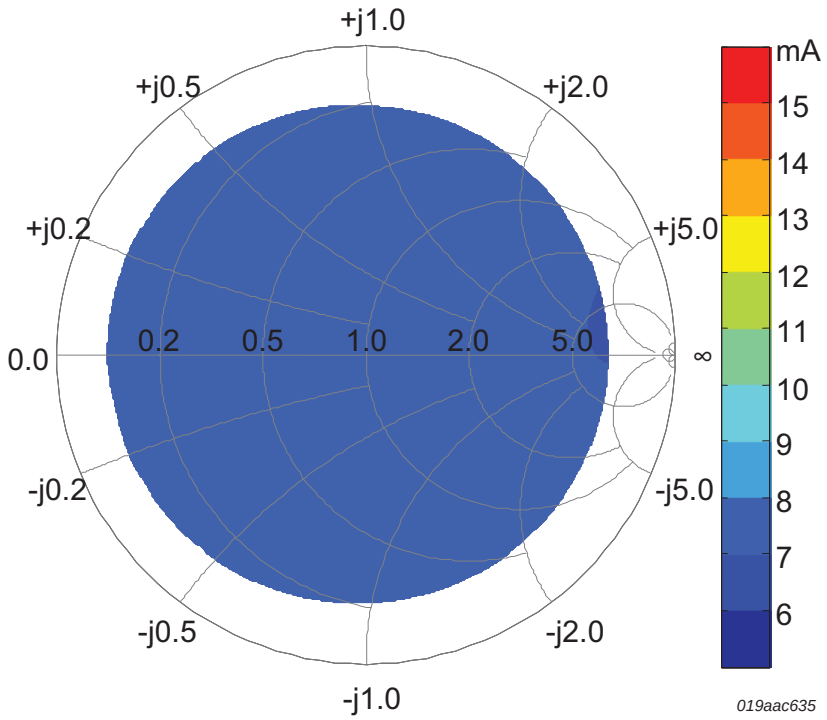

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 35. Supply current with applied impedance at 868 MHz; power setup 1

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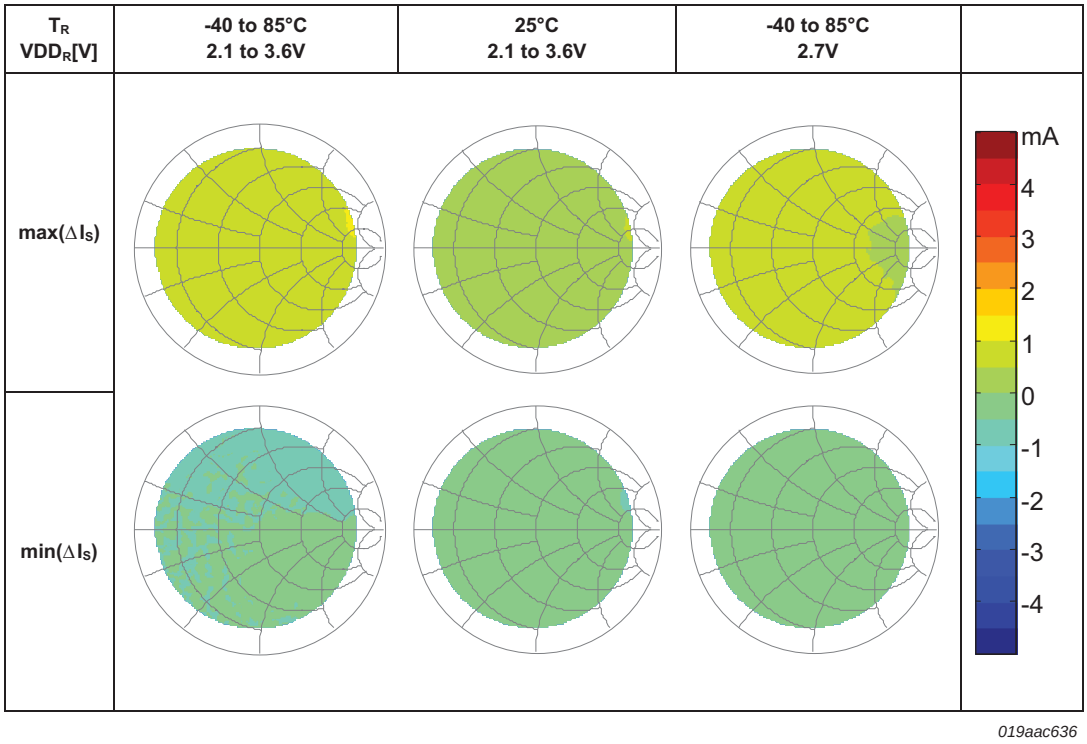

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 36. Supply current deviation at 868 MHz; power setup 1

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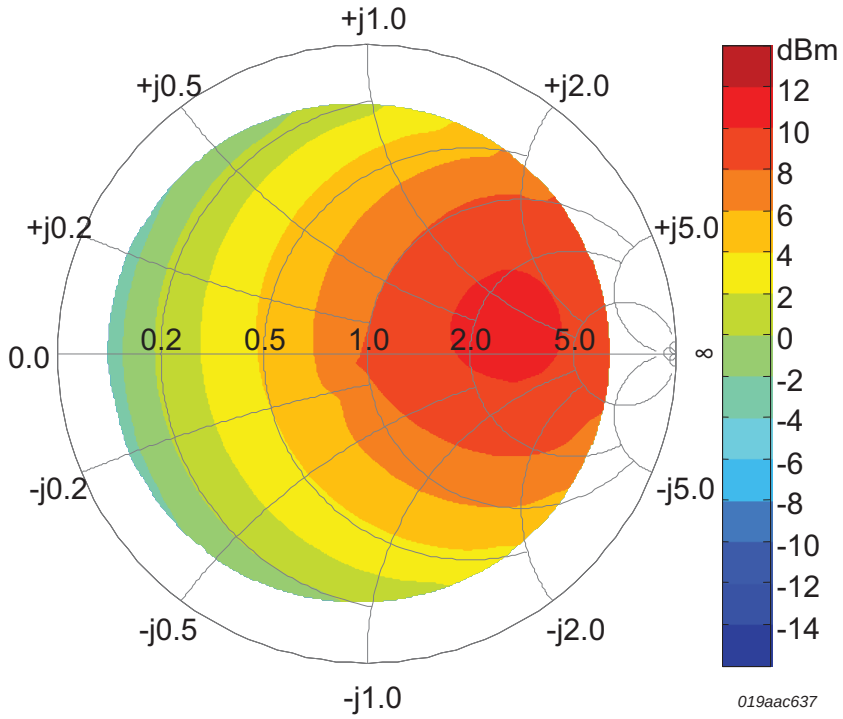
7.2.3.2 Power setup 2



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 37. Output power with applied impedance at 868 MHz; power setup 2

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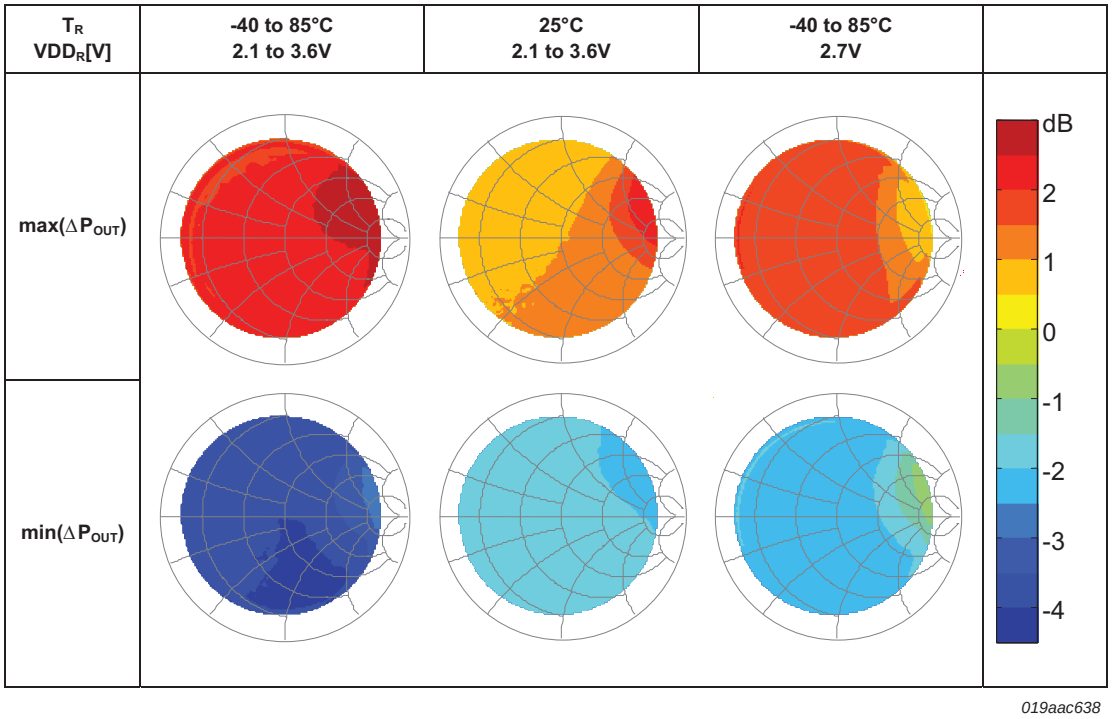

Output power deviation: $\Delta P_{OUT} = P_{OUT} (T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 38. Output power deviation at 868 MHz; power setup 2

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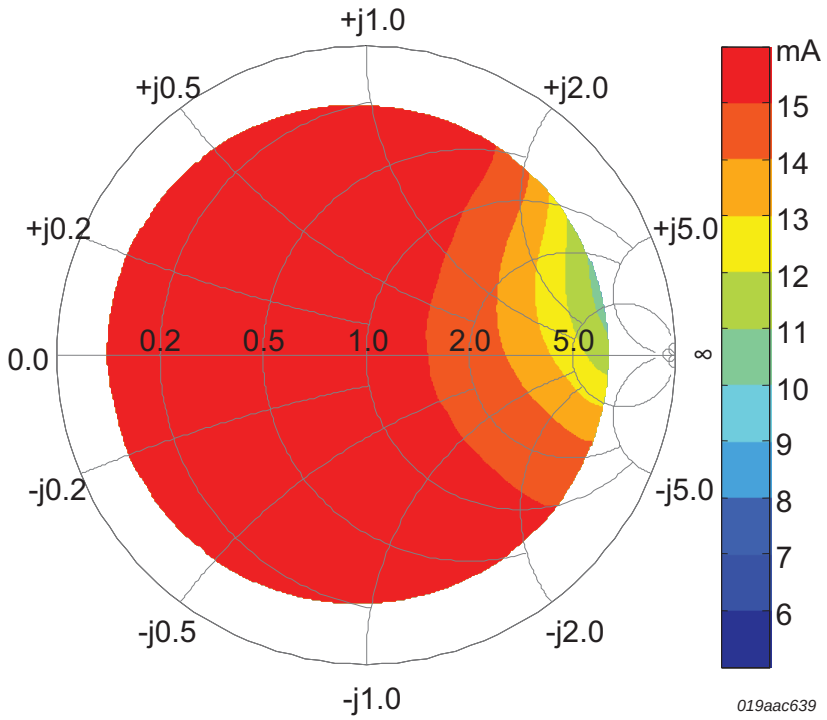

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 39. Supply current with applied impedance at 868 MHz; power setup 2

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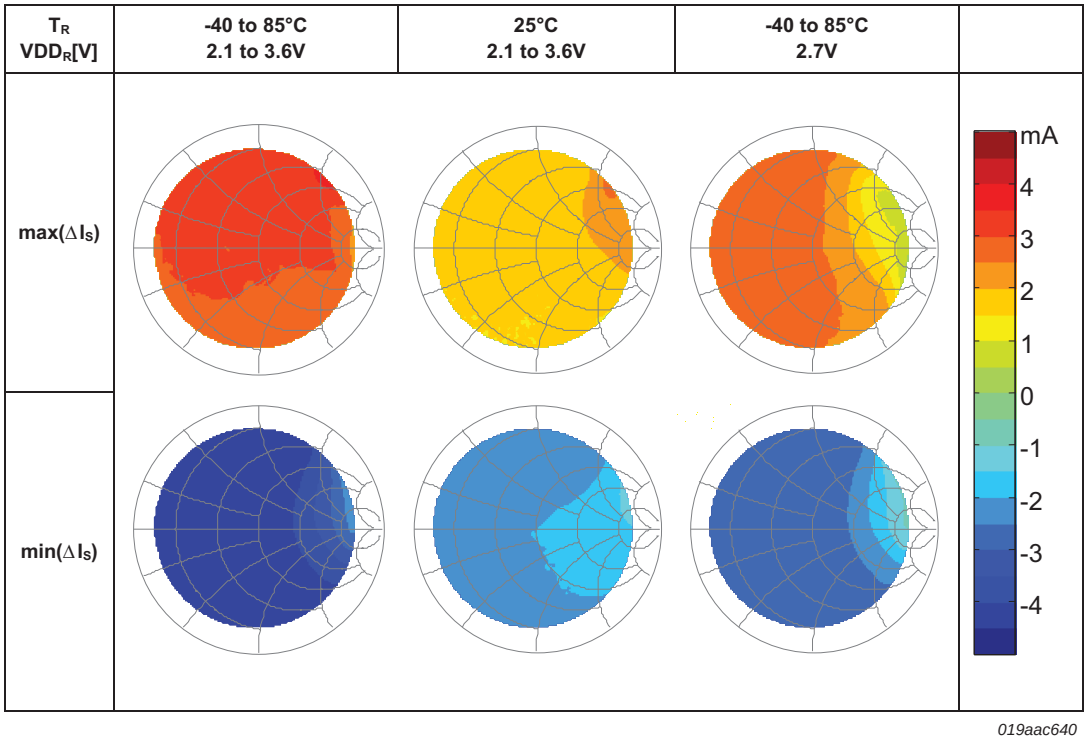

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 40. Supply current deviation at 868 MHz; power setup 2

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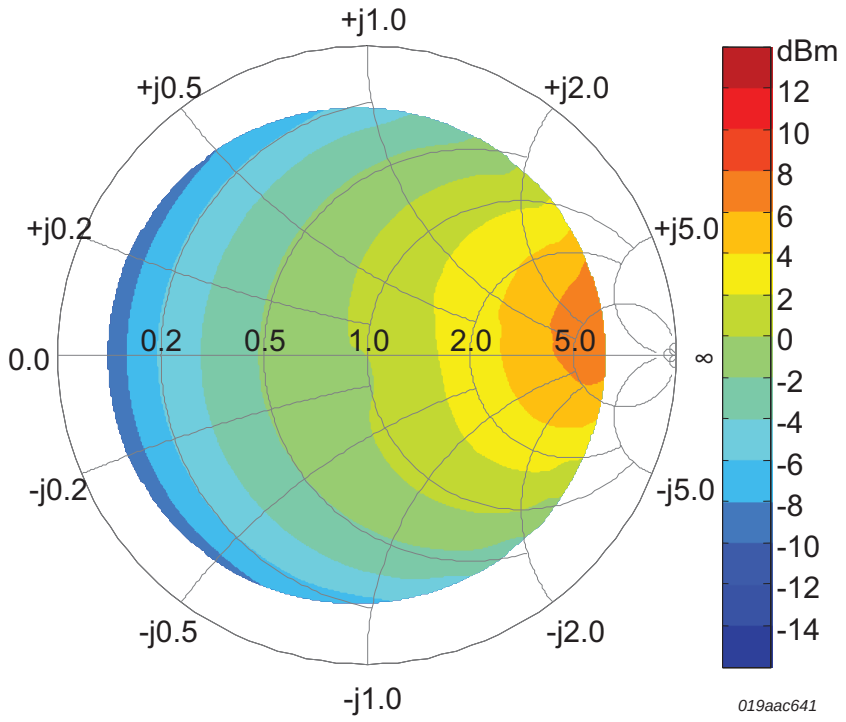
7.2.4 Optimum output impedance measured at 915 MHz

7.2.4.1 Power setup 1



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 41. Output power with applied impedance at 915 MHz; power setup 1

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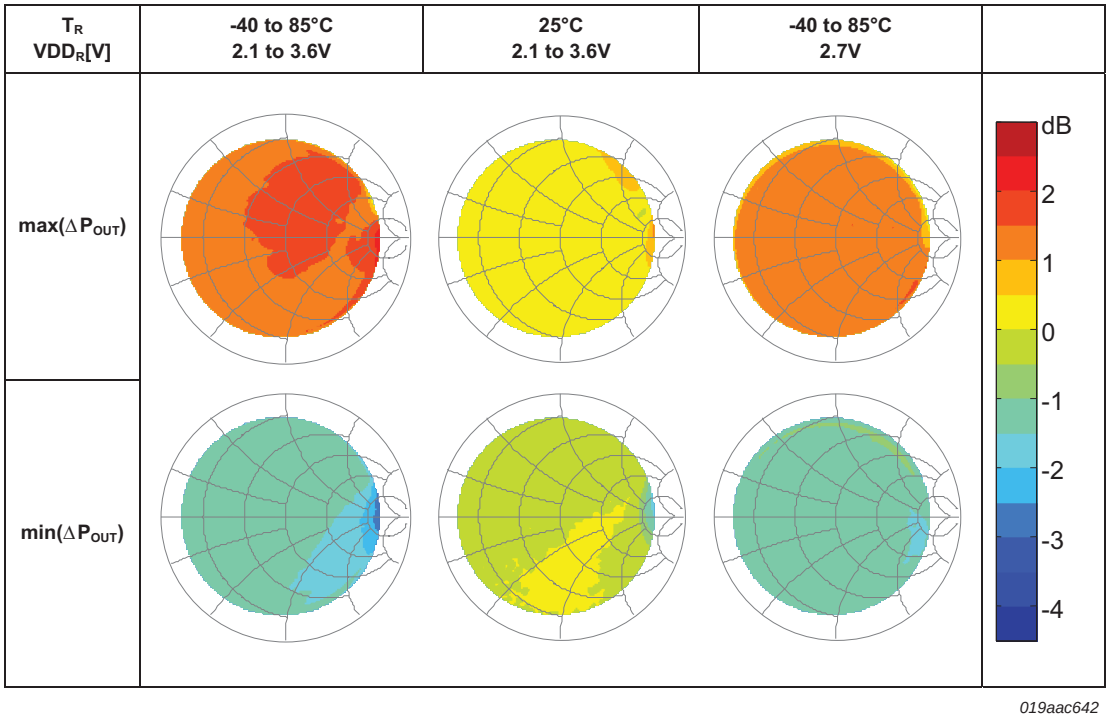

Output power deviation: $\Delta P_{OUT} = P_{OUT}(T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 42. Output power deviation at 915 MHz; power setup 1

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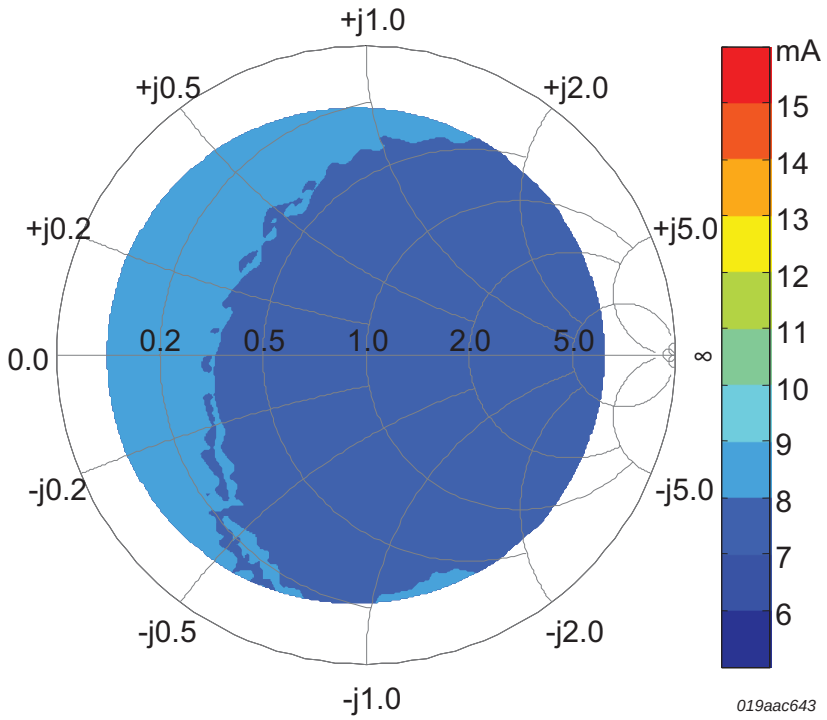

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 43. Supply current with applied impedance at 915 MHz; power setup 1

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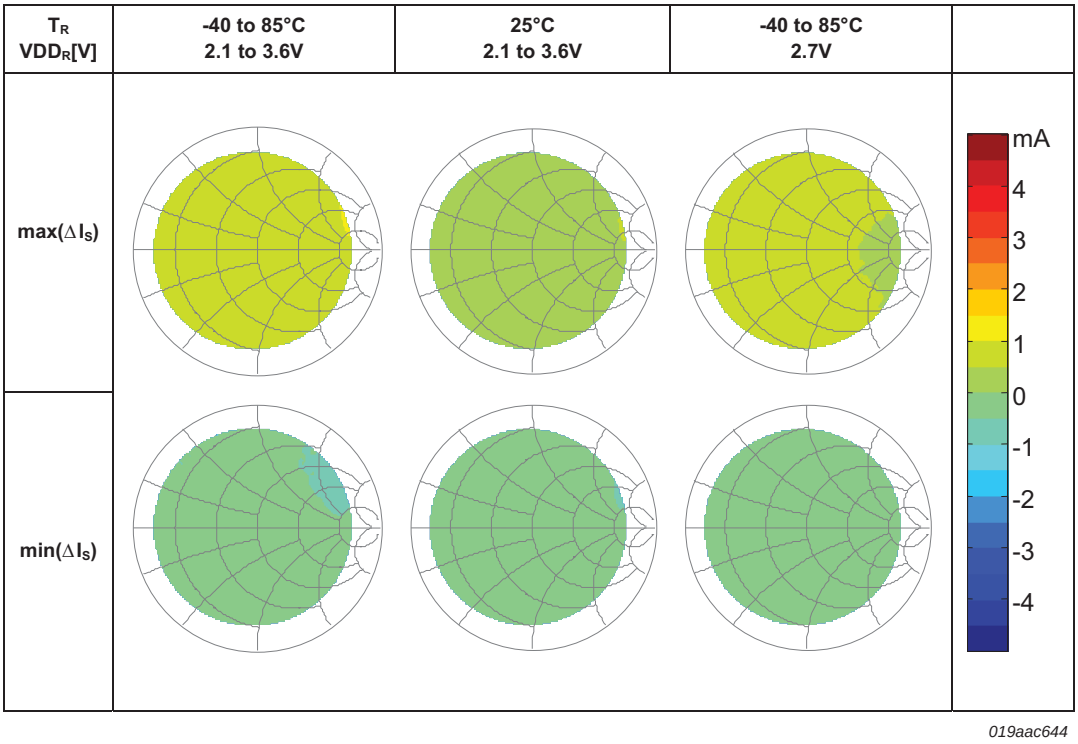

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 44. Supply current deviation at 915 MHz; power setup 1

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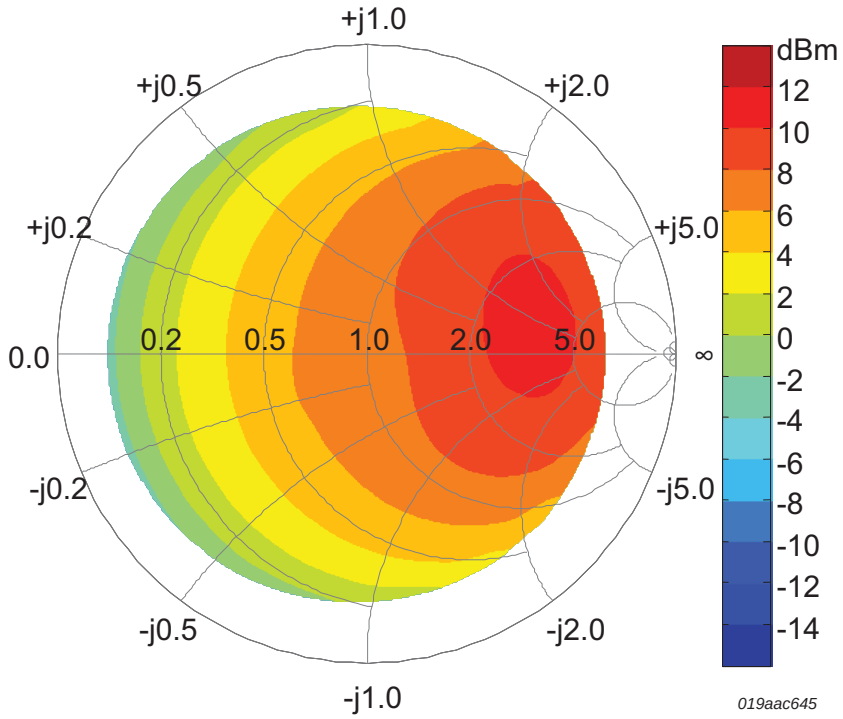
7.2.4.2 Power setup 2



$P_{OUT} = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 45. Output power with applied impedance at 915 MHz; power setup 2

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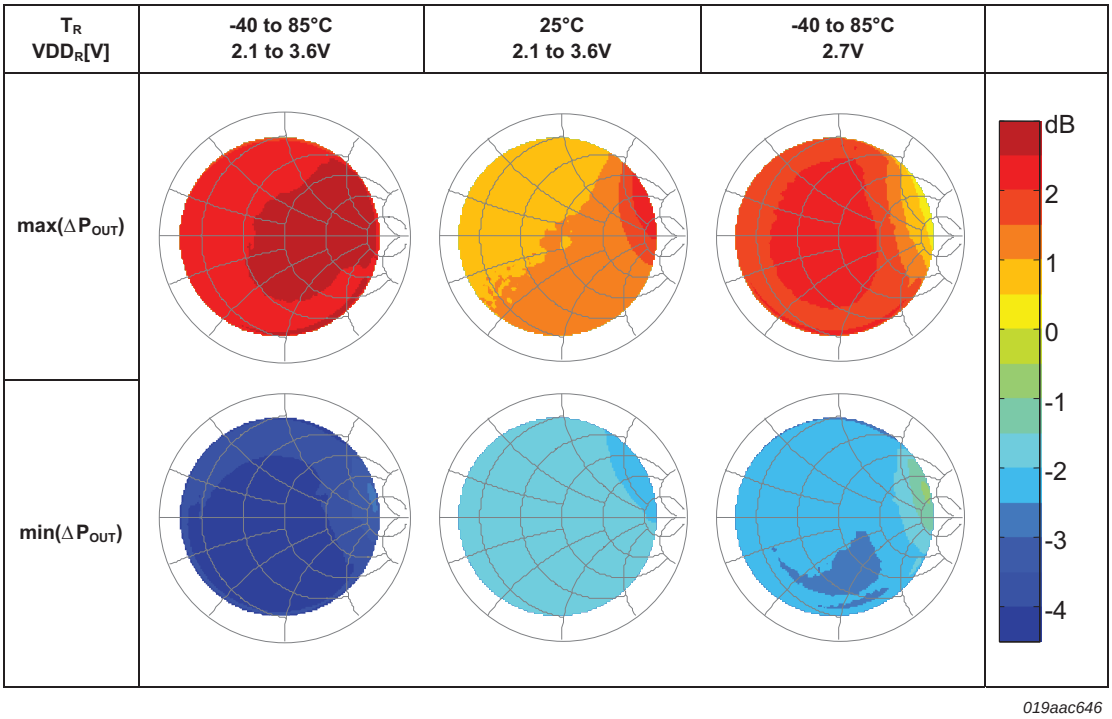

Output power deviation: $\Delta P_{OUT} = P_{OUT}(T_R, V_{DDR}) - P_{OUT}$ at 25 °C, 2.7 V.

Fig 46. Output power deviation at 915 MHz; power setup 2

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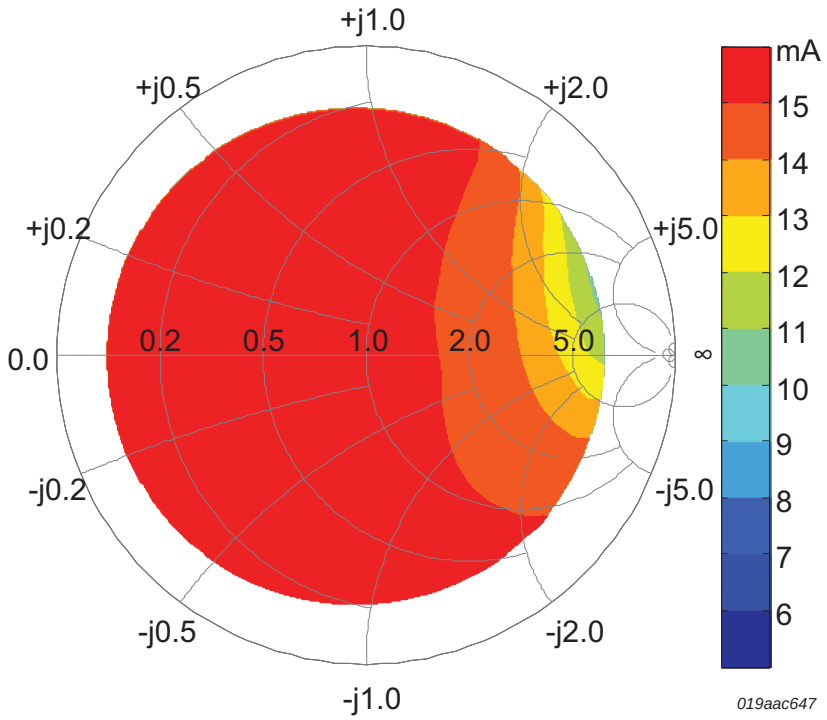

$I_S = f(Z_{OUT})$.

V_{DD} = 2.7 V, T = 25 °C.

Fig 47. Supply current with applied impedance at 915 MHz; power setup 2

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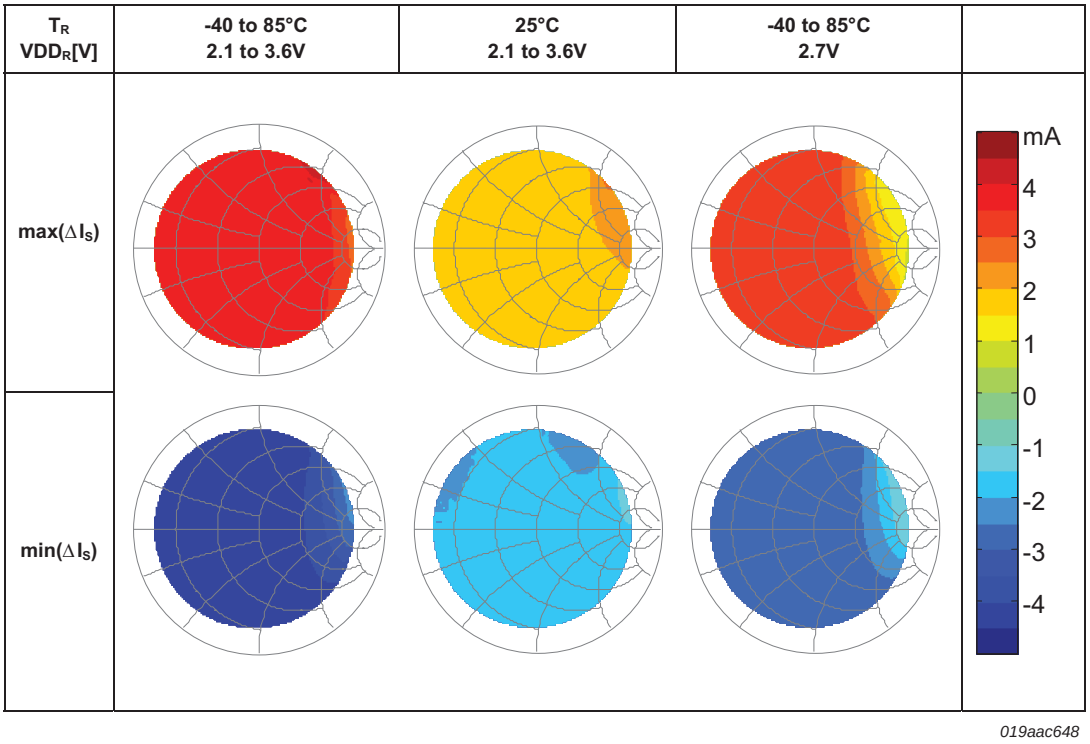

$\Delta I_S = I_S (T_R, V_{DDR}) - I_S$ at 25 °C, 2.7 V

Fig 48. Supply current deviation at 915 MHz; power setup 2

8. Abbreviations

Table 6. Abbreviations

Acronym	Description
FSK	Frequency-Shift Keying
LSB	Least Significant Bit
MSB	Most Significant Bit
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
VCO	Voltage-Controlled Oscillator

9. References

[1] OL2300 — Fractional-N PLL based transmitter data sheet

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