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PTN5110N VCONN protection programming guide

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Document information

Information	Content
Keywords	PTN5110N, TCPC, Type-C Port Controller, TCPM, USB PD PHY, Fast Role Swap
Abstract	PTN5110N is a 1-port TCPC (Type-C Port controller) compliant USB Power Delivery (PD) PHY IC that implements Type-C configuration channel interface and USB PD physical layer functions to a Type-C Port Manager (TCPM) that handles PD Policy management. The device can be used in the following applications: PC platforms (Notebook PCs, Desktop PCs, Ultra-books, Chromebooks), Tablets, 2:1 Convertibles, Smartphones and Portable devices, and PC accessories/peripherals (Docking, Mobile Monitors, Multi-Function Monitors, Portable/External hard drives, Cable adapters, Dongles and accessories, etc.)

Revision history

Rev	Date	Description
v.1.0	20180709	Initial version

1 Introduction

PTN5110N is a 1-port TCPC (Type-C Port controller) compliant USB Power Delivery (PD) PHY IC that implements Type-C configuration channel interface and USB PD physical layer functions to a Type-C Port Manager (TCPM) handling PD Policy management. It complies with USB PD[1], Type-C[2] and TCPC[3] specifications and relevant ECNs/ECRs. This IC is targeted primarily for use in system platforms (e.g. Notebook PCs, Desktop PCs, Chromebooks, Tablets, Convertibles, etc.). Other use cases may be feasible depending on the application architecture - e.g. Docks, Monitors, Accessories, Cable adapters, Smartphones etc.

It can support Type-C roles: sink, source, sink with accessory support, or DRP. It implements Type-C CC analog portion (i.e Rd/Rp/Ra detection, Rd/Rp indication) and PD Tx/Rx PHY and protocol state machines as per [3]. PTN5110N supports TCPM in system realization of the following PD roles: (i) Provider (P), (ii) Provider/Consumer (P/C) (iii) Consumer (C) (iv) Consumer/Provider (C/P).

The PTN5110N internal registers consist of the standard USB Type-C Port Interface Specification register map, as well as NXP defined register map. The standard USB Type-C Port Interface Specification register map is from 0x00 to 0x7F, and the NXP defined register map is from 0x80 to 0x9F.

NXP defined its own registers to support vendor defined features such programmable GPIO pins, VCONN current limit, VCONN protection and fault report. This application note describes the procedures to enable VCONN protection features (over current limit, short circuit protection, over temperature fault, and reverse current protection), and interrupt handling of VCONN fault.

2 VCONN protection registers

There are number of registers that must be setup to enable VCONN protection. A VCONN overcurrent fault is handled by the standard TCPC register FAULT_CONTROL; NXP expanded this further to include reverse current, short circuit and over temperature faults as well as automatic open and close of VCONN switch.

The registers to enable and to handle VCONN faults are listed below:

Table 1. VCONN fault registers

Register	Address	Description
FAULT_STATUS_MASK	0x15	Allows TCPM to mask fault event
FAULT_CONTROL	0x1B	Allows TCPM to enable/disable fault circuitry. Set the bit to '0' to enable and to '1' to disable.
FAULT_STATUS	0x1F	TCPM reads this register upon receiving a fault alert. TCPC reports the source of the fault in this register.
EXT_FAULT_CONFIG	0x88	Allows TCPM to enable OCL, OTF or RCP
EXT_STATUS	0x90	TCPC reports the source of VCONN fault in this register
VCONN_CONFIG	0x9C	Allow TCPM to enable automatic open/self-close of VCONN switch upon overcurrent fault.
VCONN_FAULT_DEBOUNCE	0x9D	Programmable RCP debounce time before a RCP event is considered valid.
VCONN_FAULT_RECOVERY	0x9E	Programmable OTF and RCP events fault recovery time – the amount of the time VCONN switch is open before it can be closed again.
VCONN_FAULT_ATTEMPTS	0x9F	Programmable number of attempts TCPC will try to close VCONN switch before giving up and alerting the TCPM.

3 VCONN protection features

In case of a catastrophic event on VCONN pin, PTN5110N offers a couple of ways to protect the VCONN switch as well as the device itself.

1. Over Current Limit (OCL) – when there is an over current fault or a short on VCONN, PTN5110N will limit current supplies by VCONN switch to the programmable limit threshold (VCONN_CONFIG).
2. Short Circuit Protection (SCP) – same as OCL.
3. Over Temperature Protection (OTP or OTF) – over temperature threshold factory programmed set to 137°C +/- 14°C (123°C min and 152°C max).
4. Reverse Current Protection (RCP) – PTN5110N monitors the reverse voltage across the VCONN switch for reverse current that flows into the VCONN pin. The reverse voltage is 55mV typical (100mV max).

4 VCONN fault interrupt

VCONN fault circuit detection can be enabled with FAULT_CONTROL.VconnOverCurrentFault bit. Once the detection circuit is enabled (VconnOverCurrentFault = 0), PTN5110N will interrupt TCPM if FAULT_STATUS_MASK.VconnOverCurrentFault is not masked, and a VCONN fault has occurred and debounced.

Upon receiving an interrupt TCPM should read the ALERT register. If ALERT.Fault bit is set, TCPM must read FAULT_STATUS register to find the source of the fault. A VCONN fault will cause FAULT_STATUS.VconnOverCurrentFault bit to be set. Further information about the VCONN fault can be determined by reading EXT_STATUS register. This register would indicate whether the fault is caused by over current, over temperature, short circuit or reverse current on VCONN pin.

5 VCONN protection programming

Individual VCONN protection fault can be enabled/disabled separately through EXT_FAULT_CONFIG register. See Section 10 for more details.

6 VCONN over current fault

6.1 Programming

1. Enable VCONN fault interrupt with FAULT_STATUS_MASK.VconnOverCurrentFault bit set to ‘1’.
2. Enable VCONN fault detection with FAULT_CONTROL.VconnOverCurrentFault bit set to ‘0’.
3. Enable VCONN over current limit with EXT_FAULT_CONFIG.VCONNOverCurrentLimitEnable bit set to ‘1’.
4. Optionally VCONN switch can be programmed to keep sourcing with the current limited or to open upon a VCONN over current fault. The default setting is not to open the VCONN switch. VCONN_CONGIG.VCONN_OCL_SwitchOpenEnable when set to ‘1’ will open up VCONN switch, otherwise, VCONN current will be clamped to a limit threshold.
   When OCL fault is programmed not to open the switch, PTN5110N will limit the current but will not generate an OCL interrupt when OCL fault occurs. When OCL fault is programmed to open the switch, PTN5110 will open the switch and generate an OCL interrupt when OCL fault occurs. TCPM then must take appropriate actions to close VCONN switch (such as inform the user to remove the dongle and re-insert the dongle).
5. Program VCONN OCL threshold with VCONN_CONFIG.VCONN_OCL_Threshold. The selectable values are 135mA, 300mA, 450mA and 600mA.

6.2 Handling

Once an over current fault has occurred and VCONN switch is programmed to open, TCPM will get an interrupt from PTN5110N. TCPM can follow the steps below to handle the fault.

1. Read ALERT register, and ALERT.Fault bit is set.
2. Read FAULT_STATUS register, and FAULT_STATUS.VCONNOverCurrentFault bit is set.
3. Read EXT_STATUS register, and EXT_STATUS.VCONNOverCurrentFaultStatus bit is set.
4. Clear fault status by writing a ‘1’ to FAULT_STATUS.VCONNOverCurrentFault.
5. Clear over current fault interrupt by setting ALERT.Fault to ‘1’.
6. TCPM must set POWER_CONTROL.EnableVCONN to enable VCONN again.

7 VCONN short circuit fault

The same programming sequence for OCL can be used to enable VCONN short current protection (SCP). When PTN5110N detects a short on VCONN, PTN5110N generates a fault interrupt and opens VCONN switch to cut off VCONN current. EXT_STATUS.VCONNShortCircuitFaultStatus bit is set to ‘1’, and TCPM can clear SCP fault by writing a ‘1’ to FAULT_STATUS.VCONNOverCurrentFault and ALERT.Fault.

TCPM must then re-enable VCONN through POWER_CONTROL.EnableVCONN bit. If the short on VCONN has not been removed, PTN5110N regenerates SCP fault.

A short on VCONN might damage the system if not handled properly. It is suggested that the system software inform the user of the power issue with the Type-C port, and advise the user to remove the dongle from the port.

Optionally, PTN5110N can be programmed to self-clear SCP fault with VCONN_CONFIG.VCONNSelfClearSCP set to ‘1’. When this bit is set, PTN5110N examines VCONN to figure out if the short has been removed after every fault recovery time. If the short is removed, then PTN5110N closes the VCONN switch without TCPM involvement.

8 Over temperature fault

8.1 Programming

1. Enable VCONN fault interrupt with FAULT_STATUS_MASK.VconnOverCurrentFault bit set to ‘1’.
2. Enable VCONN fault detection with FAULT_CONTROL.VconnOverCurrentFault bit set to ‘0’.
3. Enable VCONN over current limit with EXT_FAULT_CONFIG.VCONNOverCurrentTempFaultEnable bit set to ‘1’.
4. Once the temperature fault occurs, PTN5110N opens the VCONN switch but optionally PTN5110N can be programmed to re-close the switch when the temperature fault is no longer present. The VCONN_FAULT_RECOVERY[7:4] register specifies the time the switch is open before it can be closed again. The VCONN_FAULT_ATTEMPS[7:4] register specifies the number of attempts PTN5110N tries to reclose the switch before giving up (due to continuous presence of OTF), and generates an interrupt to TCPM.

8.2 Handling

Once a temperature fault has occurred, PTN5110N opens the switch. TCPM can follow the steps below to handle the fault.

1. Read ALERT register, and ALERT.Fault bit is set.
2. Read FAULT_STATUS register, and FAULT_STATUS.VCONNOverCurrentFault bit is set.
3. Read EXT_STATUS register, and EXT_STATUS.VCONNOverTempFaultStatus bit is set.
4. Clear fault status by writing a ‘1’ to FAULT_STATUS.VCONNOverCurrentFault.
5. Clear over current fault interrupt by setting ALERT.Fault to ‘1’.
6. TCPM must set POWER_CONTROL.EnableVCONN to enable VCONN again if VCONN_CONFIG.VCONNSelfClearTemp bit is set to ‘0’, or if temperature fault is still present after a number of attempts by PTN5110N to close the VCONN switch has failed.

9 VCONN reverse current fault

9.1 Programming

1. Enable VCONN fault interrupt with FAULT_STATUS_MASK.VconnOverCurrentFault bit set to ‘1’.
2. Enable VCONN fault detection with FAULT_CONTROL.VconnOverCurrentFault bit set to ‘0’.
3. Enable VCONN reverse current protection with EXT_FAULT_CONFIG.VCONNReverseCurrentFaultEnable bit set to ‘1’.
4. When a reverse current fault occurs, PTN5110N opens the VCONN switch but optionally PTN5110N can be programmed to re-close the switch when the reverse current fault is no longer present. The VCONN_FAULT_RECOVERY[3:0] register specifies the time the switch is open before it can be closed again. The VCONN_FAULT_ATTEMPS[3:0] register specifies the number of attempts PTN5110N tries to reclose the switch before giving up (due to the continuous presence of RCP), and generates an interrupt to TCPM.

9.2 Handling

When a reverse current fault occurs, PTN5110N opens the switch. TCPM can follow the steps below to handle the fault.

1. Read ALERT register, and ALERT.Fault bit is set.
2. Read FAULT_STATUS register, and FAULT_STATUS.VCONNOverCurrentFault bit is set.
3. Read EXT_STATUS register, and EXT_STATUS.VCONNReverseCurrentFaultStatus bit is set.
4. Clear fault status by writing a ‘1’ to FAULT_STATUS.VCONNOverCurrentFault.
5. Clear over current fault interrupt by setting ALERT.Fault to ‘1’.
6. If PTN5110N is programmed to self close the VCONN switch, it automatically closes the VCONN switch if RCP fault goes away within the number of attempts in the VCONN_FAULT_ATTEMPS register. Otherwise, PTN5110N generates an RCP interrupt to TCPM and TCPM must try to reclose the VCONN switch through POWER_CONTROL register. Please note that the RCP fault might be permanent and the user would have to remove the device to resolve the RCP issue.

10 Register listing and description

Table 2. Register listing and description

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
00h	VENDOR_ID	Read Only Word	0x1FC9	15:0	Vendor ID A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.	Required	Supported
02h	PRODUCT_ID	Read Only Word	0x5110	15:0	USB Product ID A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.		
04h	DEVICE_ID	Read Only Word	0x0004	15:0	bcdDevice A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.		
06h	USBTYPEC_REV	Read Only Word	0x0012	15:8	Reserved		
				7:0	USB Type-C Revision Version number assigned by USB-IF 0001 0001b : Type-C Revision 1.1 0001 0010b : Type-C Revision 1.2		
08h	USBPD_REV_VER	Read Only Word	0x3011	15:8	bcdUSBPD Revision 0010 0000b : USBPD Revision 2.0 0011 0000b : USBPD Revision 3.0		
				7:0	bcdUSBPD Version 0001 0000b : USBPD Version 1.0 0001 0001b : USBPD Version 1.1 Etc.		
0Ah	PD_INTERFACE_REV	Read Only Word	0x2010	15:8	bcd USB-PD Inter-Block Specification Revision 0001 0000 : TCPC Revision 1.0 0010 0000 : TCPC Revision 2.0 (this release)		
				7:0	bcd USB-PD Inter-Block Specification Version 0001 0000 : TCPC Version 1.0 0001 0001 : TCPC Version 1.1 0001 0010 : TCPC Version 1.2 Etc.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
0Ch-0Fh	Reserved	N/A	0x0000	N/A	Reserved		
10h	ALERT	Read / Write Word	0x0000	15	Vendor Defined Extended 0b: No vendor defined alert occurred 1b: Read EXT_ALERT to determine the source of the vendor defined alert. Writing 1 to this bit will clear only this bit, EXT_ALERT must also be cleared to de-assert ALERT_N.	Required	Supported
				14	Alert Extended 0b: Cleared 1b: An extended interrupt event has occurred. Read the ALERT_EXTENDED register.		
				13	Extended Status 0b: Cleared, 1b: Extended Status changed		
				12	Beginning SOP* Message Status READABLE_BYTE_COUNT is 133; this is just the beginning of an extended USB PD message with more than 128 data bytes. This bit is not set if READABLE_BYTE_COUNT is less than 133. 0b: Cleared, 1b: RECEIVE_BUFFER register changed. READABLE_BYTE_COUNT being set to 0 does not set this bit.		
				11	VBUS Sink Disconnect Detected 0b: Cleared 1b: Detected This bit shall only be asserted when POWER_CONTROL.AutoDischargeDisconnect is set		
				10	Rx Buffer Overflow 0b: TCPC Rx buffer is functioning properly 1b: TCPC Rx buffer has overflowed Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.ReceiveSOP*MessageStatus		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				9	Fault 0b: No Fault 1b: Fault Occurred. Read the FAULT_STATUS register		
				8	VBUS Voltage Alarm Lo 0b: Cleared 1b: Occured. A low-voltage alarm has occurred		
				7	VBUS Voltage Alarm Hi 0b: Cleared 1b: Occured. A high-voltage alarm has occurred		
				6	Transmit SOP* Message successful 0b: Cleared, 1b: Successful. Reset or message transmitted. Transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.		
				5	Transmit SOP* Message discarded 0b: Cleared, 1b: Discarded. Reset or SOP* message transmission not sent due to incoming receive message. Transmit SOP* message buffer registers is not full.		
				4	Transmit SOP* Message failed 0b: Cleared, 1b: Message transmission failed. no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers is not full.		
				3	Received Hard Reset 0b: Cleared, 1b: Received Hard Reset message		
				2	Received SOP* Message Status 0b: Cleared, 1b: Receive status register changed READABLE_BYTE_COUNT being set to 0 does not set this bit.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				1	Port Power Status 0b: Cleared 1b: Port status changed		
				0	CC Status Alert 0b: Cleared 1b: CC status changed Note: _Alert suffix added to differentiate from CC_Status register clearly in code generation TCPC shall not assert this bit when CC_STATUS.Looking4Connection changes state if TCPC_CONTROL.EnableLooking4ConnectionAlert is set to 0.		
12h	ALERT_MASK	Read / Write Word	0x7FFF	15	Vendor Defined Extended Masked 0b: Interrupt masked (EXT_ALERT_MASK must also be 0 to completely unmask all vendor defined alerts) 1b: Interrupt unmasked	Required	Supported
				14	Alert Extended Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				13	Extended Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				12	Beginning SOP* Message Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				11	VBUS Sink Disconnect Detected Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				10	Rx Buffer Overflow Masked 0b: Interrupt masked 1b: Interrupt unmasked		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				9	Fault Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				8	VBUS Voltage Alarm Lo Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				7	VBUS Voltage Alarm Hi Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				6	Transmit SOP* Message successful Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				5	Transmit SOP* Message discarded Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				4	Transmit SOP* Message failed Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				3	Received Hard Reset Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked (The Hard Reset should generally not be masked)		
				2	Receive SOP* Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				1	Port Power Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				0	Cc Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
14h	POWER_STATUS_MASK	Read / Write Byte	0xFF	7	Debug Accessory Connected Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked	Required	Supported
				6	TCPC Initialization Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				5	Source High Voltage Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				4	Source VBUS Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				3	VBUS Present Detection Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				2	VBUS Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				1	VCONN Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				0	Sink VBUS Connected Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
15h	FAULT_STATUS_MASK	Read / Write Byte	0xFF	7	All Registers Reset To Default Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked The condition that generates a FAULT_STATUS.AllRegistersResetToDefault Interrupt also resets this bit; therefore, writing a 0b to this bit will not mask FAULT_STATUS.AllRegistersResetToDefault Interrupt	Required	Supported
				6	Force Off VBUS Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				5	Auto Discharge Failed Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				4	Force Discharge Failed Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				3	VBUS Over Current Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				2	VBUS Over Voltage Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				1	VCONN Over Current Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				0	I2C Interface Error Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
16h	EXTENDED_STATUS_MASK	Read / Write Byte	0xFF	7:1	Reserved Shall be set to zero by sender and ignored by receiver	Register Required	

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				0	vSafe0V Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
17h	ALERT_EXTENDED_MASK	Read/ Write Byte	0xFF	7:3	Reserved Shall be set to zero by sender and ignored by receiver	Register Required	
				2	Timer Expired Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
				1	Source Fast Role Swap Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
				0	Sink Fast Role Swap Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
18h	CONFIGURE_STANDARD_OUTPUT	Read/ Write Byte	0x60	7	High Impedance outputs 0b: Standard output control 1b: Force all outputs to High Impedance May be used to save power in Sleep Controlled by the TCPM.	Optional Normative	Supported
				6	Debug Accessory Connected# 0b: Debug Accessory Connected# output is driven low 1b: Debug Accessory Connected# output is driven high If TCPC_CONTROL.DebugAccessoryControl = 0, the TCPC shall write to this register and ignore inputs from TCPM If TCPC_CONTROL.DebugAccessoryControl = 1, the TCPC shall take input from the TCPM		Supported
				5	Audio Accessory Connected 0b: Audio Accessory connected 1b: No Audio Accessory connected (default) Controlled by the TCPM		Not supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				4	Active Cable Connected 0b: No Active Cable connected 1b: Active Cable connected Controlled by the TCPM		
				3:2	MUX Control 00b: No connection. 01b: USB3.1 Connected 10b: DP Alternate Mode : 4 lanes 11b: USB3.1 + Display Port Lanes 0 & 1 Controlled by the TCPM		
				1	Connection Present 0b: No Connection 1b: Connection Controlled by the TCPM		
				0	Connector Orientation GPIO0 0b: Normal (CC1=A5, CC2=B5, TX1=A2/A3, RX1=B10/B11) default 1b: Flipped (CC2=A5, CC1=B5, TX1=B2/B3, RX1=A10/A11) If TCPC_CONTROL.DebugAccessoryControl = 0, the TCPC shall write to this register and ignore inputs from TCPM If TCPC_CONTROL.DebugAccessoryControl = 1, the TCPC shall take input from the TCPM		Supported
19h	TCPC_CONTROL	Read / Write Byte	0x00	7	Enable SMBus PEC 0b: SMBus PEC is disabled (default) 1b: SMBus PEC is enabled Enables SMBus PEC according to TCPC Spec.	Register Required	Not supported
				6	Enable Looking4Connection Alert 0b: Disable ALERT.CcStatus assertion when CC_STATUS.Looking4Connection changes (default) 1b: Enable ALERT.CcStatus assertion when CC_STATUS.Looking4Connection changes		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				5	Enable Watchdog Timer 0b: Watchdog Monitoring is disabled (default) 1b: Watchdog Monitoring is enabled Enables Watchdog Timer Monitoring according to TCPC Spec Required if DEVICE_CAPABILITIES_2.Watch Dog Timer = 1b		Supported
				4	Debug Accessory Control 0b: Controlled by TCPC (power on default) 1b: Controlled by TCPM. The TCPM writes 1b to this register to take over control of asserting the DebugAccessoryConnected#. Required (Register is required but output is not required)		Supported
				3:2	I2C Clock Stretching Control Clock Stretching Control 00b: Disable clock stretching. TCPC shall not perform any clock stretching during I2C transfers. 01b: Reserved 10b: Enable clock stretching. TCPC is allowed limited clock stretching during each I2C Transfer. 11b: Enable clock stretching only if the Alert pin is not asserted. As soon as Alert is asserted, clock stretching is disabled by the TCPC. The TCPC datasheet should contain details as to the power consequences of clock stretching as well as the max duration of clock stretching per I2C transaction. This is only necessary if clock stretching is implemented. The TCPC shall limit total clock stretching as detailed in TCPC Spec I2C Physical Interface Specifications. This feature is optional. The TCPC is allowed to ignore updates to this bit field if it has not implemented clock stretching. The power on default value is such to disable clock stretching.		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				1	BIST Test Mode Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the TCPC. The TCPM should clear this bit when a detach is detected. 0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert. The TCPM can mask or ignore received message alerts when this bit is set to 1 since the TCPC may or may not assert the alert. The TCPM may also treat received messages in this mode in the same way as received messages during normal operation.		Supported
				0	Plug Orientation 0b: When Vconn is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When Vconn is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. Required		Supported
1Ah	ROLE_CONTROL	Read / Write Byte	Set according to MTP	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				6	DRP 0b: No DRP. Bits B3..0 determine Rp/Rd/Ra or open settings 1b: DRP The TCPC shall use the Rp value defined in B5..4 when a connection is resolved, ie. Upon etnry to Potential_Connect_as_Src in TCPC Spec Figure "TCPC State Machine before a Connection". The TCPC toggles CC1 & CC2 after receiving COMMAND.Look4Connection and until a connection is detected. Upon connection, the TCPC shall resolve to either an Rp or Rd and report the CC1/CC2 State in the CC_STATUS register. The CC pins shall stay in Potential_start_as_SRC or Potential_start_as_ Sink until directed otherwise.	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				5:4	Rp Value 00b: Rp default 01b: Rp 1.5A 10b: Rp 3.0A 11b: Reserved		
				3:2	CC2 00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6		
				1:0	CC1 00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6		
1Bh	FAULT_CONTROL	Read / Write Byte	0x00	7:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				4	Force Off VBUS Enable 0b: Force Off VBUS circuit enabled 1b: Force Off VBUS circuit disabled Note that the STANDARD INPUT SIGNAL Force Off Vbus (4.5.1) has the same behavior as writing to this bit. Optional Normative	Partial Required	Supported
				3	VBUS Discharge Timer 0b: VBUS Discharge Timer enabled 1b: VBUS Discharge Timer disabled Optional Normative		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				2	VBUS Over Current Protection Fault Enable 0b: Internal and External OCP circuit enabled 1b: Internal and External OCP circuit disabled The TCPC shall not disconnect VBUS due to internal OCP.		Not supported
				1	VBUS Over Voltage Protection Fault Enable 0b: Internal and External OVP circuit enabled 1b: Internal and External OVP circuit disabled The TCPC shall not disconnect VBUS due to internal OVP.		Supported
				0	VCONN Over Current Fault Enable 0b: Fault detection circuit enabled 1b: Fault detection circuit disabled Required if DEVICE_CAPABILITIES_2.VCONNOvercurrentFaultCapable = 1b		Not supported
1Ch	POWER_CONTROL	Read / Write Byte	0x60	7	Fast Role Swap Enable 0b: Disable Fast Role Swap function 1b: Enable Fast Role Swap function Sink TCPC shall support this bit if DEVICE_CAPABILITIES_2.SinkFRSwap = 1b. Source TCPC shall support this bit if DEVICE_CAPABILITIES_2.SourceFRSwap = 1b. The detailed functional requirements for Source and Sink TCPCs supporting Fast Role Swap are provided in TCPC Spec. *Additional PTN5110 Specific Behaviour:* *- Assert the FRS_EN pin while this bit is set* *- Enable detection of the FRS signal on CC by the PHY* *- Once FRS is detected, monitor the vbus voltage, and control the EN_SNK* and EN_SRC pins according to the USBPD3.0 spec* *While enabled* *- The FRO clock will always be enabled* *- The ADC will be enabled to monitor VBUS* *When 0b EXT_GPIO_CONFIG.FRS_EN can be used to control the FRS_EN pin independent of the Fast Role Swap feature.*	Partial Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				6	VBUS_VOLTAGE Monitor 0b: VBUS_VOLTAGE Monitoring is enabled 1b: VBUS_VOLTAGE Monitoring is disabled (default) Controls only VBUS_VOLTAGE Monitoring. VBUS_VOLTAGE shall report all zeros if disabled. Optional Normative		
				5	Disable Voltage Alarms 0b: Voltage Alarms Power status reporting is enabled 1b: Voltage Alarms Power status reporting is disabled (default) Controls VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. Required if DEVICE_CAPABILITIES_1.VBUSMeasuremen andAlarmCapable = 1b		
				4	AutoDischargeDisconnect 0b: The TCPC shall not automatically discharge VBUS based on VBUS voltage (default) 1b: The TCPC shall automatically discharge Setting this bit in a Source TCPC triggers the following actions upon disconnection detection: 1. Disable sourcing power over VBUS 2. VBUS discharge Sourcing power over VBUS shall be disabled before or at the same time as starting VBUS discharge. Setting this bit in a Sink TCPC triggers the following action upon disconnection detection: 1. VBUS discharge The TCPC shall automatically disable discharge (without clearing this bit) once the voltage on VBUS is below vSafe0V (max) or VBUS_STOP_DISCHARGE_THRESHOLD.VBUS_STOP_DISCHARGE_THRESHOLD, if enabled, takes priority over vSafe0V. TCPC shall not re-apply discharge circuit if VBUS rises above VBUS_STOP_DISCHARGE_THRESHOLD or vSafe0V. Required		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				3	Enable Bleed Discharge 0b: Disable bleed discharge (default) 1b: Enable bleed discharge of VBUS Bleed Discharge is a low current discharge to provide a minimum load current if needed 10K Ohms maximum or 2mA minimum Optional Normative		
				2	Force Discharge 0b: Disable forced discharge (default) 1b: Enable forced discharge of VBUS. Optional Normative		
				1	VCONN Power Supported 0b: TCPC delivers at least 1W on VCONN 1b: TCPC delivers at least the power indicated in DEVICE_CAPABILITIES.VCONNPowerSupported Refer to TCPC datasheet for actual power limit implemented Optional Normative		
				0	Enable VCONN 0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC Required		
1Dh	CC_STATUS	Read Only Byte	0x00	7:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				5	Looking4Connection 0b: the TCPC has stopped toggling or (ROLE_CONTROL.DRP=00) 1b: the TCPC is toggling	Required	Supported
				4	ConnectResult 0b: the TCPC is presenting Rp 1b: the TCPC is presenting Rd This bit is only valid if the TCPC was a DRP and has stopped DRP toggling.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement

				3:2	CC2 State
					If (ROLE_CONTROL.CC2=Rp) or (ConnectResult=0)
					00b: SRC_Open (Open, Rp)
					01b: SRC_Ra (below maximum vRa)
					10b: SRC_Rd (within the vRd range)
					11b: reserved
					If (ROLE_CONTROL.CC2=Rd) or (ConnectResult=1)
					00b: SNK_Open (Below maximum vRa)
					01b: SNK_Default (Above minimum vRd-Connect)
					10b: SNK_Power1_5 (Above minimum vRd-Connect) Detects Rp 1.5A
					11b: SNK_Power3_0 (Above minimum vRd-Connect) Detects Rp 3.0A
					If ROLE_CONTROL.CC2=Ra, this field is set to 00b
					If ROLE_CONTROL.CC2=Open, this field is set to 00b
					This field always returns 00b if (Look4Connection=1) or (POWER_CONTROL.EnableVconn=1 and TCPC_CONTROL.PlugOrientation=1). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.		

				1:0	CC1 State
					If (ROLE_CONTROL.CC1 = Rp) or (ConnectResult=0)
					00b: SRC_Open (Open, Rp)
					01b: SRC_Ra (below maximum vRa)
					10b: SRC_Rd (within the vRd range)
					11b: reserved
					If (ROLE_CONTROL.CC1 = Rd) or ConnectResult=1)
					00b: SNK_Open (Below maximum vRa)
					01b: SNK_Default (Above minimum vRd-Connect)
					10b: SNK_Power1_5 (Above minimum vRd-Connect) Detects Rp-1.5A
					11b: SNK_Power3_0 (Above minimum vRd-Connect) Detects Rp-3.0A
					If ROLE_CONTROL.CC1=Ra, this field is set to 00b
					If ROLE_CONTROL.CC1=Open, this field is set to 00b
					This field always returns 00b if (Look4Connection=1) or (POWER_CONTROL.EnableVconn=1 and TCPC_CONTROL.PlugOrientation=0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
1Eh	POWER_STATUS	Read Only Byte	0x48	7	Debug Accessory Connected 0b: No Debug Accessory connected (default) 1b: Debug Accessory connected Autonomously controlled by the TCPC or controlled by the TCPM. Decision if controlled by the TCPC or TCPM is set in the TCPC_ CONTROL register. Optional Normative	Required	Supported
				6	TCPC Initialization Status 0b: The TCPC has completed initialization and all registers are valid 1b: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..-0Fh Required		
				5	Sourcing High Voltage 0b: vSafe5V 1b: High Voltage This bit does not control the path, just provides a monitor of the status. Assert as long as supplying voltage greater than vSafe5V. Required if voltage higher than vSafe5V can be sourced This bit is not valid if POWER_STATUS.SourcingVbus = 0b.		
				4	Sourcing VBUS 0b: Sourcing VBUS is disabled 1b: Sourcing VBUS is enabled This does not control the path, just provides a monitor of the status. Required		
				3	VBUS Detection Enabled 0b: VBUS Detection Disabled 1b: VBUS Detection Enabled (default) Indicates whether the TCPC is monitoring for VBUS Present and vSafe0V level, or the detection circuits have been powered off Required		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				2	VBUS Present 0b: VBUS Disconnected 1b: VBUS Connected The TCPC shall report VBUS present when TCPC detects VBUS rises above 4V. The TCPC shall report VBUS is not present when TCPC detects VBUS falls below 3.5V. The TCPC may report VBUS is not present if VBUS is between 3.5V and 4V. This bit is not valid when POWER_STATUS.VbusDetectionEnabled = 0b. Required		
				1	VCONN Present 0b: VCONN is not present 1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V Required		
				0	Sinking VBUS 0b: Sink is Disconnected (Default and if not supported) 1b: TCPC is sinking VBUS to the system load Required		
1Fh	FAULT_STATUS	Read / Write Byte	0x80	7	All Registers Reset To Default 0b: No Fault detected 1b: All Registers Reset To Default fault latched This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs.	Required	Supported
				6	Force Off VBUS Status 0b: No Fault Detected, no action (default and not supported) 1b: VBUS Source/Sink has been forced off due to external fault The TCPC has disconnected VBUS due to STANDARD_INPUT.ForceOffVbus. Required if STANDARD_INPUT_CAPABILITIES_1.ForceOffVbus = 1b		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				5	Auto Discharge Failed 0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.AutoDischargeDisconnect is set, the TCPC shall report discharge fails if Vbus is not below vSafe0V within tSafe0V. Required		
				4	Force Discharge Failed 0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.ForceDischarge is set, the TCPC shall report a discharge fails if Vbus is not below vSafe0V within tSafe0V. Required if DEVICE_CAPABILITIES_1.ForceDischarge =1b		
				3	Internal or External VBUS Over Current Protection Fault 0b: Not in an over-current protection state 1b: Over-current fault latched Required if DEVICE_CAPABILIITES_1.VBUSOCPReporting = 1b		
				2	Internal or External VBUS Over Voltage Protection Fault 0b: Not in an over-voltage protection state 1b: Over-voltage fault latched. Required if DEVICE_CAPABILIITES_1.VBUSOVPReporting = 1b		
				1	VCONN Over Current Fault 0b: No Fault detected 1b: Over current VCONN fault latched Required if DEVICE_CAPABILITIES_2.VCONNOvercurrentFaultCapable = 1b		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				0	I2C Interface Error 0b: No Error 1b: I2C error has occurred. Some of the conditions for asserting this bit: • TCPM writes to the TRANSMIT register when the TRANSMIT_BUFFER is empty • The watchdog timer has expired • TCPM writes an invalid COMMAND • TCPM writes a non-zero value to a reserved bit in a register • TCPM writes to the TRANSMIT_BUFFER when TCPC is transmitting the Fast Role Swap signal as triggered by the STANDARD INPUT signal Source Fast Role Swap • TCPM writes to CONFIG_EXTENDED1.FRSwapBidirectionalPin and STANDARD_INPUT_CAPABILITIES.SourceFastRoleSwap is not 10b Required		
20h	EXTENDED_STATUS	Read Only Byte	0x00	7:1	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				0	vSafe0V 0b: VBUS is not at vSafe0V 1b: VBUS is at vSafe0V The TCPC shall report VBUS is at vSafe0V when TCPC detects VBUS is below 0.8V. This bit is not valid when POWER_STATUS.VbusDetectionEnabled = 0b. Required ***PTN5110 Specific:*** ***Latency for rising edge and falling edge will be different. Rising edge (VBUS enters vSafe0V region) will meet tSetReg, falling edge will have a larger latency and may not update until vbus rises to vbus present region.***	Required	Supported
21h	ALERT_EXTENDED	Read / Write Byte	0x00	7:3	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				2	Timer Expired 0b: Generic timer is not expired 1b: Generic timer has expired		Supported
				1	Source Fast Role Swap 0b: No Fast Role Swap signal sent 1b: Fast Role Swap signal sent due to STANDARD INPUT Source Fast Role Swap is set low		Not supported
				0	Sink Fast Role Swap 0b: No Fast Role Swap signal received 1b: Fast Role Swap signal received		Supported
22h	Reserved	N/A	0x00	N/A	Reserved		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
23h	COMMAND	Write Only Byte	0x00	7:0	Command 0001 0001b : **WakeI2C** (no action is taken other than to wake the I2C interface). 0010 0010b : **DisableVbusDetect.** Disable Vbus present detection. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing or sinking power over Vbus enabled. 0011 0011b : **EnableVbusDetect.** Enable Vbus present detection. 0100 0100b : **DisableSinkVbus.** Disable sinking power over Vbus. This COMMAND does not disable POWER_STATUS.VBUSPresent detection. 0101 0101b : **SinkVbus.** Enable sinking power over Vbus and enable Vbus present detection. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing power over Vbus enabled. 0110 0110b : **DisableSourceVbus.** Disable sourcing power over Vbus. The TCPC shall stop reporting FAULT_STATUS. Internal or External OCP or OVP Faults. This COMMAND does not disable POWER_STATUS.VBUSPresent detection. 0111 0111b : **SourceVbusDefaultVoltage.** Enable sourcing vSafe5V over Vbus and enable Vbus present detection. Source shall transition to vSafe5V if at a high voltage. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sinking power over Vbus enabled. 1000 1000b : **SourceVbusHighVoltage.** Execute sourcing high voltage over Vbus. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it is either does not have ability to source voltages higher than vSafe5V or is already sourcing vSafe5V. The actual voltage to be sourced may be set in a vendor defined manner. The TCPM may need to send vendor defined commands before sending this COMMAND.	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
					1001 1001b : **Look4Connection.** Start DRP Toggling if ROLE_CONTROL.DRP=1b. If ROLE_CONTROL.CC1/CC2 = 01b start with Rp, if ROLE_CONTROL.CC1/CC2 =10b start with Rd. If ROLE_CONTROL.CC1/CC2 are not both 01b or 10b, then do not start toggling. 1010 1010b : **RxOneMore.** Configure the receiver to automatically clear the RECEIVE_DETECT register after sending the next GoodCRC. This is used to shutdown reception of packets at a known point regardless of packet separation or the depth of the receive FIFO in the TCPC. 1100 1100b : **SendFRSwapSignal.** Source TCPC sends Fast Role Swap signal within tTCPCSendFRSwap after receiving this command if POWER_CONTROL.FastRoleSwapEnable = 1b. TCPC shall ignore this command and assert the FAULT_STATUS.I2CinterfaceError if POWER_CONTROL.FastRoleSwapEnable = 0b. 1101 1101b : **ResetTransmitBuffer.** The TCPC resets the pointer of the TRANSMIT_BUFFER register and the contents of TRANSMIT_BUFFER becomes invalid when this command is issued by the TCPM. This command shall be supported by TCPC compliant with USB Port Controller Specification Revision 2.0, 1110 1110b : **ResetReceiveBuffer.** The TCPC resets the pointer of RX_BUFFER when this command is issued by the TCPM. TCPC does not clear the content of the buffer upon receiving this command. The TCPM issues this command in order to re-read the RECEIVE_BUFFER.RX_BUF_BYTE_x. This command shall be supported by TCPC compliant with USB Port Controller Specification Revision 2.0, 1111 1111b : **I2C Idle**		
24h	DEVICE_CAPABILITIES_1	Read Only Word	0x7EDF	15	VBUS High Voltage Target 0b: VBUS_HV_TARGET register not implemented (default) 1b: VBUS_HV_TARGET register implemented	Required	Not supported
				14	VBUS OCP Reporting 0b: VBUS OCP is not reported by the TCPC 1b: VBUS OCP is reported by the TCPC Support for both FAULT_STATUS.InternalorExternalOCP and FAULT_CONTROL. InternalorExternalOCP implemented		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				13	VBUS OVP Reporting 0b: VBUS OVP is not reported by the TCPC 1b: VBUS OVP is reported by the TCPC Support for both FAULT_STATUS.InternalorExternalOVP and FAULT_CONTROL. InternalorExternalOVP implemented		Supported
				12	BleedDischarge 0b: No Bleed Discharge implemented in TCPC 1b: Bleed Discharge is implemented in the TCPC Support for POWER_CONTROL.EnableBleedDischarge implemented		Supported
				11	ForceDischarge 0b: No Force Discharge implemented in TCPC 1b: Force Discharge is implemented in the TCPC Support for POWER_CONTROL.ForceDischarge, FAULT_STATUS.ForceDischargeFailed, and VBUS_STOP_DISCHARGE_THRESHOLD implemented Support for VBUS_STOP_DISCHARGE_THRESHOLD register implemented when act as Source		Supported
				10	VBUS Measurement and Alarm Capable 0b: No VBUS voltage measurement nor VBUS Alarms 1b: VBUS voltage measurement and VBUS Alarms Reported in VBUS_VOLTAGE, VBUS_VOLTAGE_ALARM_HI_CFG, and VBUS_VOLTAGE_ALARM_LO_CFG Registers		Supported
				9:8	Source Resistor supported 00b: Rp default only 01b: Rp 1.5A and default 10b: Rp 3.0A, 1.5A, and default 11b: Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				7:5	Roles Supported 000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support 100b: DRP only 101b: Source, Sink, DRP, Adapter/Cable all supported 110b: Source, Sink, DRP 111b: Not valid		Source, Sink, DRP. Supported
				4	SOP'_DBG/SOP"_DBG Support 0b: All SOP* except SOP'_DBG/SOP"_DBG 1b: All SOP* messages are supported Configured in RECEIVE_DETECT and TRANSMIT		Supported
				3	Source VCONN 0b: TCPC is not capable of switching VCONN 1b: TCPC is capable of switching VCONN Support for POWER_CONTROL.EnableVCONN and POWER_STATUS.VCONNPresent implemented		Supported
				2	Sink VBUS 0b: TCPC is not capable controlling the sink path to the system load 1b: TCPC is capable of controlling the sink path to the system load Support for POWER_STATUS.SinkingVbus, COMMAND.SinkVbus, and COMMAND.DisableSinkVbus implemented		Supported
				1	Source High Voltage VBUS 0b: TCPC is not capable of controlling the source high voltage path to VBUS 1b: TCPC is capable of controlling the source high voltage path to VBUS Support for VBUS_VOLTAGE, POWER_STATUS.SourcingHighVoltage, and COMMAND.SourceVbusHighVoltage implemented NOTE: DEVICE_CAPABILITIES_1.VBUS Measurement and Alarm Capable shall be set to 1b if Source High Voltage VBUS is enabled		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				0	Source VBUS 0b: TCPC is not capable of controlling the source path to VBUS 1b: TCPC is capable of controlling the source path to VBUS Support for POWER_STATUS.SourcingVbus, COMMAND.SourceVbusDefaultVoltage, COMMAND.DisableSourceVbus, COMMAND.EnableVbusDetect and COMMAND.DisableVbusDetect implemented		Supported
26h	DEVICE_CAPABILITIES_2	Read Only Word	0x37C7	15:14	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	
				13	Generic Timer 0b: GENERIC_TIMER register is not supported 1b: GENERIC_TIMER register is supported		Supported
				12	Long Message 0b: TCPC is only capable of passing 30 bytes content of the SOP* message 1b: TCPC is capable of passing 264 bytes content of the SOP* message. TRANSMIT _BUFFER is capable to hold 264 bytes content of the SOP* message. The TCPM can write up to 132 bytes to the TX_BUF_BYTE_ x in one burst. RECEIVE_BUFFER is sized to hold a 264 bytes content SOP* message plus a 30 bytes content SOP* message.		Supported
				11	SMBus PEC 0b: TCPC_CONTROL.EnableSMBusPEC not implemented 1b: TCPC_CONTROL.EnableSMBusPEC implemented		Not supported
				10	Source FR Swap 0b: Not capable of sending Fast Role Swap signal as Source TCPC when receiving COMMAND.SendFRSwapSignal or when STANDARD INPUT Source Fast Role Swap is set low. 1b: Capable of sending Fast Role Swap signal as Source TCPC when receiving COMMAND.SendFRSwapSignal. If STANDARD_INPUT_ CAPABITILIES.SourceFRSwap = 1b, capable of sending Fast Role Swap signal as Source TCPC when STANDARD INPUT Source Fast Role Swap is set low.		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				9	Sink FR Swap 0b: POWER_CONTROL.FastRoleSwapEnable not supported as Sink TCPC 1b: POWER_CONTROL.FastRoleSwapEnable supported as Sink TCPC		Supported
				8	Watchdog Timer 0b: TCPC_CONTROL.Enable Watchdog Timer not implemented 1b: TCPC_CONTROL.Enable Watchdog Timer implemented		Supported
				7	Sink Disconnect Detection 0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default: Use POWER_STATUS.VbusPresent=0b to indicate a Sink disconnect) 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented		Supported
				6	Stop Discharge Threshold 0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented (default) 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented		Supported
				5:4	VBUS Voltage Alarm LSB 00b: TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01b: TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11: reserved Support for VBUS_VOLTAGE_ALARM_LO_CFG and VBUS_VOLTAGE_ALARM_HI implemented		Default supported.

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				3:1	VCONN Power Supported 000b: 1.0W 001b: 1.5W 010b: 2.0W 011b: 3W 100b: 4W 101b: 5W 110b: 6W 111b: External		External Supported.
				0	VCONN Overcurrent Fault Capable 0b: TCPC is not capable of detecting a Vconn fault 1b: TCPC is capable of detecting a Vconn fault Support for FAULT_STATUS.VCONNOverCurrentFault and FAULT_CONTROL.VCONNOverCurrentFault implemented		Supported
28h	STANDARD_INPUT_CAPABILITIES	Read Only Byte	0x06	7:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				4:3	Source Fast Role Swap 00b: Not present in TCPC 01b: Present in TCPC as an input only pin 10b: Present in TCPC as a bidirectional pin, sharing with the STANDARD OUTPUT signal Vbus Sink Disconnect Detect Indicator. The “Vbus Sink Disconnect Detect Indicator” bit in STANDARD_OUTPUT_CAPABILITIES register shall also be set to 1. 11b: Reserved	Required	Not supported
				2	Vbus External Over Voltage Fault Capable 0b: Not present in TCPC 1b: Present in TCPC		Supported
				1	Vbus External Over Current Fault Capable 0b: Not present in TCPC 1b: Present in TCPC		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				0	Force Off VBUS Capable (Source or Sink) 0b: Not present in TCPC 1b: Present in TCPC		Supported
29h	STANDARD_OUTPUT_ CAPABILITIES	Read Only Byte	0x40	7	Vbus Sink Disconnect Detect Indicator 0b: Not present in TCPC 1b: Present in TCPC Shall present in TCPC if “Source Fast Role Swap” in STANDARD_INPUT_CAPABILITIES is set to 10b ((present as a bidirectional pin)).	Required	Not supported
				6	Debug Accessory Indicator 0b: Not present in TCPC 1b: Present in TCPC		Supported
				5	Vbus Present Monitor 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				4	Audio Adapter Accessory Indicator 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				3	Active Cable Indicator 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				2	MUX Configuration Control 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				1	Connection Present Indicator 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				0	Connector Orientation 0b: Not present in TCPC 1b: Present in TCPC		Not supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
2Ah	CONFIGURE EXTENDED1	Read / Write Byte	0x00	7:2	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Optional Normative	Not supported
				1	FR Swap Bidirectional Pin 0b: The bidirectional pin is configured as STANDARD INPUT signal Source Fast Role Swap (default) 1b: The bidirectional pin is configured as STANDARD OUTPUT signal Vbus Sink Disconnect Detect Indicator The TCPC shall ignore TCPM writing to this bit and assert FAULT_STATUS.I2CinterfaceError if STANDARD_INPUT_CAPABILITIES.SourceFastRoleSwap is not set to 10b (present as a bidirectional pin), and STANDARD_OUTPUT_CAPABILITIES.VbusSinkDisconnectDetectIndicator is not set to 1.		
				0	Standard Input Source FR Swap 0b: Allow STANDARD INPUT signal Source Fast Role Swap to trigger sending Fast Role Swap signal (default) 1b: Block STANDARD INPUT signal Source Fast Role Swap to trigger sending Fast Role Swap signal This bit enables or disables STANDARD INPUT signal Source Fast Role Swap functionality. Required if STANDARD_INPUT_CAPABILITIES.SourceFastRoleSwap is set to either 01b or 10b (present).		
2Bh	Reserved	N/A		N/A	Reserved		
2Ch	GENERIC_TIMER	Write Only Word	0x0000	15:0	Timer Value 16-bit timer value with 0.1ms LSB. A non-zero value starts the timer. A value of zero stops the timer. The timer does not restart after it has expired. Required if DEVICE_CAPABILITIES_2.GenericTimer = 1b.	Optional Normative	Supported
2Eh	MESSAGE_HEADER_INFO	Read / Write Byte	0x02	7:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				4	Cable Plug 0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				3	Data Role 0b: UFP 1b: DFP		
				2:1	USB PD Specification Revision 00b: Revision 1.0 01b: Revision 2.0 (*NOTE - As USBPD 2.0 requires this value, the TCPM should select this even when it has support for USBP3.0, unless the partner also supports USBPD3.0*) 10b: Revision 3.0 (*NOTE - USBPD 3.0 allows GoodCRC to use any value except 11b reserved*) 11b: Reserved		
				0	Power Role 0b: Sink 1b: Source		
2Fh	RECEIVE_DETECT	Read / Write Byte	0x00	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				6	Enable Cable Reset 0b: TCPC does not detect Cable Reset signaling (default) 1b: TCPC detects Cable Reset signaling	Required	Supported
				5	Enable Hard Reset 0b: TCPC does not detect Hard Reset signaling (default) 1b: TCPC detects Hard Reset signaling		
				4	Enable SOP_DBG_PP message 0b: TCPC does not detect SOP_DBG" message (default) 1b: TCPC detects SOP_DBG" message		
				3	Enable SOP_DBG_P message 0b: TCPC does not detect SOP_DBG' message (default) 1b: TCPC detects SOP_DBG' message		
				2	Enable SOP_PP message 0b: TCPC does not detect SOP" message (default) 1b: TCPC detects SOP" message		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				1	Enable SOP_P message 0b: TCPC does not detect SOP' message (default) 1b: TCPC detects SOP' message		
				0	Enable SOP message 0b: TCPC does not detect SOP message (default) 1b: TCPC detects SOP message		
30h	READABLE_BYTE_COUNT	Read Only Byte	0x00	7:0	Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). The content of this register is undefined when the RECEIVE_BUFFER is cleared	Required	Supported
	RX_BUF_FRAME_TYPE	Read Only Byte	0x00	7:3	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				2:0	Received SOP* Message 000b: Received SOP 001b: Received SOP' 010b: Received SOP'' 011b: Received SOP_DBG' 100b: Received SOP_DBG'' 110b: Received Cable Reset All others are reserved. Type of received frame. This register is “hidden” and can only be accessed by reading at address 30h.		
	RX_BUF_BYTE_x	Read Only Byte	0x00		Receive Buffer Bytes. These registers are “hidden” and can only be accessed by reading at address 30h.		
50h	TRANSMIT	Read/ Write Byte	0x00	7:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	Supported
				5:4	Retry Counter 00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				3	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				2:0	Transmit SOP* message 000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP'' 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)		
51h	I2C_WRITE_BYTE_COUNT	Write Only Byte	0x00	7:0	The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I2C/SMBus transaction.	Required	Supported
	TX_BUF_BYTE_x	Write Only Byte	0x00		Transmit Buffer Bytes. These registers are “hidden” and can only be accessed by writing to address 51h.	Required	Supported
70h	VBUS_VOLTAGE	Read Only Word	0x0000	15:12	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Optional Normative	Supported
				11:10	Vbus Scale Factor 00: VBUS measurement not scaled. 01: VBUS measurement divided by 2 10: VBUS measurement divided by 4 11: reserved		
				9:0	VBUS voltage measurement 10-bit measurement of (VBUS / Scale Factor) TCPM multiplies this value by the scale factor to obtain the voltage measurement. Voltages greater than or equal to 4V shall meet +/-2% absolute value or +/- 50mV, whichever is greater. The LSB is 25mV.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
72h	VBUS_SINK_DISCONNECT_ THRESHOLD	Read / Write Word	0x008C	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	Supported
				9:0	Vbus Sink Disconnect trip point (Default 3.5V) 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_ CAPABILITIES_2.VbusVoltageAlarmLsb.		
74h	VBUS_STOP_DISCHARGE_ THRESHOLD	Read / Write Word	0x0020	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				9:0	Vbus Stop Discharge trip point (Default 0.8V) 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_ CAPABILITIES_2.VbusVoltageAlarmLsb.		
76h	VBUS_VOLTAGE_ALARM_HI_CFG	Read / Write Word	0x0000	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Optional Normative	Supported
				9:0	Vbus Lo Voltage trip point 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_ CAPABILITIES_2.VbusVoltageAlarmLsb.		
78h	VBUS_VOLTAGE_ALARM_LO_CFG	Read / Write Word	0x0000	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				9:0	Vbus Hi Voltage trip point 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_ CAPABILITIES_2.VbusVoltageAlarmLsb.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
7Ah	VBUS_HV_TARGET	Read / Write Word	0x0000	15:0	VBUS voltage target 16-bit for the VBUS voltage target with 20mV LSB. +/- 5% accuracy. The TCPC shall ignore if the value is less than 5.5V (113h) or DEVICE_CAPABILITIES_1.VbusHighVoltageTarget is set to 0b.	Optional Normative	Not supported
7Ch-7Fh	Reserved	N/A	0x0000	N/A	Reserved		
80h	EXT_CFG_ID	Read Only Word	NA	15:0	For NXP Internal Use Only	Vendor Defined	Supported
82h	EXT_ALERT	Read / Write Word	0x0000	15:8	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				7	GPIO Status Change 0b: Cleared 1b: An GPIO status change has occurred, read the EXT_GPIO_STATUS register. Only IILIM_5V_VBUS can be configured to raise an alert on change. See EXT_GPIO_CONFIG and EXT_GPIO_ALERT_CONFIG.		
				6:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
84h	EXT_ALERT_MASK	Read / Write Word	0x0000	15:8	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				7	GPIO Status Change 0b: Interrupt masked (default) 1b: Interrupt unmasked		
				6:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
86h	EXT_CONFIG	Read /Write Word	0x0000	15:7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6:4	Reserved Shall be set to zero by sender, shall be ignored by receiver.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				3:2	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				1:0	Automatic Discharge for Negative Transition (Controls the behaviour when executing the COMMAND.SourceVbusDefaultVoltage some time after executing COMMAND.SourceVbusHighVoltage, while still connected.) 00b : Set EN_SNK1=0, Discharge to 5V, Set EN_SRC=1 (default) 01b : Set EN_SNK1=0, Discharge to VBUS_STOP_DISCHARGE_ THRESHOLD, Set EN_SRC=1 10b : Set EN_SNK1=0, Automatic discharge disabled, Allow TCPM to use force discharge, when ADC monitors 5V set EN_SRC=1 11b: Reserved		
88h	EXT_FAULT_CONFIG	Read / Write Byte	0x1F	7:4	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				4	Open Fets On ADC Alarm 0b: Do not open fets on ADC Alarm 1b: Open FETs (EN_SNK1, EN_SRC) on ADC Alarm (High or Low) (Default)		
				3	VCONN Over Current Limit Enable (OCL) 0b: OCL and SCL Fault detection circuit disabled 1b: OCL and SCL Fault detection circuit enabled (Default) when FAULT_ CONTROL.VCONN Over Current Fault set to Enabled (0) (Default) **This register should be left at the default value for normal operation.** VCONN Short Circuit Protection (SCP) is also enabled/disabled by this bit. FAULT_CONTROL.VCONN Over Current Fault Must also be set to Enabled (0). this register must be set before enabling the vconn switch or while FAULT_CONTROL.VCONN Over Current Fault is disabled.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				2	VCONN Over Temperature Fault Enable (OTF) 0b: OTF Fault detection circuit disabled 1b: OTF Fault detection circuit enabled (Default) when FAULT_CONTROL.VCONN Over Current Fault set to Enabled (0) (Default) **This register should be left at the default value for normal operation.** FAULT_CONTROL.VCONN Over Current Fault Must also be set to Enabled (0), this register must be set before enabling the vconn switch or while FAULT_CONTROL.VCONN Over Current Fault is disabled.		
				1	Reserved Shall be set to 1 by sender, shall be ignored by receiver.		
				0	VCONN Reverse Current Fault Enable (RCP) 0b: RCP Fault detection circuit disabled 1b: RCP Fault detection circuit enabled (Default) when FAULT_CONTROL.VCONN Over Current Fault set to Enabled (0) (Default) **This register should be left at the default value for normal operation.** FAULT_CONTROL.VCONN Over Current Fault Must also be set to Enabled (0), this register must be set before enabling the vconn switch or while FAULT_CONTROL.VCONN Over Current Fault is disabled.		
89h	Reserved	Read / Write Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
8ah	Reserved	Read /Write Word	0x0000	15:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
8ch	Reserved	Read /Write Word	0x0000	15:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
8eh	EXT_CONTROL	Read /Write Byte	0x60	7:4	Bleed Discharge Strength (Only applied on write to POWER_CONTROL) 0001b : Select 3.2K Ohm typical (+/- 15%) pulldown resistor to ground on Vbus 0010b : Select 8K Ohm typical (+/- 15%) pulldown resistor to ground on Vbus 0100b : Select 20K Ohm typical (+/- 15%) pulldown resistor to ground on Vbus 1000b : Select 50 KOhm typical (+/- 15%) pulldown resistor to ground on Vbus Other values - resistors are applied in parallel: 0110b : 5.7K Ohm (+/- 15%) (Select 8K Ohm and 20K Ohm) pulldown resistor to ground on Vbus (Default) This register does not enable the bleed discharge. This value must be changed before writing to POWER_CONTROL.Enable Bleed Discharge.	Vendor Defined	Supported
				3	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				2:1	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				0	VCONN Force Discharge 0b: VCONN discharge path is disabled. 1b: VCONN switch is disabled and the discharge path is enabled. The VCONN discharge path will be automatically disabled when the VCONN Voltage completes discharge to vVCONNDischarge, however the TCPM must clear this bit manually, after wating tVCONNDischarge. When using this bit to control a VCONN discharge, a read-modify-write should be used to ensure the other fields are not changed. This should always be cleared to 0 before writing POWER_ CONTROL.Enable VCONN = 1.		
8fh	Reserved	Write Only Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
90h	EXT_STATUS	Read Only Word	0x0000	15:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				4	VCONN Over Current Limit Fault Status (OCL) 0b: No Fault detected 1b: Over current VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				3	VCONN Over Temperature Fault Status (OTF) 0b: No Fault detected 1b: Over temperature VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				2	VCONN Short Circuit Fault Status (SCF) 0b: No Fault detected 1b: Short circuit VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				1	VCONN Reverse Current Fault Status (RCP) 0b: No Fault detected 1b: Reverse current VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
92h	EXT_GPIO_CONFIG	Read / Write Byte	0x03	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	FRS_EN 0b : Input Pin, Output will be set according to POWER_CONTROL.Fast Role Swap Enable (default) 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write. POWER_CONTROL.Fast Role Swap Enable always has priority over this field.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				5	EN_SRC 0b : Controlled by COMMAND.SourceVbusDefaultVoltage (default) 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write. **This register should be left at the default value for standard TCPC operation.**		
				4	EN_SNK1 0b : Controlled by COMMAND.SinkVbus or COMMAND.SourceVbusHighVoltage (default) 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write. **This register should be left at the default value for standard TCPC operation.**		
				3	IILIM_5V_VBUS 0b : Input Pin 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write.		
				2:0	Reserved Shall be set to 0x3 by sender, shall be ignored by receiver.		
93h	EXT_GPIO_CONTROL	Read / Write Byte	0x00	7:2	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	FRS_EN 0b : Drive Low, Unless POWER_CONTROL.Fast Role Swap Enable is set. 1b : Drive High (Only when EXT_GPIO_CONFIG.FRS_EN = 1 and POWER_CONTROL.Fast Role Swap Enable = 0) POWER_CONTROL.Fast Role Swap Enable always has priority over this field. To change only 1 pin value the TCPM must do a read-modify-write.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				5	EN_SRC 0b : Drive Low 1b : Drive High (Only when EXT_GPIO_CONFIG.EN_SRC = 1) To change only 1 pin value the TCPM must do a read-modify-write.		
				4	EN_SNK1 0b : Drive Low 1b : Drive High (Only when EXT_GPIO_CONFIG.EN_SNK1 = 1) To change only 1 pin value the TCPM must do a read-modify-write.		
				3	IILIM_5V_VBUS 0b : Drive Low 1b : Drive High (Only when EXT_GPIO_CONFIG.IILIM_5V_VBUS = 1) To change only 1 pin value the TCPM must do a read-modify-write.		
				2:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
94h	EXT_GPIO_ALERT_CONFIG	Read /Write Word	0x0038	15:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				5:3	IILIM_5V_VBUS 000b: Active Low Level Sensitive 001b: Active High Level Sensitive 010b: Rising Edge Triggered 011b: Falling Edge Triggered 100b: Triggered on both edges 101b: Reserved 110b: Reserved 111b: Disable Interrupt (default)		
				2:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
96h	EXT_GPIO_STATUS	Read Only Byte	unde fined	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	FRS_EN 0b : Pin is low (or input disabled) 1b : Pin is high		
				5:4	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				3	IILIM_5V_VBUS 0b : Pin is low (or input disabled) 1b : Pin is high		
				2:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
97h	SOURCE_HIGH_VOLTAGE_MB4B_ TIME	Read / Write Byte	Device Specific PTN5110 HQ/PTN5 110DHQ: 0x1E PTN51 10THQ: 0x00	7:0	Source High Voltage Make Before Break Time (ms). Controls the behaviour when the TCPM issues the SourceVbusHighVoltage command: 0 : Break before make: Disable the EN_SRC and then enable EN_SNK1 immediately. 1-255 : Make before break: Time, in milliseconds(ms), EN_SRC and EN_ SNK1 will both be enabled immidiately, then after this time EN_SRC is disabled and EN_SNK1 only enabled.	Vendor Defined	Supported
98h	Reserved	Read Only Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
99h	Reserved	Read Only Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
9Ah	ADC_FILTER_CONTROL_1	Read / Write Byte	0x00	7:0	ADC Voltage Filter Control - Controls the amount of debounce/filtering performed on the ADC voltage threshold detects. This is used for the Vbus Over and Vbus Under Voltage Alarms. 0 : Disabled. No debouncing/filtering is performed 1 - 255 : The measured voltage must be beyond the threshold (above for high thresholds, below for low thresholds) for ADC_FILTER_CONTROL_ 1*256 us before the condition is considered true and an interrupt asserted.	Vendor Defined	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
9Bh	ADC_FILTER_CONTROL_2	Read / Write Byte	0x13	7:0	ADC Voltage Filter Control - Controls the amount of debounce/filtering performed on the ADC voltage threshold detects. This is used for the Vbus Sink Disconnect Alarm. 0 : Disabled. No debouncing/filtering is performed 1 - 255 : The measured voltage must be beyond the threshold for ADC_FILTER_CONTROL_2 * 256 us before the condition is considered true and an interrupt asserted. 0x13: 4.9ms (default)	Vendor Defined	Supported
9Ch	VCONN_CONFIG	Read / Write Byte	0x02	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	VCONN OCL Switch Open Enable 0b: Keep sourcing current on VCONN, with the current limited. (Default) 1b: Open the switch and alert the host that a fault has occurred.		
				5	VCONN_SelfClearCtrl_Temp Controls the behaviour when a VCONN switch over temperature fault occurs. 0b: Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1b: The device waits for VCONN_TempFault_FaultRecovery time before reclosing the Vconn switch. This is attempted VCONN_NumVconnAttempts_TempFault times. If the fault persists then raise FAULT_STATUS.VCONN Over Current Fault.		
				4	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				3	VCONN_SelfClearCtrl_RCP Controls the behaviour when a VCONN switch reverse current fault occurs. 0b: Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1b: The device waits for VCONN_RCP_FaultRecovery time before reclosing the Vconn switch. This is attempted VCONN_NumVconnAttempts_RCP times. If the fault persists then raise FAULT_STATUS.VCONN Over Current Fault.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				2:0	VCONN_OCL_Threshold This specifies the Vconn current limiting threshold. 000b : 150 mA 001b : 300 mA 010b : 450 mA (Default) 011b : 600 mA 1xxb : Reserved (Typical values, see datasheet for Min/Max)		
9Dh	VCONN_FAULT_DEBOUNCE	Read / Write Byte	0x08	7:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				5:2	VCONN_RCP_FaultDebounce This controls how long a Vconn RCP must be present for it to be considered valid. 0001b : ~12 us 0010b : ~36 us (Default) 0011b : ~60 us 0100b : ~100 us 0101b : ~200 us 0110b : ~500 us 0111b : ~1000 us 1000b : ~2 ms 1001b : ~5 ms 1010b : ~10 ms 1011b : ~20 ms 11xxb : ~50 ms		
				1:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
9Eh	VCONN_FAULT_RECOVERY	Read / Write Byte	0x11	7:4	VCONN_TempFault_FaultRecovery 0000b : 0ms 0001b: 500ms (Default) 0010b: 1000ms 0011b-1111b: Reserved This specifies the amount of time the switch is to be opened after an Temperature fault is detected before the switch can be reclosed. Each value represents 500 ms. The min value is 0. The max value is 1s.	Vendor Defined	Supported
				3:0	VCONN_RCP_FaultRecovery 0000b : 0ms 0001b: 500ms (Default) 0010b: 1000ms 0011b: 1500ms 0100b: 2000ms 0101b: 2500ms 0110b: 3000ms 0111b: 3500ms 1000b: 4000ms 1001b: 4500ms 1010b: 5000ms 1011b-1111b: Reserved This specifies the amount of time the switch is to be opened after an RCP fault is detected before the switch can be reclosed. Each value represents 500 ms. The min value is 0. The max value is 5s.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
9Fh	VCONN_FAULT_ATTEMPTS	Read / Write Byte	0x00	7:4	VCONN_NumVconnAttempts_TempFault 0 : Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1-16 : Number of times to attempt to recovery from the over temperature fault. This is the number of attempts the device will try to close the Vconn switch before giving up and alerting the TCPM. After each fault occurrence, the device will increment an internal counter and reclose the Vconn switch. If the counter exceeds VCONN_NumVconnAttempts then the switch will still be closed but the TCPM will be alerted with the FAULT_STATUS.VCONN Over Current Fault. The internal counter is cleared each time the TCPM request for the Vconn switch to be closed.	Vendor Defined	Supported
				3:0	VCONN_NumVconnAttempts_RCP 0 : Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1-16 : Number of times to attempt to recovery from the reverse current fault. This is the number of attempts the device will try to close the Vconn switch before giving up and alerting the TCPM. After each fault occurrence, the device will increment an internal counter and reclose the Vconn switch. If the counter exceeds VCONN_NumVconnAttempts then the switch will not be closed and the TCPM will be alerted with the FAULT_STATUS.VCONN Over Current Fault. The internal counter is cleared each time the TCPM request for the Vconn switch to be closed.		
A0h-FFh	Reserved	N/A	0x0000	N/A	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported

11 References

1	**USB Power Delivery Specification**	Revision 3.0, Version 1.1 January 2017
2	**USB Type-C Cable and Connector Specification**	Revision 1.2, March 25, 2016
3	**USB Type-C Port Controller Interface Specification**	Revision 2.0, Version 1.0, Oct 2017

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