NXP Semiconductors
Application Note

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KW41Z BLE + IEEE® 802.15.4 Protocol Switching Timings

1. Introduction

This document describes the measurement method and protocol switching time of the radio from IEEE 802.15.4 to BLE and the other way round.

The Mobile Wireless Systems (MWS) coexistence module allows the coexistence of multiple wireless protocols (such as Bluetooth® and ZigBee® stacks) on the same MCU and/or protocols on different MCUs (such as Bluetooth and WiFi). The MWS is configured for the BLE to take priority over the IEEE 802.15.4. This means that if an IEEE 802.15.4 transaction is ongoing and the BLE wants to use the physical interface, the IEEE 802.15.4 task will be interrupted to attend the BLE task because the BLE requires to maintain timing synchronization. It is expected that some IEEE 802.15.4 packets may be dropped while the BLE task is active. Therefore, the IEEE 802.14.5 acknowledgments and retransmissions at the MAC level and/or application level should be considered to allow packet recovery.

The protocol switching time analysis explained in this document is measured by the FRDM-KW41Z hardware using a BLE + IEEE 802.15.4 hybrid application.

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2. Hardware setup

The tests described in this document use the FRDM-KW41Z evaluation board. The ports monitored by the oscilloscope are:

- Channel 1: J4[4] → GPIO protocol switch.
- Channel 2: J2[10] → TX_Switch.
- Channel 3: J2[9] → RX_Switch.

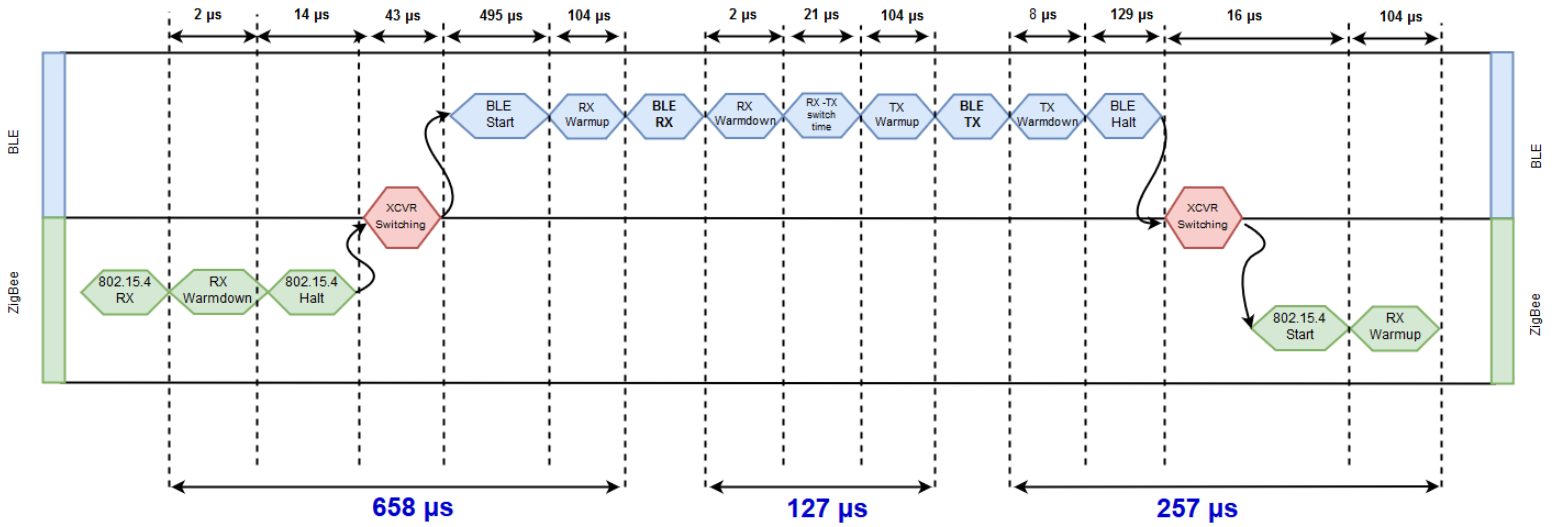

Figure 1. Protocol switching time

The BLE TX and RX timings are variable depending on the payload of the packet and they are not included in the graphic. It takes the BLE 1 µs to send 1 bit of data. The shortest BLE packet is 80 bits long and the longest packet is 2,120 bits long.

3. Definitions

Here are the definitions used in this document.

- **802.15.4 RX:** The IEEE 802.15.4 protocol acquires the radio, completes the RX warm-up phase, and is in the ON phase.
- **TSM:** Transceiver Sequence Manager.

  TX/RX warm-down: The radio to transition from the TX/RX ON (active) phase to the IDLE state. It can be calculated as:
  - TX/RX warmdown time = END_OF_TX/RX_WD - END_OF_TX/RX_WU
- **Protocol halt (802.15.4/BLE):** The transition from the radio in the IDLE state to the startup of the next protocol. It finishes when the radio starts the switching protocol.
- **XCVR switching:** The time needed for the OS to release the radio from one protocol, move to the IDLE state, and acquire the radio by some other protocol. It also includes the OS context switching.

- **BLE start:** The time needed for the radio to reach the start of the warm-up phase of any sequence (TX/RX depending on the scenario) after the radio is acquired by the BLE. This stage is the BLE preprocessing time before the radio activity.
- **TX/RX warm-up:** The radio transitions from the IDLE state, completes the warm-up phase, and switches to the TX/RX ON phase.
- **BLE TX:** The BLE protocol acquires the radio, completes the TX warm-up phase, and is in the ON phase.
- **802.15.4 start:** After the radio is acquired by the IEEE 802.15.4 stack, the time needed by the IEEE 802.15.4 to reach the start of the warm-up phase of any sequence (TX/RX, depending on the scenario). This stage is the preprocessing time before the radio activity.

4. Transceiver Sequence Manager (TSM) module

The TSM module supports one TX and one RX sequence. Each sequence consists of three phases:

- Warm-up phase.
- ON phase.
- Warm-down phase.

The central element of the TSM is an 8-bit counter. The counter is held at zero during the idle state. Any sequence can be launched from the idle state by an initiating event. During an initiating event, the TSM counter counts from zero to a programmed stop point during the warm-up phase, determined by the END_OF_TX_WU or END_OF_RX_WU registers, depending on whether the sequence is TX or RX. At the end of the warm-up stop point, the TSM counter holds its count and the TSM sequence enters the ON phase. The TSM counter remains in the ON phase and holds its count until the initiating event de-asserts or an abort occurs. When either of these conditions occurs during the ON phase, the TSM counts from the point it held during the ON phase and the sequence enters the warm-down phase. The counter continues counting until a programmed stop point is reached. This stop point is determined by the END_OF_TX_WD or END_OF_RX_WD registers, depending on whether the sequence is TX or RX. After this point is reached, the sequence returns to the IDLE state and the TSM counter returns to zero. The four 8-bit registers that control the duration of the warm-up phase (END_OF_TX_WU [7:0] and END_OF_RX_WU[7:0]) and the duration of the warm-down phase (END_OF_TX_WD[7:0] and END_OF_RX_WD[7:0]) reside in the END_OF_SEQ register.

4.1. TSM and END_OF_SEQ registers

All TSM-controlled outputs are active-high. During the warm-up and warm-down phases of any sequence, any TSM-controlled output can be programmed to assert once and then de-assert once by programming the timing registers associated with the output. Each output has four 8-bit timing registers associated with it.

The case described in this document uses the TSM-controlled output as GPIO2_TRIG_EN and GPIO3_TRIG_EN which can be asserted and de-asserted using these TSM registers: GPIO2_TRIG_E N_RX_LO, GPIO2_TRIG_E N_RX_HI, GPIO2_TRIG_E N_TX_LO, GPIO2_TRIG_E N_TX_HI, GPIO3_TRIG_E N_RX_LO, GPIO3_TRIG_E N_RX_HI, GPIO3_TRIG_E N_TX_LO, and GPIO3_TRIG_E N_TX_HI. It is programmed using the TSM_TIMING49 (TIMING49) and

TSM_TIMING50 (TIMING50), respectively. The register details of the timing registers are described in Section 5, “Software configurations”.

4.1.1. TX sequence generation

During the warm-up phase of a TX sequence, when the 8-bit TSM counter increments and the TSM counter equals or exceeds the programmed value of OUTPUTNAME_TX_HI[7:0] but is less than the programmed value of OUTPUTNAME_TX_LO[7:0], the corresponding TSM output will transition high.

During the warm-up or warm-down phase of a TX sequence, when the TSM counter equals or exceeds the programmed value of OUTPUTNAME_TX_LO[7:0], the TSM output will transition low.

If the programmed value of OUTPUTNAME_TX_HI[7:0] is greater than the length of a TX sequence (set by register END_OF_TX_WD[7:0]), then that signal will never transition high during a TX sequence. A convenient way to make sure that a signal does not assert during a TX sequence is to set its OUTPUTNAME_TX_HI[7:0]=255.

4.1.2. RX sequence generation

During the warm-up phase of an RX sequence, when the 8-bit TSM counter increments and the TSM counter equals or exceeds the programmed value of OUTPUTNAME_RX_HI[7:0] but is less than the programmed value of OUTPUTNAME_RX_LO[7:0], the corresponding TSM output will transition high.

During the warm-up or warm-down phase of an RX sequence, when the TSM counter equals or exceeds the programmed value of OUTPUTNAME_RX_LO[7:0], the TSM output will transition low.

If the programmed value of OUTPUTNAME_RX_HI[7:0] is greater than the length of an RX sequence (set by register END_OF_RX_WD[7:0]), the signal will never transition high during an RX sequence. A convenient way to make sure a signal does not assert during an RX sequence is to set its OUTPUTNAME_RX_HI[7:0]=255.

NOTE

The OUTPUTNAME in the case described in this document is GPIO2_TRIG_EN and GPIO3_TRIG_EN.

For more details about the function of the TSM module, see the *MKW41Z/31Z/21Z Reference Manual* (document MKW41Z512RM), section 45.5.2.1.

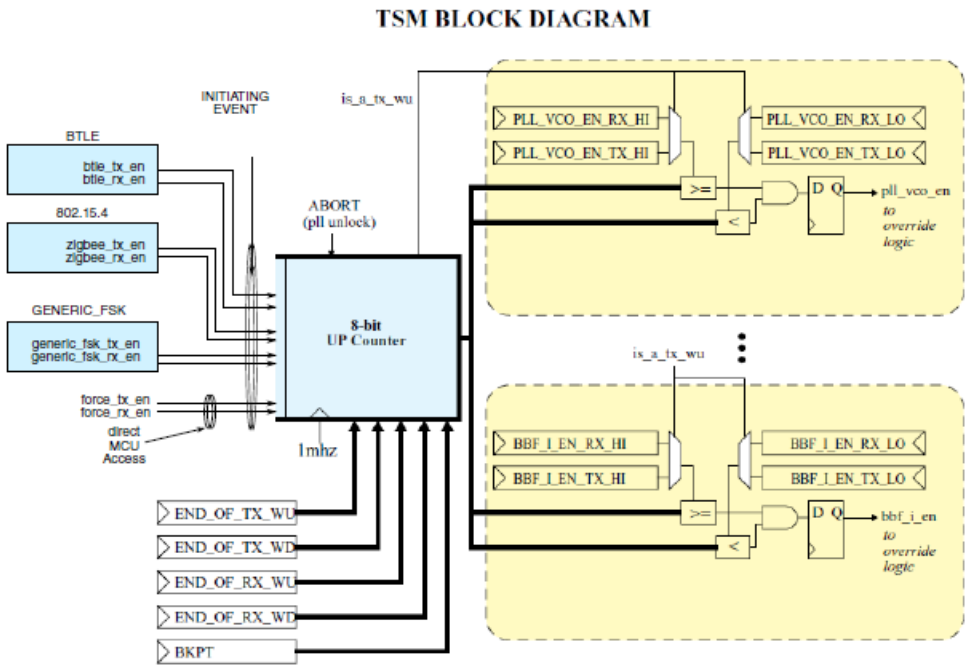

Figure 2. TSM block diagram

5. Software configurations

These ports are configured for external monitoring:

- PTB3: Protocol switching pin.
- PTC2: TX_Switch.
- PTC3: RX_Switch.

The protocol switching pin is configured to assert high/low when the transceiver switches between BLE and IEEE 802.15.4, respectively. In the hybrid application, this can be done at the MWS layer. This code snippet determines the active protocol inside the *MWS.c* file:

```
mwsStatus_t MWS_Acquire (mwsProtocols_t protocol, uint8_t force)
{
…
    if (mActiveProtocol == gMWS_802_15_4_c)
    {
        GpioClearPinOutput(&protocol_active);
    }else if (mActiveProtocol == gMWS_BLE_c)
    {
        GpioSetPinOutput(&protocol_active);
    }
}
```

NOTE

It is not always necessary to use the PTB3 as a protocol switching pin. You can configure any other GPIO as a protocol switching pin.

The GPIO TX_Switch and RX_Switch can be configured as TX/RX warm-up/warm-down to calculate the switching time. The register configurations for each phase of switching are described in these sections:

- Section 7, "Protocol switching from IEEE 802.15.4 to BLE".
- Section 8, "TX/RX switching in BLE mode".
- Section 9, "Protocol switching from BLE to IEEE 802.15.4".

The GPIO TX_Switch and RX_Switch are controlled by the gpio2_trig_en and gpio3_trig_en signals, which are the output of the TSM module. It can be configured to assert high and low using these TSM registers:

Table 1. XCVR_TSM->TIMING49

Field	Function
31-24 GPIO2_TRIG_EN_RX_LO	De-assertion time setting for GPIO2_TRIG_EN (RX) This field sets the point during a TSM RX sequence (the tsm_count[7:0] value) at which the GPIO2_TRIG_EN signal or group will transition from HI to LO.
23-16 GPIO2_TRIG_EN_RX_HI	Assertion time setting for GPIO2_TRIG_EN (RX) This field sets the point during a TSM RX sequence (the tsm_count[7:0] value) at which the GPIO2_TRIG_EN signal or group will transition from LO to HI.
15-8 GPIO2_TRIG_EN_TX_LO	De-assertion time setting for GPIO2_TRIG_EN (TX) This field sets the point during a TSM TX sequence (the tsm_count[7:0] value) at which the GPIO2_TRIG_EN signal or group will transition from HI to LO.
7-0 GPIO2_TRIG_EN_TX_HI	Assertion time setting for GPIO2_TRIG_EN (TX) This field sets the point during a TSM TX sequence (the tsm_count[7:0] value) at which the GPIO2_TRIG_EN signal or group will transition from LO to HI.

Table 2. XCVR_TSM->TIMING50

Field	Function
31-24 GPIO3_TRIG_EN_RX_LO	De-assertion time setting for GPIO3_TRIG_EN (RX) This field sets the point during a TSM RX sequence (the tsm_count[7:0] value) at which the GPIO3_TRIG_EN signal or group will transition from HI to LO.
23-16 GPIO3_TRIG_EN_RX_HI	Assertion time setting for GPIO3_TRIG_EN (RX) This field sets the point during a TSM RX sequence (the tsm_count[7:0] value) at which the GPIO3_TRIG_EN signal or group will transition from LO to HI.
15-8 GPIO3_TRIG_EN_TX_LO	De-assertion time setting for GPIO3_TRIG_EN (TX) This field sets the point during a TSM TX sequence (the tsm_count[7:0] value) at which the GPIO3_TRIG_EN signal or group will transition from HI to LO.
7-0 GPIO3_TRIG_EN_TX_HI	Assertion time setting for GPIO3_TRIG_EN (TX) This field sets the point during a TSM TX sequence (the tsm_count[7:0] value) at which the GPIO3_TRIG_EN signal or group will transition from LO to HI.

For more details about the TSM timing registers, see the *MKW41Z/31Z/21Z Reference Manual* (document MKW41Z512RM), section 45.2.2.4.1.

By default, the TSM END OF SEQUENCE (END_OF_SEQ) register is configured with these values during the hybrid application initialization:

- END_OF_RX_WD = 0x69.
- END_OF_RX_WU = 0x68.
- END_OF_TX_WD = 0x6F.

- END_OF_TX_WU = 0x67.

For more details about the END_OF_SEQ register, see the *MKW41Z/31Z/21Z Reference Manual* (document MKW41Z512RM), section 45.2.2.4.3.1.

5.1. Configuring END_OF_SEQ register

To calculate the switching time, change the value of END_OF_RX_WD in the code as follows:

```
fsl_xcvr.h
#define END_OF_RX_WD    (END_OF_RX_WU + 2)
```

For more details about the generation of waveforms using the TSM register configurations and the END_OF_SEQ registers, see Section 4.1, "TSM and END_OF_SEQ registers".

Figure 3 describes the above change:

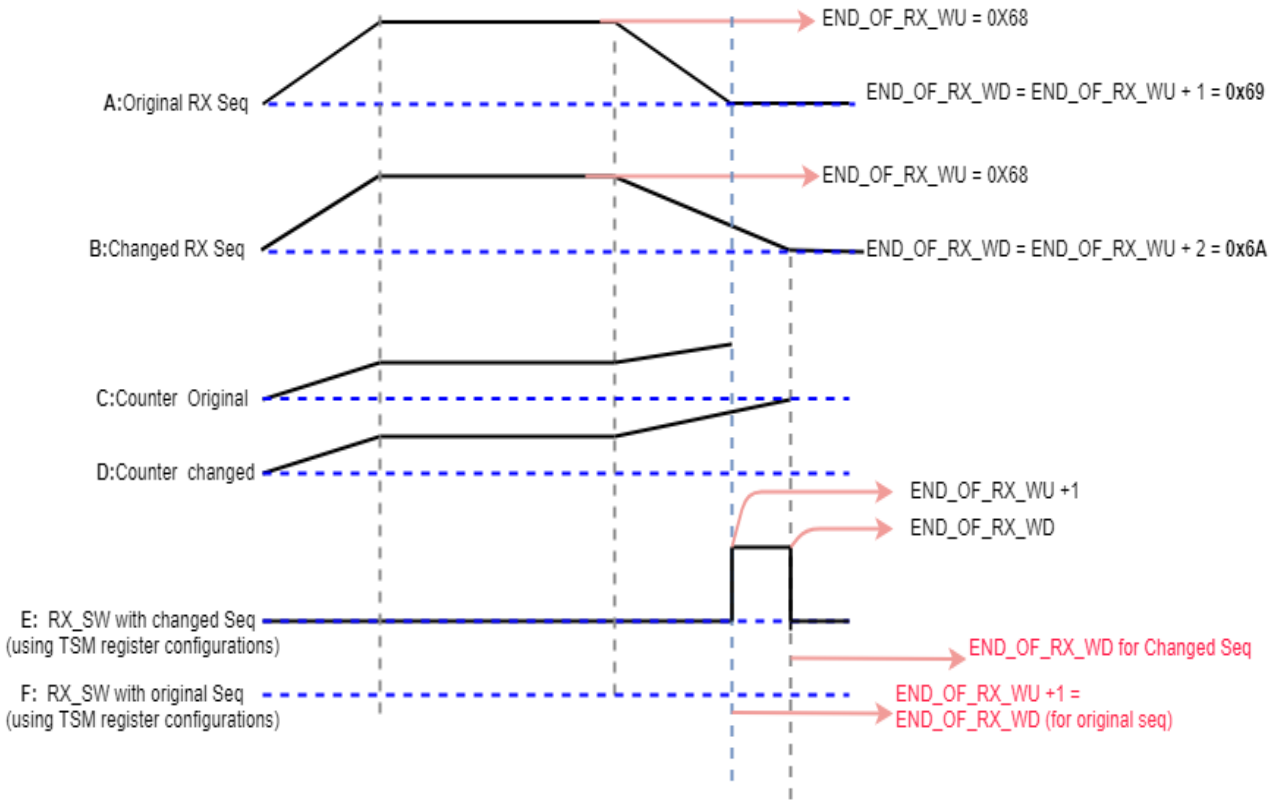

Figure 3. Generating RX warm-down waveform

To generate the RX warm-down waveform using the TSM register configurations on the RX_SWITCH GPIO, configure GPIO3_TRIG_EN_RX_HI = END_OF_RX_WU +1 and GPIO3_TRIG_EN_RX_LO = END_OF_RX_WD as the counter starts incrementing again from the END_OF_RX_WU value at the start of the warm-down phase and increments up to END_OF_RX_WD. As per the original values of the END_OF_SEQ registers, END_OF_RX_WD = END_OF_RX_WU +1. To generate the RX warm-down, configure the following:

- GPIO3_TRIG_EN_RX_HI = END_OF_RX_WU +1 = END_OF_RX_WD.

- GPIO3_TRIG_EN_RX_LO = END_OF_RX_WD.

See the “F” waveform in Figure 3.

The RX switch output transits high at the GPIO3_TRIG_EN_RX_HI value and low at GPIO3_TRIG_EN_RX_LO. GPIO3_TRIG_EN_RX_HI = GPIO3_TRIG_EN_RX_LO, so it cannot generate the RX warm-down waveform.

To generate the RX warm-down waveform, GPIO3_TRIG_EN_RX_LO - GPIO3_TRIG_EN_RX_HI = 2. To achieve this condition, modify the END_OF_SEQ register value END_OF_RX_WD = END_OF_RX_WU + 2. (see the “B” and “E” waveforms in Figure 3).

The updated values of the END_OF_SEQ registers are:

- END_OF_RX_WD = 0x6A.
- END_OF_RX_WU = 0x68.
- END_OF_TX_WD = 0x6F.
- END_OF_TX_WU = 0x67.

6. TSM register configurations explanation

The calculation of the switching time requires the generation of these waveforms:

1. Protocol switching.
2. TX warm-up/warm-down.
3. RX warm-up/warm-down.

The generation of the protocol switching waveforms is described in Section 5, “Software configurations”. The TX/RX warm-up/warm-down time is configured in these registers:

- END_OF_RX_WD, END_OF_RX_WU, END_OF_TX_WD, and END_OF_TX_WU.
- On FRDM-KW41Z, there is no GPIO that directly gives the output of any of the above-mentioned registers. To replicate the output of the above-mentioned registers as a waveform, the TSM registers (TIMING49 and TIMING50) that give the output at the GPIO (TX_SWITCH and RX_SWITCH) are used. The configuration of the TSM registers is done using the values of the TX/RX warm-up/warm-down.

The waveform generation at the GPIO (as per the configuration of the TSM register) is described in detail in Section 4.1, “TSM and END_OF_SEQ registers”.

6.1. Warm-up phase configuration

To generate the TX warm-up waveform at gpio2_trig_en (which can be seen at the TX_Switch GPIO), the waveform must transit high at the start of the TX warm-up, remain in the high state, and transit low at the end of the TX warm-up phase. The width of the waveform in a high state shall give you the value of the TX warm-up time.

- TX warm-up time = END_OF_TX_WU.

As described in Section 4.1.1, “TX sequence generation”, program the GPIO2_TRIG_EN_TX_HI = 1 so that the waveform generated at TX_Switch transits high when the TSM counter equals 1 (which

indicates the initiating event) and low when the TSM counter reaches GPIO2_TRIG_EN_TX_LO (which is programmed with the value in END_OF_TX_WU).

The waveform for the TX sequence is generated so that registers GPIO2_TRIG_EN_RX_HI and GPIO2_TRIG_EN_RX_LO are programmed with 255, as described in Section 4.1.2, "RX sequence generation". This results in the values mentioned in Section 6.1.1, "Register configuration for TX warm-up phase" for the TSM register.

The same logic applies to the RX warm-up phase, but, for the RX sequence waveform, configure the values of GPIO3_TRIG_EN_RX_HI = 1 , GPIO3_TRIG_EN_RX_LO = END_OF_RX_WU, GPIO3_TRIG_EN_TX_HI, and GPIO3_TRIG_EN_TX_LO as 255, which results in the values for the TSM register mentioned in Section 6.1.2, "Register configuration for RX warm-up phase". The output waveform for this is at the RX_Switch GPIO.

6.1.1. Register configuration for TX warm-up phase

At an initiating event, the TSM counter starts incrementing and counts up to the END_OF_TXWU value. The TSM output gpio3_trig_en asserts high at the GPIO3_TRIG_EN_TX_HI point and de-asserts at the GPIO3_TRIG_EN_TX_LO value to assert the RX switch output (controlled by the TSM timing register 50) high at the start of the TX warm-up phase and de-assert low at end of the TX warm-up phase:

- GPIO2_TRIG_EN_TX_HI = 1.
- GPIO2_TRIG_EN_TX_LO = END_OF_TXWU.

This leads to the following value to be configured in the TSM timing register 49:

- XCVR_TSM->TIMING49 = 0xFFFF6701.

6.1.2. Register configuration for RX warm-up phase

At an initiating event, the TSM counter starts incrementing and counts to the END_OF_RXWU value. The TSM output_gpio2_trig_en asserts high at the GPIO2_TRIG_EN_RX_HI point and de-asserts low at GPIO2_TRIG_EN_RX_LO to assert the TX switch output (controlled by the TSM timing register 49) at the start of the RX warm-up phase and de-assert at the end of the RX warm-up phase.

- GPIO2_TRIG_EN_RX_HI = 1.
- GPIO2_TRIG_EN_RX_LO = END_OF_RXWU.

This leads to the following value to be configured in the TSM timing register 49:

- XCVR_TSM->TIMING49 = 0x6801FFFF.

6.2. Warm-down phase configuration

To generate the TX warm-down waveform at gpio2_trig_en (which can be seen at the TX_Switch GPIO), the waveform must transit high at the start of the TX warm-down, remain in the high state, and transit low at the end of the TX warm-down phase. The width of the waveform in the high state shall give the value of the TX warm-down time.

- TX warm-down time = END_OF_TX_WD - END_OF_TX_WU.

Before the TX warm-down, the TSM is in the ON phase, so that the TSM counter holds its value at the END_OF_TX_WU count. At the start of the warm-down phase, the TSM counter starts increasing its value from the last count (which is at END_OF_TX_WU) and counts to END_OF_TX_WD. As described in Section 4.1.1, "TX sequence generation", program the GPIO2_TRIG_EN_TX_HI = END_OF_TX_WU + 1 so that the waveform generated at TX_Switch transits high when the TSM counter starts incrementing its value at the start of the TX warm-down and GPIO2_TRIG_EN_TX_LO = END_OF_TX_WD to transit the TX_Switch to low at END_OF_TX_WD.

Generate the waveform for the TX sequence so that registers GPIO2_TRIG_EN_RX_HI and GPIO2_TRIG_EN_RX_LO are programmed with 255, as described in Section 4.1.2, "RX sequence generation". This results in the values mentioned in Section 6.2.1, "Register configuration for TX warm-down phase" for the TSM register.

The same logic applies to the RX warm-down phase, but, for the RX sequence waveform, configure the values of GPIO3_TRIG_EN_RX_HI = END_OF_RX_WU + 1, GPIO3_TRIG_EN_RX_LO = END_OF_RX_WD, GPIO3_TRIG_EN_TX_HI, and GPIO3_TRIG_EN_TX_LO as 255, which results in the values mentioned in Section 6.2.2, "Register configuration for RX warm-down phase" for the TSM register.

6.2.1. Register configuration for TX warm-down phase

The TSM counter is at the END_OF_TXWU value and the TSM starts counting again, when the output de-asserts and counts to the END_OF_TXWD value to assert the RX switch output (controlled by the TSM timing register 50) high at the start of the TX warm-down phase and de-assert the RX switch at the end of the TX warm-down phase.

- GPIO3_TRIG_EN_RX_HI = END OF TXWU + 1.
- GPIO3_TRIG_EN_RX_LO = END OF TXWD.

This leads to the following value to be configured in the TSM timing register 50:

- XCVR_TSM -> TIMING50 = 0XFFFF6F68.

6.2.2. Register configuration for RX warm-down phase

The TSM counter is at the END_OF_RXWU value, so the TSM starts counting again when the output de-asserts and counts to the END_OF_RXWD value to assert the RX switch output (controlled by the TSM Timing Register 50) high at the start of the RX_WARMDOWN value and de-assert the RX switch at the end of the RX_WARMDOWN value.

- GPIO3_TRIG_EN_RX_HI = END OF RXWU + 1.
- GPIO3_TRIG_EN_RX_LO = END OF RXWD.

This leads to the following value to be configured in the TSM timing register 50:

- XCVR_TSM -> TIMING50 = 0x6A69FFFF.

7. Protocol switching from IEEE 802.15.4 to BLE

In the hybrid application, the hybrid device is in the IEEE 802.15.4 RX mode by default. When the radio intends to switch to BLE, the device first receives in BLE and then transmits the BLE service characteristics to the mobile device, so the total IEEE 802.15.4-to-BLE switching time equals the start of the RX warm-down phase in IEEE 802.15.4 to the end of the RX warm-up phase in BLE. To calculate these timings, generate the RX warm-down and RX warm-up waveforms at the TX_SWITCH and RX_SWITCH GPIOs, respectively.

See Section 6.2.2, "Register configuration for RX warm-down phase" and Section 6.1.2, "Register configuration for RX warm-up phase" for the values of the TSM registers.

7.1.1. Measurements

The IEEE 802.15.4-to-BLE switching time is calculated as follows:

- IEEE 802.15.4-to-BLE switching time = IEEE 802.15.4 RX warm-down + IEEE 802.15.4 halt + XCVR switching + BLE start + BLE RX warm-up.

The test steps are:

1. Start the IEEE 802.15.4 network. By default, the IEEE 802.15.4 is in the RX mode, hence the radio is in the IEEE 802.15.4 RX ON phase.
2. Start the BLE advertising on the hybrid device to start switching between IEEE 802.15.4 and BLE.
3. Observe the waveforms on the oscilloscope.

RX warm-down time = END_OF_RX_WD (104 µs) – END_OF_RX_WU (106 µs) = 2 µs.

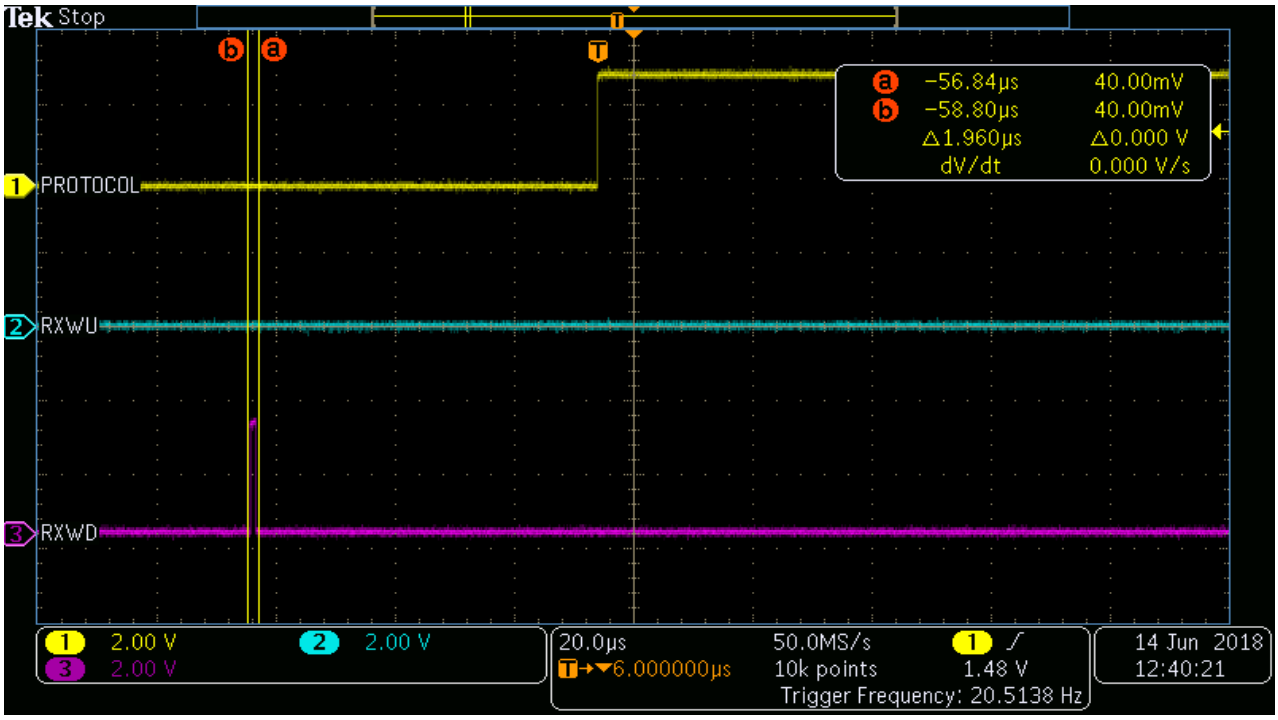

Figure 4. RX warm-down

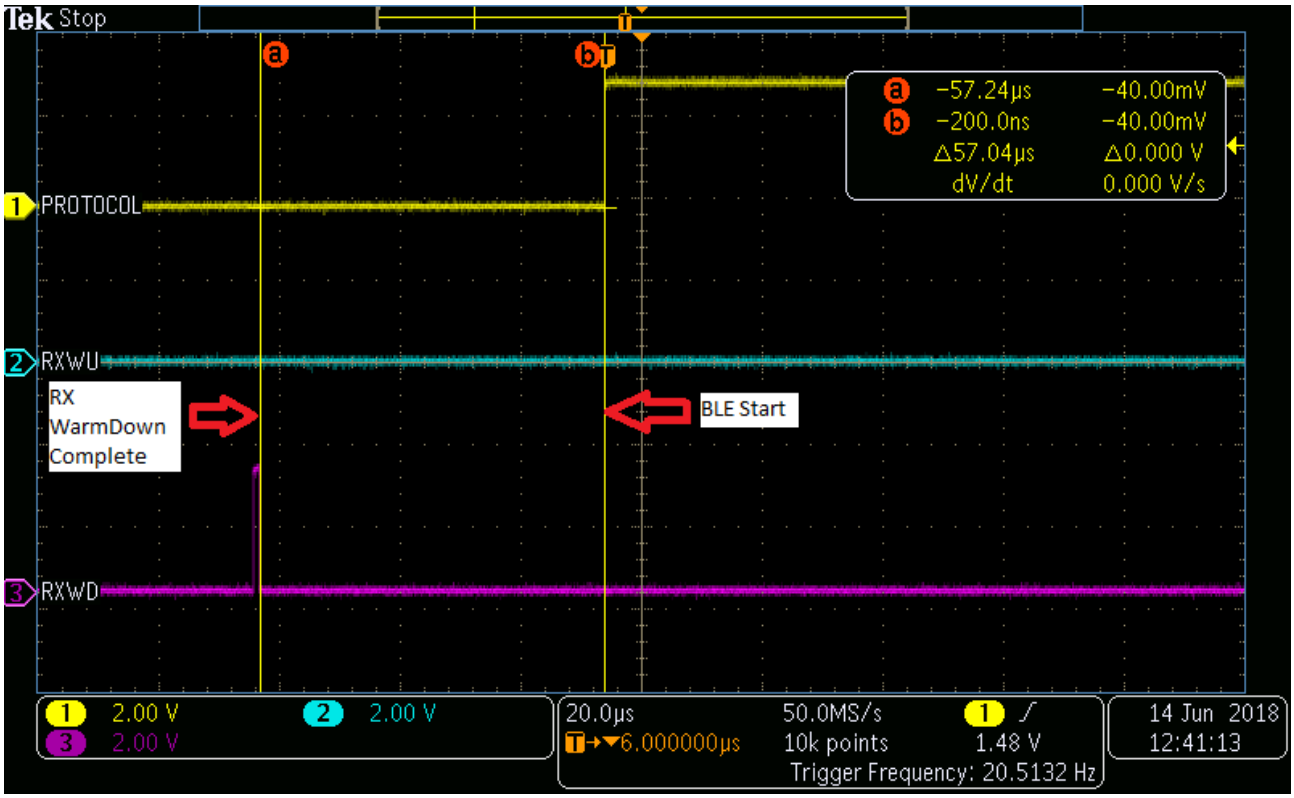

Figure 5. 802.15.4 halt + XCVR switch

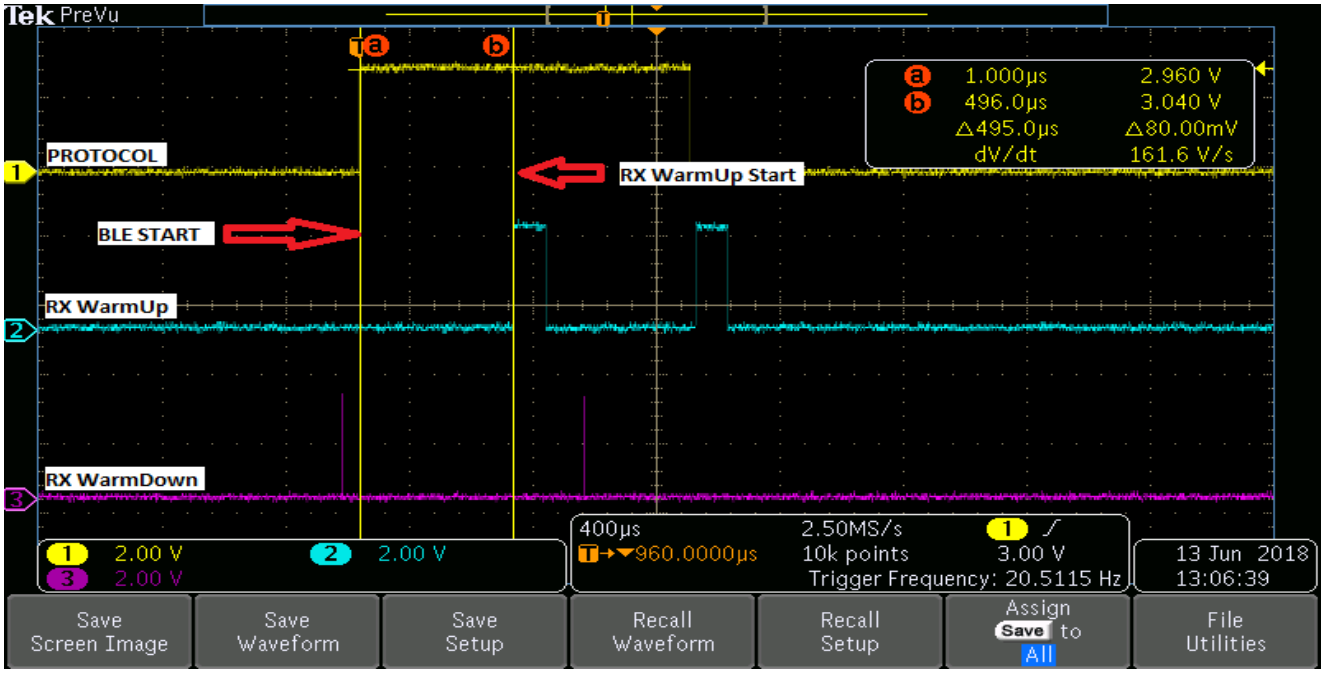

Figure 6. BLE start

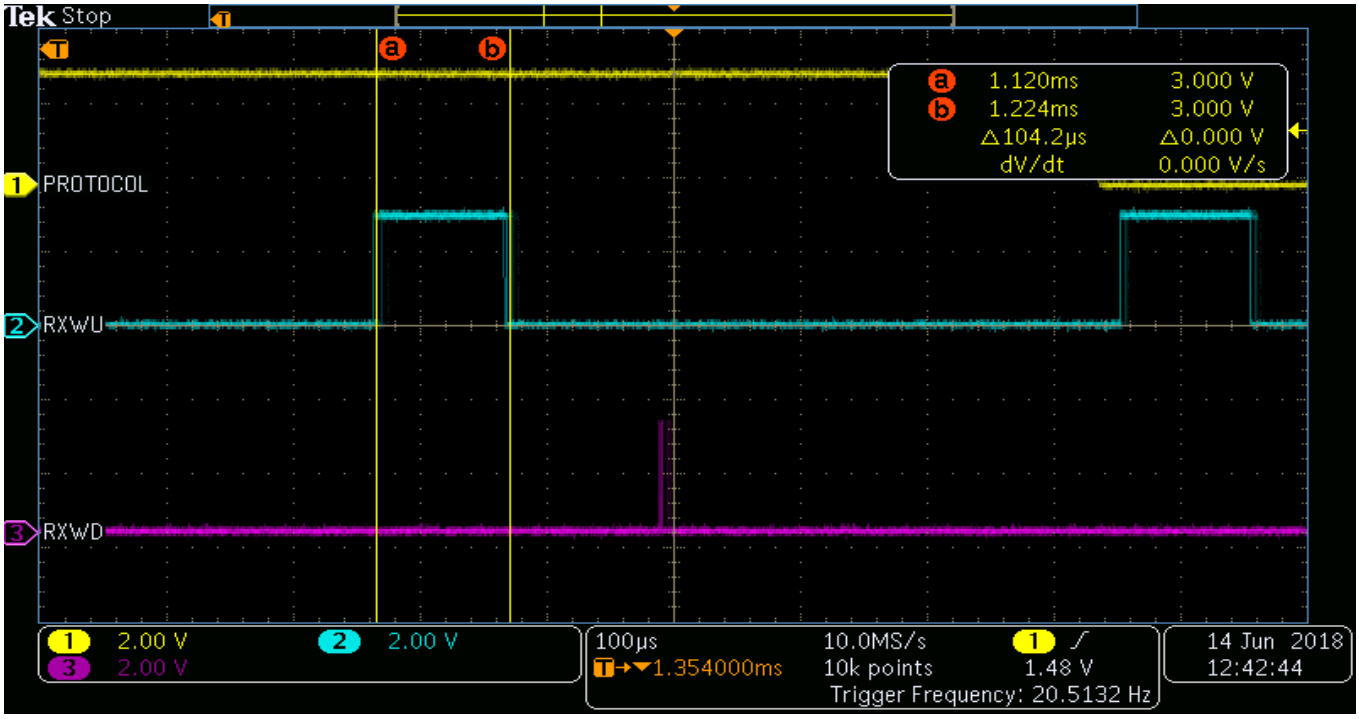

Figure 7. RX warm-up phase

8. TX/RX switching in BLE mode

When the radio switches from IEEE 802.15.4 to BLE, the BLE always starts in the RX mode and then switches to the TX mode to transmit the BLE service characteristics to the remote device. The TX/RX switching time in the BLE mode equals the addition of the BLE RX time, switching from RX to TX and BLE TX time.

8.1. Calculating BLE RX time

To calculate the RX time in the BLE mode, generate the RX warm-down and RX warm-up waveforms at the TX_SWITCH and RX_SWITCH GPIOs, respectively.

See Section 6.2.2, “Register configuration for RX warm-down phase” and Section 6.1.2, “Register configuration for RX warm-up phase” to configure the values of the TSM registers.

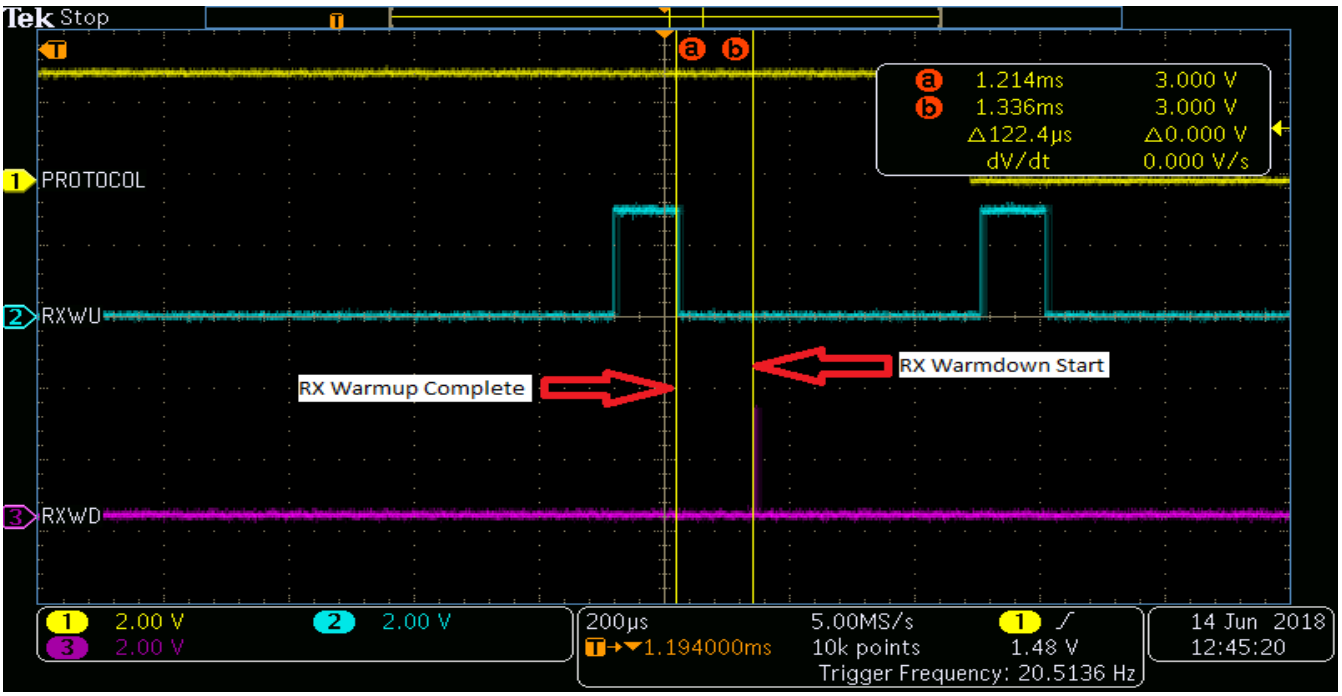

Figure 8. BLE RX

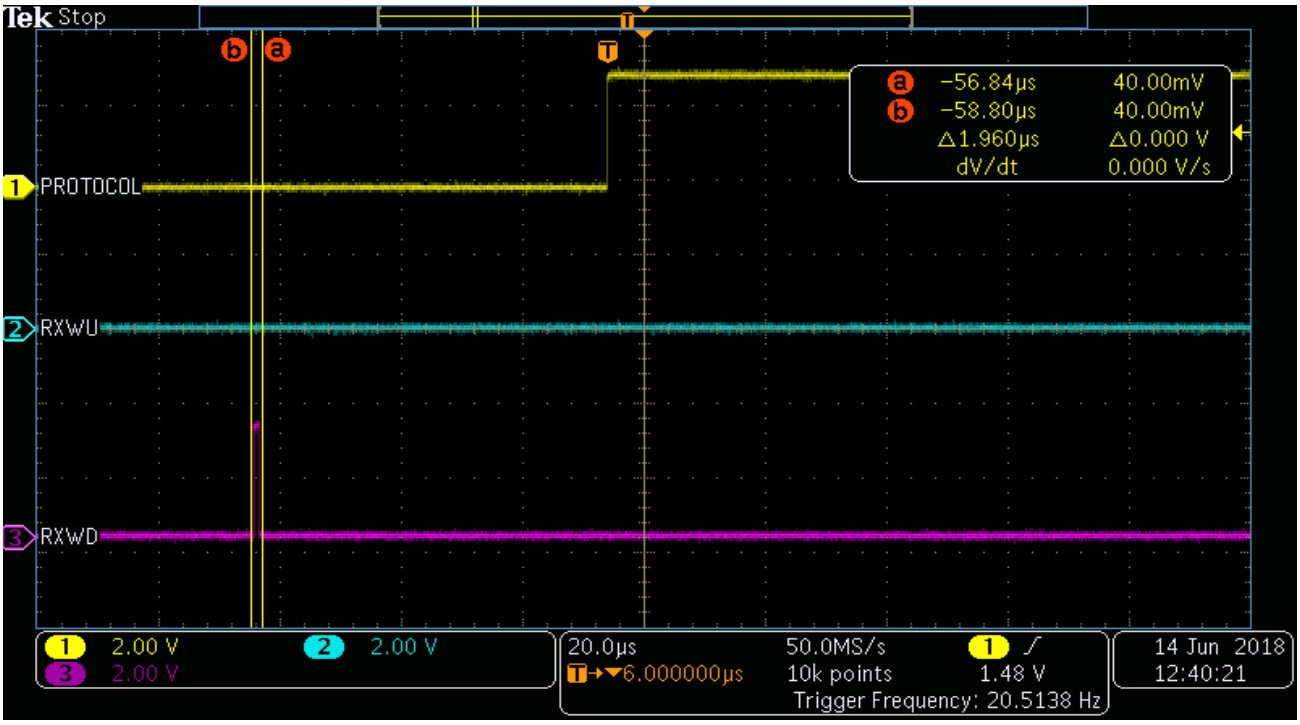

Figure 9. RX warm-down

8.2. Calculating BLE RX to TX switching time

At the switching phase from BLE to IEEE 802.15.4, the radio is in the TX mode and after switching to IEEE 802.15.4, it is in the RX mode. The total switching time from BLE to IEEE 802.15.4 equals the start of the RX warm-down in BLE to the end of the RX warm-up in IEEE 802.15.4. To calculate this timing, generate the RX warm-down and TX warm-up waveforms at the TX_SWITCH and RX_SWITCH GPIOs, respectively.

See Section 6.2.2, "Register configuration for RX warm-down phase" and Section 6.1.1, "Register configuration for TX warm-up phase" to configure the values of the TSM registers.

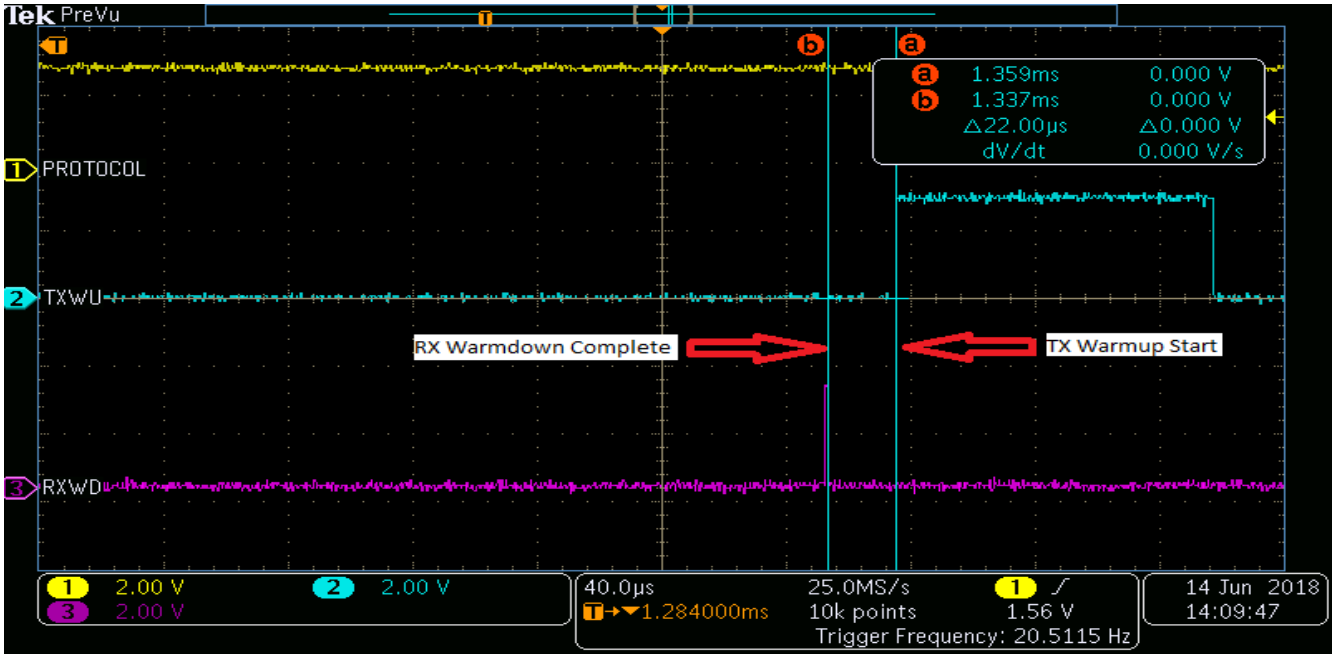

Figure 10. BLE RX to TX switching time

8.3. Calculating BLE TX time

To calculate this timing, generate the TX warm-down and TX warm-up waveforms at the TX_SWITCH and RX_SWITCH GPIOs, respectively.

See Section 6.2.1, "Register configuration for TX warm-down phase" and Section 6.1.1, "Register configuration for TX warm-up phase" to configure the values of the TSM registers.

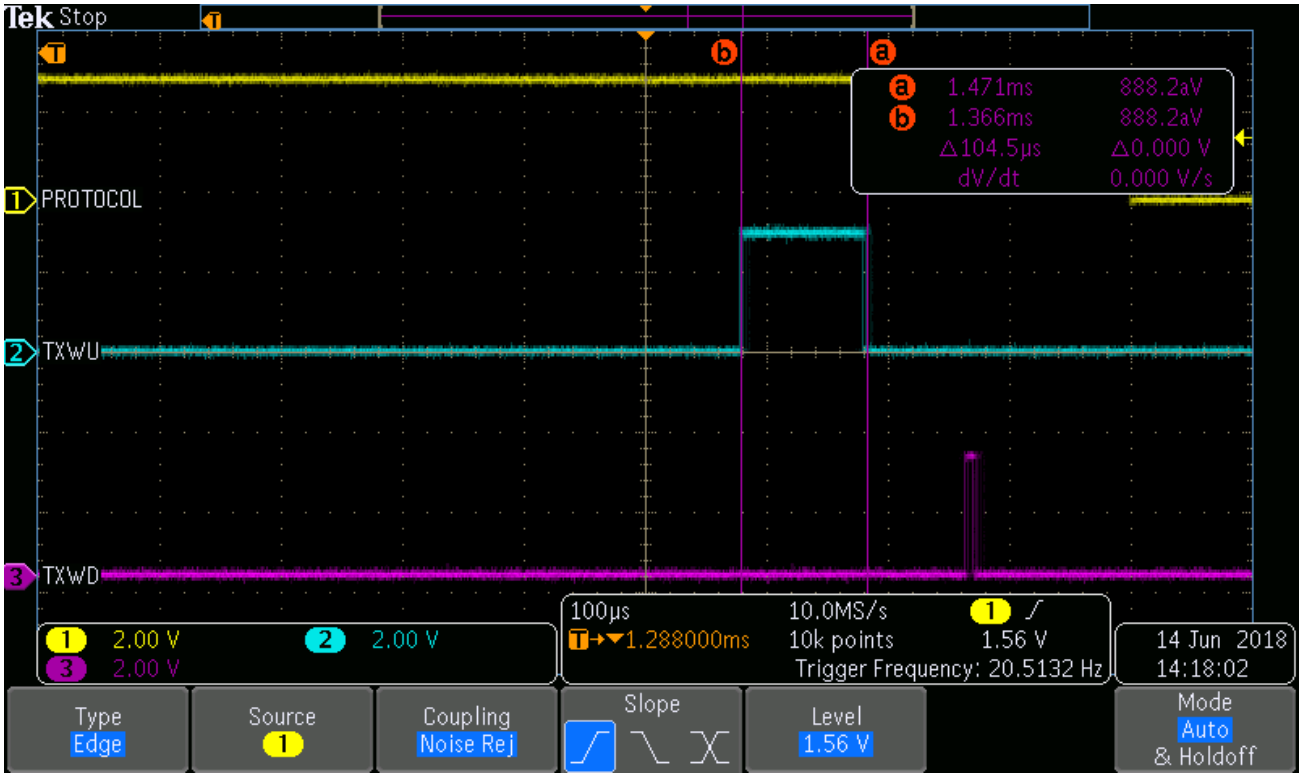

Figure 11. TX warm-up time

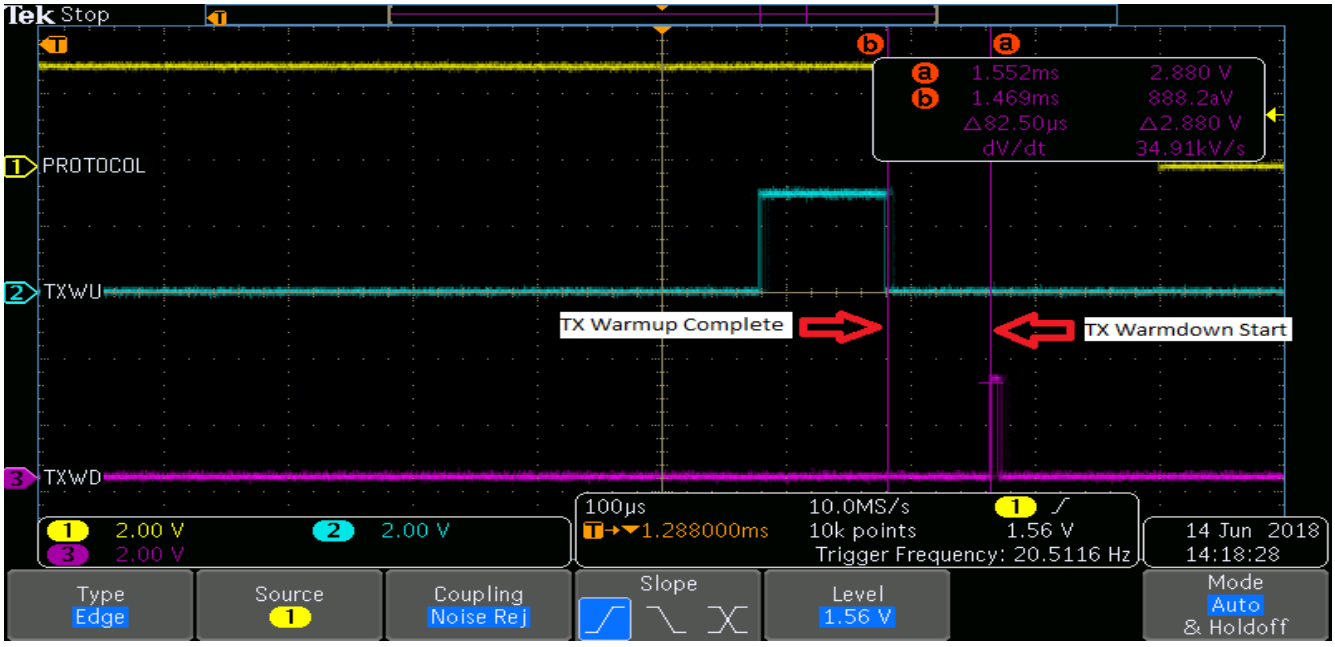

Figure 12. BLE TX time

9. Protocol switching from BLE to IEEE 802.15.4

When the radio switches from BLE to IEEE 802.15.4, the BLE is in the TX mode, because the hybrid device transmits the BLE service characteristics to the mobile device. After switching to IEEE 802.15.4, it is in the RX mode (by default, IEEE 802.15.4 is in the RX mode). The total BLE-to-IEEE 802.15.4 switching time equals the start of the TX warm-down state in BLE to the end of the RX warm-up state in IEEE 802.15.4. To calculate these timings, generate the RX warm-up and TX warm-down waveforms at the TX_SWITCH and RX_SWITCH GPIOs, respectively.

See Section 6.1.2, "Register configuration for RX warm-up phase" and Section 6.2.1, "Register configuration for TX warm-down phase" to configure the values of the TSM registers.

9.1. Measurements

The BLE-to-IEEE 802.15.4 switching time is calculated as follows:

- BLE-to-IEEE 802.15.4 switching time = BLE TX warm-down + BLE halt + XCVR switching + IEEE 802.15.4 start + end of RX warm-up.

Here are the test steps:

1. Start the IEEE 802.15.4 network. By default, IEEE 802.15.4 is in the RX mode. Hence, the radio is in the IEEE 802.15.4 RX ON phase.
2. Start the BLE advertising. The application starts to switch between IEEE 802.15.4 and BLE.
3. Create a connection between the host and the client.
4. Observe the waveforms on the oscilloscope.

TX warm-down time = END_OF_TX_WD (111 µs) – END_OF_TX_WU (103 µs) = 8 µs.

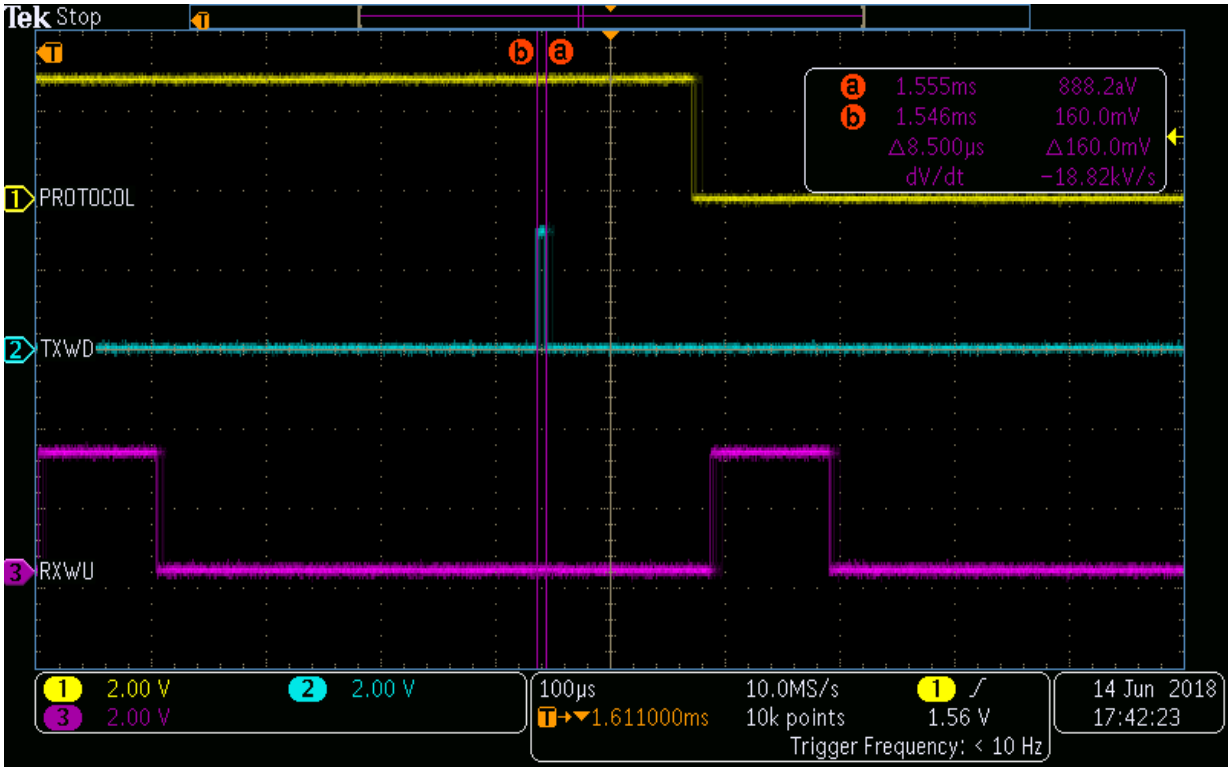

Figure 13. TX warm-down phase

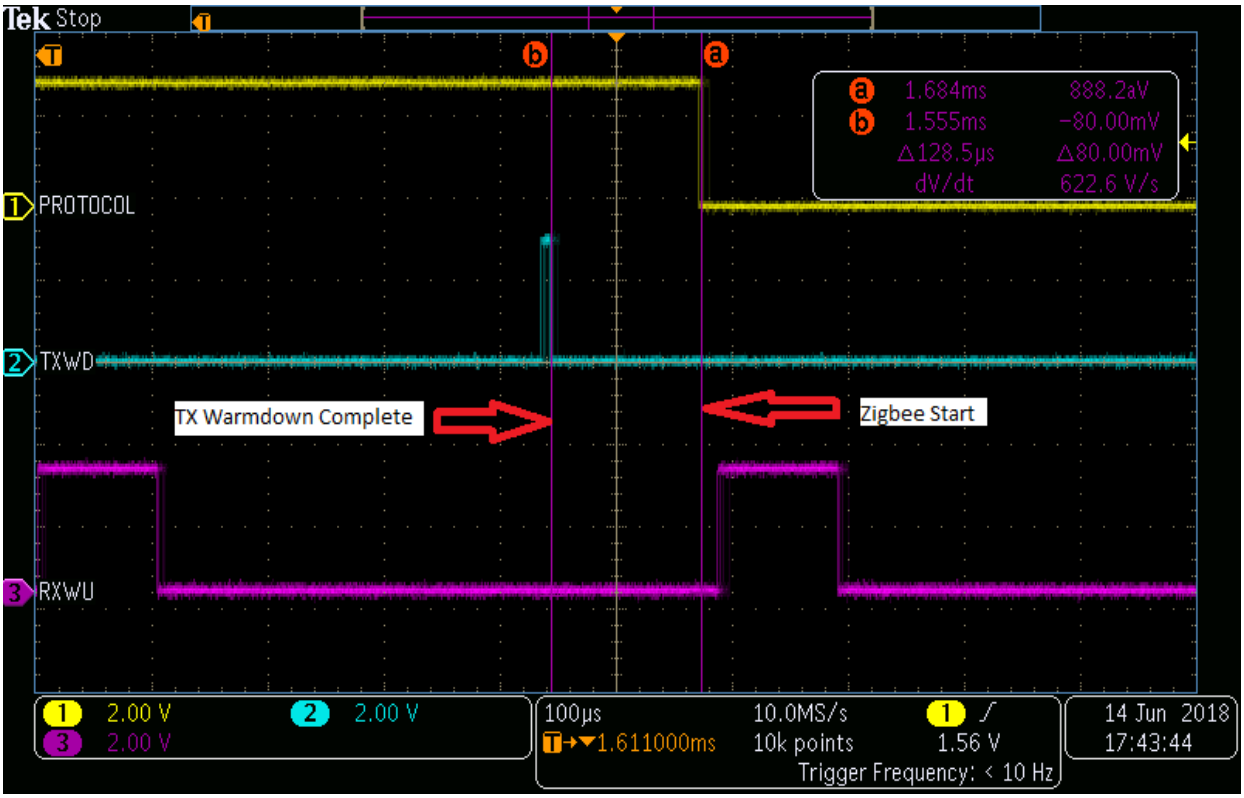

Figure 14. BLE halt phase

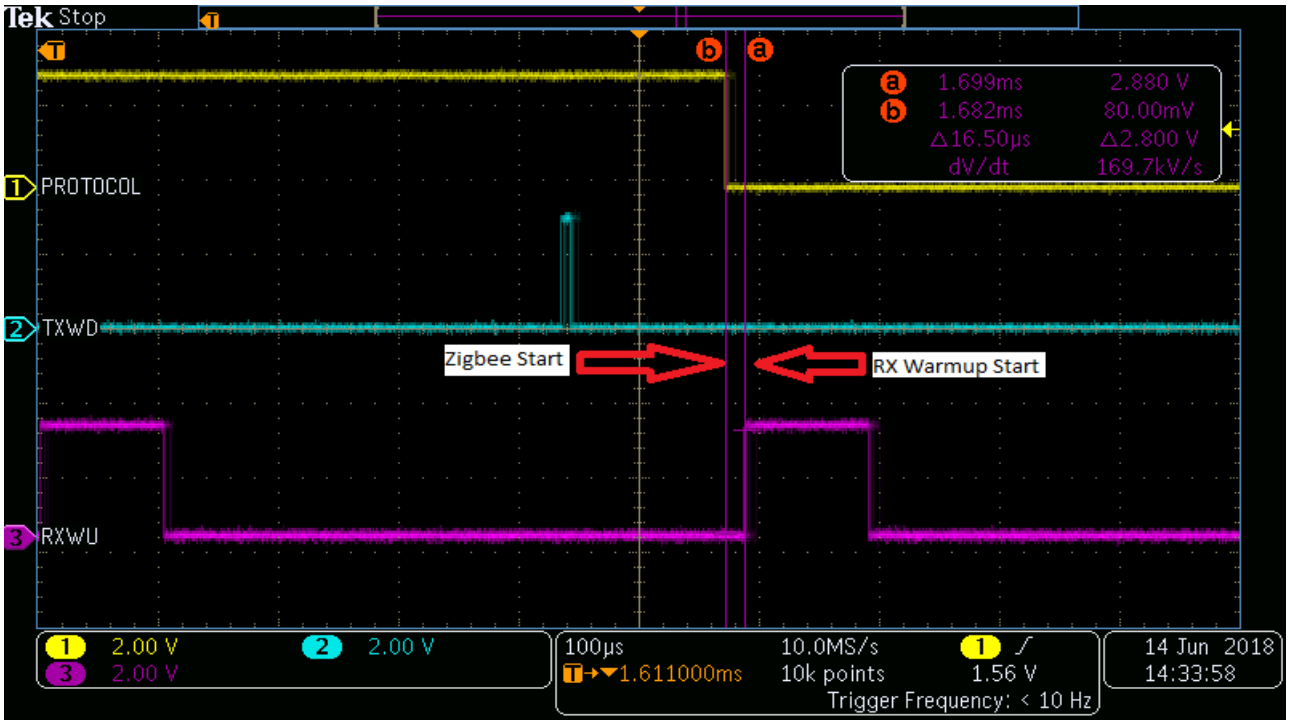

Figure 15. XCVR switch + 802.15.4 start

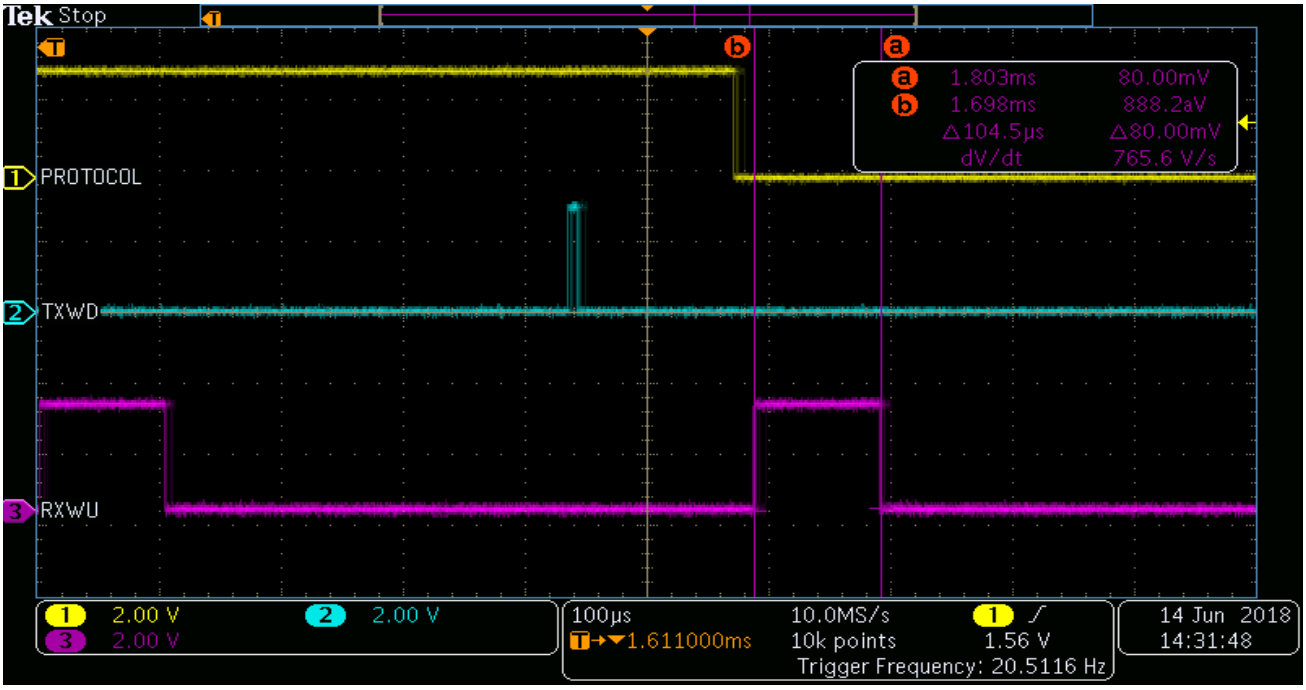

Figure 16. RX warm-up phase

10. Conclusion

The KW41Z MCU supports multi-protocol coexistence in a single chip. By default, the hybrid device is in the IEEE 802.15.4 mode. When you initiate BLE on the device, the KW41Z radio starts to switch between IEEE 802.15.4 and BLE. After that, BLE takes the priority over IEEE 802.15.4 to maintain the connection synchronization. The BLE TX and RX duration is not included in the summary diagram because it changes according to the payload. This document describes the procedure to measure the protocol switching time on a BLE/IEEE 802.15.4 hybrid device using different signals to monitor and measure each transition.

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