AN12988

PN7160 hardware design guide

Rev. 1.5 — 13 January 2023 Application note

Document information

Information	Content
Keywords	PN7160 hardware design guide, power modes, clock, IC interfaces
Abstract	This document is intended to provide an overview on how to integrate the NFC contactless frontend from hardware perspective. It presents the different hardware design options offered by the IC and provides guidelines on how to select the most appropriate ones for a given implementation. This document highlights the different IC power states and how to operate them in order to minimize the average power consumption.

Revision history

Rev	Date	Description
1.5	20230112	• PMU Clarification - CFG1, CFG2 (with/without DC-DC converter), EMI Optimization • The master/slave replacement into controller/target in this document follows the recommendation of the NXP - I2C standards organization.
1.4	20210928	TVDD pin renamed as VDD(TX) to align with data sheet
1.3	20210913	Security status changed into "Company public", no content change
1.2	20210819	• TVDD CFG1 description updated • Security status changed into "Company restricted"
1.1	20210705	Editorial updates
1.0	20210302	Initial version

1 Introduction

The PN7160 is a full feature NFC controller designed for integration in devices compliant with NFC standards (NFC Forum including NCI and EMVCo).

It is designed based on learning from previous NXP NFC device generation to ease the integration of the NFC technology in devices by providing:

- A low PCB footprint and a reduced external Bill of Material by enabling as unique feature the capability to achieve RF standards (NFC Forum, EMVCo)
- An optimized architecture for low power consumption in different modes (standby, low-power polling loop)
- A highly efficient integrated power management unit allowing direct supply from a mobile battery while a constant power (operating distance in Reader/Writer mode) for extended battery supply range (2.8 V to 5.5 V) can be achieved.
- Support of an external DC-DC converter like NXP PCA9412A, to provide more output power.

The RF contactless front-end support various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC 14443, ISO/IEC 15693, MIFARE, and FeliCa specifications. This new contactless front-end design brings a major performance step-up with on one hand a higher sensitivity and on the other hand the capability to work in active load modulation communication enabling the support of small antenna form factor (for listen mode). It also allows to provide a higher output power by supplying the transmitter output stage from 2.7 V to 5.25 V. This NFC controller provides new features:

- Enhanced Dynamic LMA (DLMA) to optimize and to enhance load modulation amplitude depending on external field strength. It allows higher range communication distance in card mode.
- 5° steps for LMA phase adjustment
- Dynamic power control which allows to make use of the maximum power in reader mode without exceeding the maximum power allowed by the standard in 0 distance
- Improved receiver sensitivity
- 1.25 W output transmitter power

/!\	In this document, the generic word NFCC is used to designate the PN7160.

2 Abbreviations

Acronym	Description
AN	Application note
BOM	Bill of material
CFG	Configuration
CLK	Clock
DWL_REQ	Download Request pin
EEPROM	Electrically Erasable Programmable Read Only Memory
GND	Ground
GPIO	General Purpose Input Output
HW	Hardware
I²C	Inter-Integrated Circuit (serial data bus)
IC	Integrated Circuit
IO	Input / Output
IRQ	Interrupt Request
mA	milliampere
MHz	Megahertz
mW	milliwatt
NFC	Near Field Communication
NFCC	Near Field Communication Controller
PMU	Power Management unit
RF	Radiofrequency
RST	Reset
SPI	Serial Peripheral Interface
VEN	V ENable pin (PN7160 Hard reset control)

3 References

[I2C] I2C bus specification and user manual Rev 03, defined by NXP. Last revision from June 2007 can be found here: http://ics.nxp.com/support/documents/interface/pdf/i2c.bus.specification.pdf

[SPI] SPI Block Guide, Freescale — [V04.0114 July2004]

User manual - UM11495 PN7160 NFC controller

Product data sheet - PN7160_PN7161 Near Field Communication (NFC) controller

Application note - AN13219 PN7160 Antenna design and matching guide

Application note - AN13287 PN7160 Linux porting guide

4 NFCC interfaces

The purpose of this chapter is to give an overview of the NFCC interfaces and to show how the chip is interconnected to the external world.

The PN7160 provides the following interfaces:

- Host interface
- Clock interface
- Power interface
- Antenna interface

Table 1. PN7160 interface summary

Interface	Short description	Options
Host interface	Link PN7160 with host controller	• I^2C, SPI • IRQ • VEN • DWL_REQ
Clock interface	Input clock needed by the PN7160 when generating RF field	• XTAL based • External clock based
Power interface	Interface to PN7160 power management unit	• CFG1 • CFG2 - DC-DC is not used • CFG2 - DC-DC is used
Antenna interface	Link PN7160 to an NFC antenna in order to enable communication with a remote contactless device	

5 Typical application schematics

The purpose of this chapter is to propose application schematics for PN7160 IC.

5.1 PN7160 HVQFN40

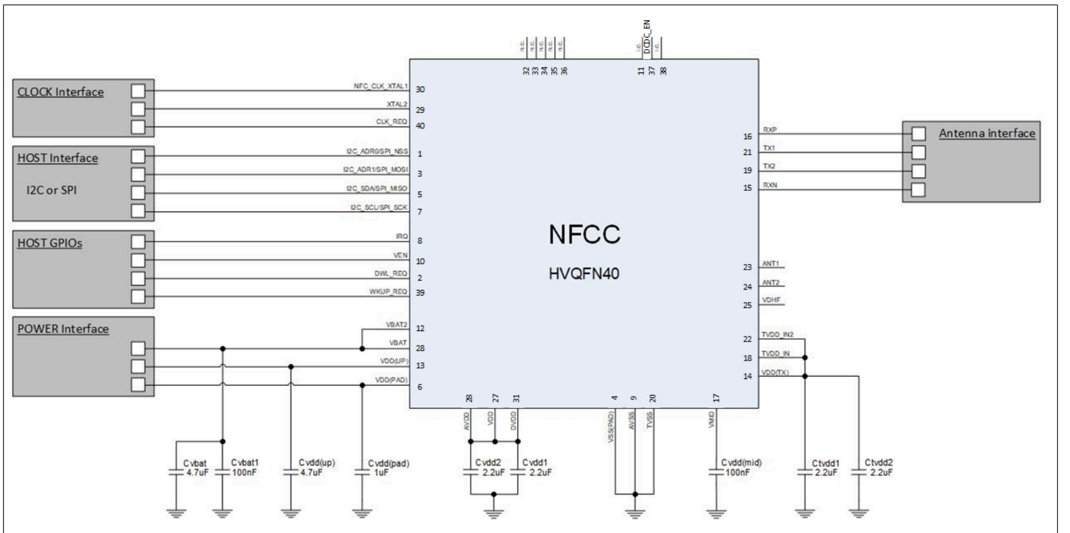

Figure 1. PN7160 version HVQFN40 Typical Application

/!\	Since the signal TX_PWR_REQ is not available on the HVQFN package variant. The DCDC_EN (37) pin can be used as an alternative.

5.2 PN7160 VFBGA64

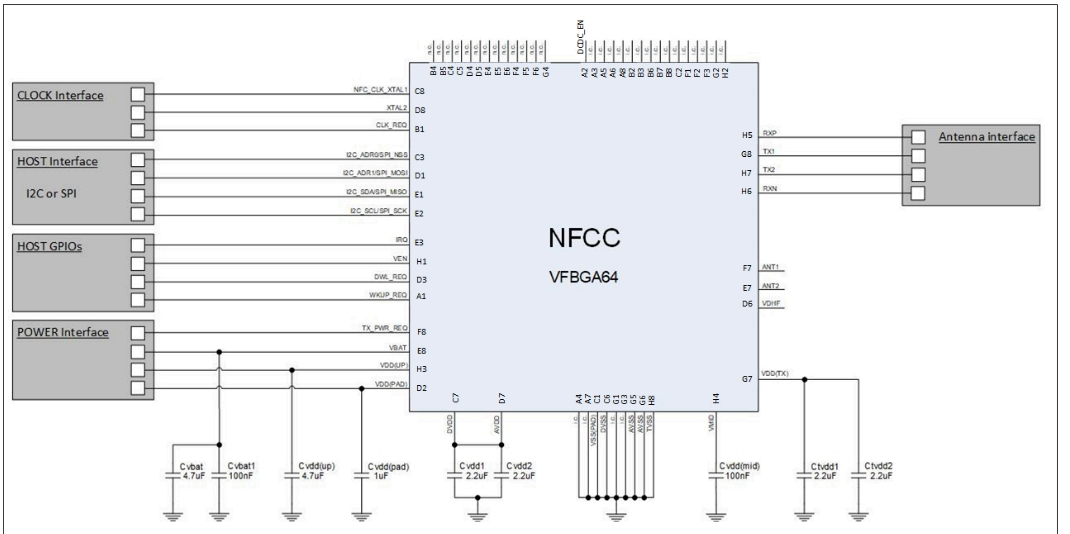

Figure 2. PN7160 version VFBGA64 Typical Application

/!\	The DCDC_EN (A2) pin can be used as an alternative to the pin TX_PWR_REQ (F8).

6 NFC controller host interface

2 host interfaces are available:

- I^2C interface
- SPI interface

/!\	Note that the host interface (SPI, I^2C) used by the PN7160 is configured during chip production. A separate ordering number is assigned to each host interface.

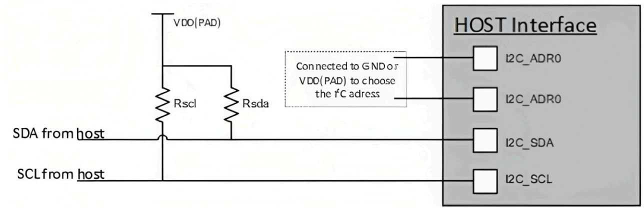

Figure 3. I^2C interface

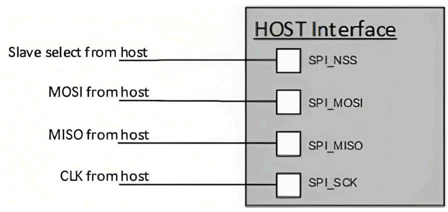

Figure 4. SPI interface

PN7160 is intended to be connected to a host controller, from a hardware point of view the interface can be an I^2C or a SPI link.

An IRQ pin is used by the NFCC chip to inform the host that a message must be read (for more detail see Section 7.1).

6.1 Host interface connection

The selection between both interfaces is configured during IC manufacturing so there are different ordering numbers for the I^2C version and the SPI version of the PN7160. See the table below.

Table 2. PN7160/61 Configurations

Part Number	Specification	Control Interface	Package
PN7160A1EV/C100	Standard Product	I^2C	VFBGA64
PN7160A1HN/C100			HVQFN40
PN7160B1EV/C100		SPI	VFBGA64
PN7160B1HN/C100			HVQFN40
PN7161A1EV/C100	Same as PN7160 + Apple ECP	I^2C	VFBGA64
PN7161A1HN/C100			HVQFN40

Table 2. PN7160/61 Configurations*...continued*

Part Number	Specification	Control Interface	Package
PN7161B1EV/C100		SPI	VFBGA64
PN7161B1HN/C100			HVQFN40

Therefore, no board level configuration is needed to select the host interface which will be used by the chip.

The following pinning assignment applies based on the selected interface:

Table 3. PN7160 VFBGA - Host interface pinning

Interface Pin	HIF1 C3	HIF2 D1	HIF3 E2	HIF4 E1
I^2C	I^2C_ADR0	I^2C_ADR1	SCL	SDA
SPI	SPI_NSS	SPI_MOSI	SPI_SCK	SPI_MISO

Table 4. PN7160 HVQFN - Host interface pinning

Interface Pin	HIF1 #5	HIF2 #7	HIF3 #1	HIF4 #3
I^2C	SDA	SCL	I^2C_ADR0	I^2C_ADR1
SPI	SPI_MISO	SPI_SCK	SPI_NSS	SPI_MOSI

6.2 I^2C bus specificities

Target address:

In the case where I^2C is the selected host interface, the chip answers to a given I^2C target address.

This is determined by the combination of a base address and the logical state of I^2C_ADR0 and I^2C_ADR1 pins:

b'0 1 0 1 0 I^2C_ADR1 I^2C_ADR0' where I^2C_ADR0 is the least significant bit.

For instance, if I^2C_ADR0 and I^2C_ADR1 are both tied to ground, the 7-bits target[1] address of the PN7160 is 0x28.

Table 5. I^2C target 8-bits address

I2C_ADR1 level	I2C_ADR0 level	PN7160 write address (R/W bit = 0)	PN7160 read address (R/W bit = 1)
0 (GND)	0 (GND)	0x50	0x51
0 (GND)	1 (VDD(PAD))	0x52	0x53
1 (VDD(PAD))	0 (GND)	0x54	0x55
1 (VDD(PAD))	1 (VDD(PAD))	0x56	0x57

Pullup selection:

1 The master/slave replacement into controller/target in this document follows the recommendation of the NXP - I2C standards organization.

Pullup resistors to VDD(PAD) are required on the I^2C lines SDA and SCL. The resistors value must be selected in order to meet the I^2C timing requirements based on the line capacitance, the VDD(PAD) level and the targeted maximum I^2C clock speed.

More details can be found in the *I²C bus specification* document.

7 Host GPIOs

The PN7160 host GPIOs are directly connected to host processor GPIOs.

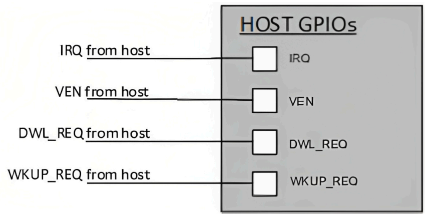

Figure 5. Host GPIOs interface

7.1 PN7160 frames reading synchronization (IRQ pin)

PN7160 answers / notifications toward the host controller are asynchronous and they can be triggered by an external event (e.g detection of a card in the RF field).

Therefore, a mechanism must be put in place so that asynchronous frames from the PN7160 are well captured by the host controller. For this, 3 implementations can be foreseen on the host controller side:

- 1- IRQ pin external interrupt
- 2- IRQ pin polling
- 3- Read polling

For "1-", connect pin IRQ of the PN7160 to an external interrupt line on the host controller side. In this case, when the PN7160 has some data available, the IRQ line will be asserted and if configured accordingly, a software interrupt is generated on the host controller side. A host interface read is then managed by the corresponding interrupt handler.

For "2-", the principle is to regularly poll the status of the IRQ pin and when it toggles, to perform a read on the host interface.

For "3-", the principle is to regularly perform some read on the host interface and to discard frames starting with the default value as in this case it would mean that no data is available from the PN7160. Default value is 0xFF in case of SPI bus. For the I^2C bus, the I^2C address will not be acknowledged in case the PN7160 does not have any meaningful data to send to the host.

/!\	Implementation "1-" is recommended

IRQ pin polarity (e.g. active high or low) is configurable with register settings. Details can be found in the *PN7160 User Manual*.

IRQ Signal Specification:

- The signal can be configured active high or active low via the NCI Configuration API, this configuration being stored in non-volatile memory
- The signal will be active anytime data is available in the PN7160 send buffer
- The pad state is maintained during the Standby mode
- The pad is configured to pull down in hard Power-down mode

7.2 Reset control (VEN Pin)

The PN7160 HW is activated using the input pin VEN. When VEN is greater than 1.1 V the PN7160 core is supplied from VBAT. For VEN lower than 0.4 V, the PN7160 is in hard power down state and the internal core of the chip is no more supplied. The chip is reset when VEN is switched back to a voltage level higher than 1.1 V.

It is strongly recommended to foresee a control of VEN pin from the host controller side so that it can reset PN7160 whenever needed.

The VEN pin state is considered as valid information only when the VDD(PAD) pad is supplied. Indeed, VEN signal is supposed to be driven by the host controller with which VDD(PAD) supply is shared. When the supply is not there, this means that the host controller is not able to drive a meaningful state on the PN7160 VEN pin.

When VDD(PAD) is not present, the level of VEN is determined thanks to a 2-bit register stored in a non-volatile memory to define if the chip is operating in hard power down state or in active mode (VEN_Pulld and VEN_Value) as depicted in Table 6.

Table 6. VEN configuration

VEN external	VDD(PAD) active	VEN_Pulldown cases	VEN_Value cases	Actual VEN internal value
0 (via host)	Y	0	X	= 0 (via Host)[2]
1 (via host)	Y	0	X	= 1 (via Host)[2]
0 (via host)	Y	1 (default)	X	= 0 (via Host)
1 (via host)	Y	1 (default)	X	= 1 (via Host)
VDD(PAD) not active = VEN via Host not defined	N	0	X	X (Undefined)[1]
	N	0	X	X (Undefined)[1]
	N	1 (default)	0	= 0 (VEN_Value)
	N	1 (default)	1	= 1 (VEN_Value)

[1] VEN_Pulld default value being 1, it is strongly recommended not to program it to 0 since, when VDD(PAD) is inactive, VEN internal value will be undefined.

[2] VEN_Pulld default value being 1, there is no added value to program it to 0 due to [1].

7.3 Download mode control (DWL_REQ Pin)

PN7160 entry in download mode is managed through the DWL_REQ pin.

Although NXP strongly advises driving this pin through the host controller, in case where download mode control is not supported, this pin must be tied to ground or left open (internal pulldown).

When the DWL_REQ pin is set to the digital high level (this pin is referenced to VDD(PAD) power level) at reset (VEN transition from digital low to digital high), the chip boots in download mode.

In this case, the download protocol described in the *PN7160 User Manual* can be used to load a new firmware image into the chip.

This firmware upgrade feature is fully supported by the NXP HAL middleware stack (Android and Linux) if the DWL_REQ (DL_REQ) pin is connected a GPIO pin of the host controller.

A comparison between the operation of the PN7160 in both download mode and normal mode is given in the diagram below:

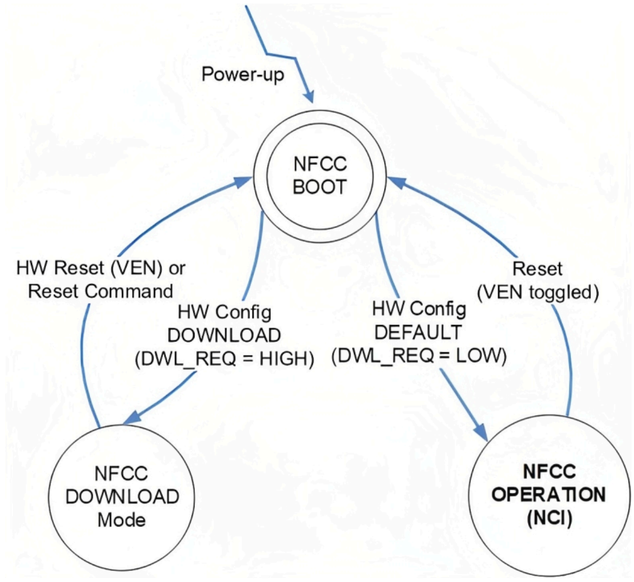

Figure 6. PN7160 download mode entry

7.4 Wake-up request pin (WKUP_REQ Pin)

When the PN7160 goes in standby mode, there is 3 possibilities to wake it up:

- PN7160 detects an external RF field
- Host controller sends a command (via host interface) to PN7160
- Host drives WKUP_REQ pin to high level

7.5 Host interface pins characteristics

Detailed characteristics of the host interface pins can be found in the *PN7160 Product datasheet*.

8 Clock interface

The PN7160 core can run without any external clock (based on an internal oscillator), however a 27.12 MHz clock is needed:

- to generate the RF field in poll mode
- to generate the ALM load modulation in listen mode

2 clock configurations can be considered:

- CLK provided by an Xtal oscillator
- CLK provided by an external source

8.1 Clock provided by an XTAL oscillator

A 27.12 MHz crystal can be used as input clock for PN7160.

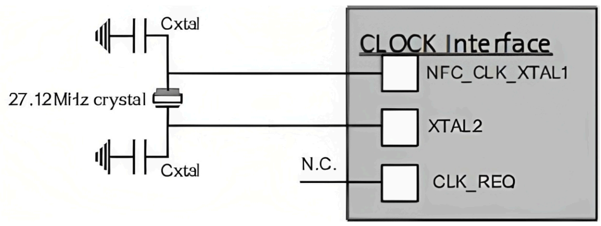

Figure 7. Clock provided by an XTAL oscillator

When using a crystal, frequency accuracy and drive level must be carefully selected according to the specification provided in the *PN7160 Product Datasheet*.

The PN7160 clock interface must be configured properly to reflect whether it is connected to a 27.12 MHz crystal oscillator or to an external clock. This is done through the NCI host interface (details can be found in *PN7160 User Manual*).

/!\	Note that the crystal-based solution is less optimized from Bill of Material perspective as it not only requires a crystal oscillator but also 2 additional decoupling capacitors on NFC_CLK_XTAL1 and XTAL2 pins. However, the crystal-based solution guarantees the same kind of performances.

8.1.1 XTAL references

PN7160 clock interface with xtal oscillator has been verified with several references as given below. Other crystal units might be suitable for the specified usage, but only the ones below have been validated by NXP.

- NDK:
  - NX2016SA 27.12 MHz EXS00A-CS06346.
  - NX2016HA 27.12 MHz EXS00A-CH00075
- MURATA
  - XRCGB27M120F3M10R0

8.1.2 XTAL layout recommendations

The XTAL must be connected as close as possible to the CLK1 and CLK2 pins from the PN7160 to achieve the best performances as possible.

Please follow these guidelines for the layout of the XTAL connections:

- As the XTAL is very sensitive to parasitic capacitance and noise, we advise to:
  - put the XTAL far from other signals (especially other CLK lines or signals with frequent switching)
  - limit the crosstalk between CLK lines and other signals
- Load capacitor connections:
  - Choose capacitor with a good temperature stability like COG
  - Place the capacitors closed to each other and close to the XTAL
  - Avoid connecting them to a dirty ground (perturbed by return current from others functionalities on the board like USB, PWM or power supply lines)

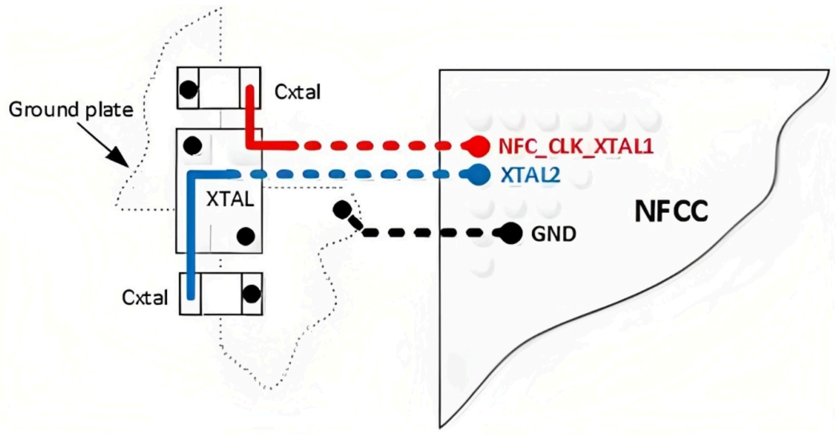

Figure 8. XTAL connection example

8.2 Clock provided by an external source

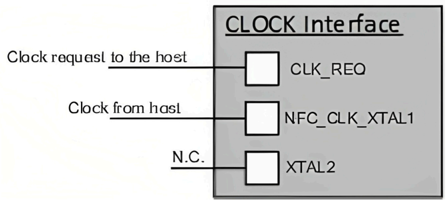

Figure 9. Clock provided by an external source

8.2.1 External clock source requirements

When an external system clock is used, the input clock frequency must be one of the following values:

- 13 MHz
- 19.2 MHz
- 24 MHz
- 26 MHz
- 32 MHz
- 38.4 MHz
- 52 MHz

For proper operation, the external clock frequency must be indicated to PN7160. This is done through the NCI host interface (details can be found in *PN7160 User Manual*).

Please note that the voltage level of the system clock signal provided to PN7160 must fulfill to data sheet (*PN7160 Product Datasheet*) requirements (voltage levels, phase noise). On top of these data sheet requirements, square shape must fulfill below requirements:

Table 7. NFC_CLK_XTAL1 square shape input clock specifications

Parameter	Min	Typ	Max
peak-to-peak voltage	0.4 V	-	1.8 V
rising/falling time	-	-	10 ns

The PN7160 input impedance on the NFC_CLK_XTAL1 pin depends on the input clock frequency (see table below).

Table 8. NFC_CLK_XTAL1 pin input impedance

Input clock frequency	Active mode		Standby or hard power mode	
	min	Max	Min	Max
13 MHz	25 kΩ	86 kΩ	49 kΩ	53 kΩ
52 MHz	5 kΩ	7.5 kΩ	12 kΩ	14 kΩ

Based on this input clock signal, the PN7160 internal PLL generates the required 27.12 MHz internal clock for field generation.

8.2.2 Clock request mechanism

In order to optimize the device power consumption, the PN7160 input clock could be provided by the system only when it is actually needed by the chip (e.g. when the PN7160 needs to generate an RF field). For this, a clock request mechanism has been put in place, only applicable when an external clock is used (not with a crystal). This is enabled via CLOCK_ REQUEST_CFG parameter, configured through the NCI host interface (details can be found in *PN7160 User Manual*).

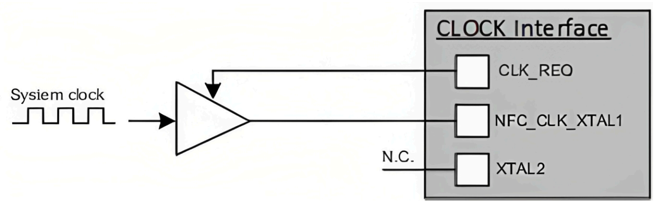

Figure 10. Clock request mechanism

When the PN7160 needs an input clock, it will toggle the CLK_REQ pin to the digital high level and keeps it high as long as the input clock is required.

It requires then a specific connection of the CLK_REQ pin which would switch on the system clock signal whenever the pin is at the digital high level and switch it off when the pin is set back to the digital low level.

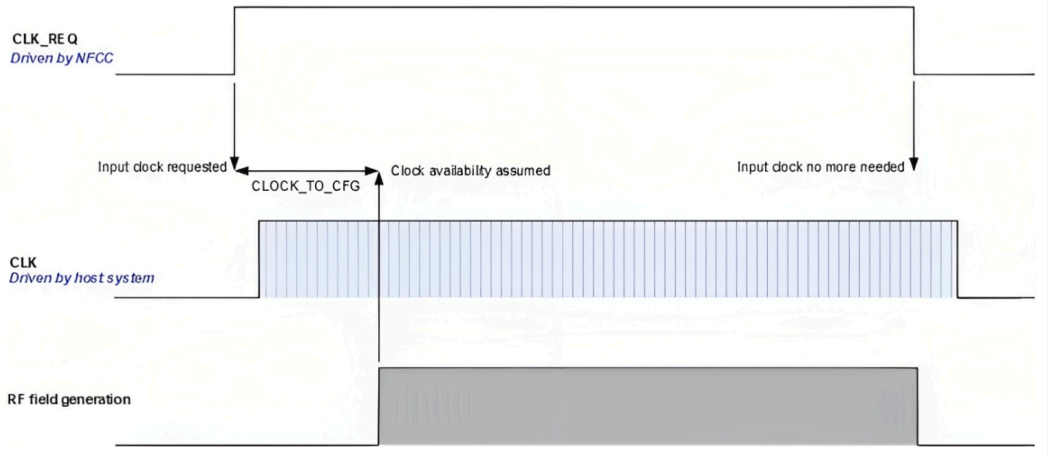

Figure 11. Clock request through CLK_REQ pin

CLOCK_TO_CFG is a timeout which can be configured through EEPROM settings. It represents the duration after PN7160 has raised its CLK_REQ pin during which the host system must provide a valid and stable clock on CLK pin.

/!\	CLK_REQ pin shall be left unconnected when not used since it is driven low

9 Power interface

9.1 External capacitors requirement

The recommended external capacitors are listed below (referring to application schematics in chapter Section 5):

Table 9. Decoupling capacitors need

Capacitor	Value	Comments
Cvdd(up)	4.7uF/7V	Voltage tolerance depends on the voltage on Vdd(up)
Cvbat	4.7uF/ 5.5V	
Cvbat1	100nF/ 5.5V	
Cvdd1	2.2uF/2V	2 *2.2uF one as close as possible of each pin (DVDD and AVDD)
Cvdd2	2.2uF/2V	
Ctvdd1	2.2uF/5.5V	2 *2.2uF are needed to avoid derating issue
Ctvdd2	2.2uF/5.5V	
Cvdd(pad)	1µF/3.3V	
Cvdd(mid)	100nF/1.8V	

A tolerance of 10 % or better is recommended for those capacitors.

/!\	Component de-rating over voltage and temperature must be carefully considered during the decoupling capacitors selection process

9.2 External power supplies

The PN7160 needs 3 external power supplies to operate.

- VBAT: This is the main power supply of the NFCC.
- VDD(PAD): This is the power supply for the host interface and GPIOs.
- VDD(UP): This is the power supply allowing to generate TXLDO.
  - VDD(TX): Output supply voltage for the transmitter. It is internally connected to the transmitter input supply voltage

Table 10. External power supplies voltage

Parameter	Min	Typ	Max	Unit
VBAT	2.8	-	5.5	V
VDD(PAD)	1.65	1.8	1.95	V
	3.0	3.3	3.6	
VDD(UP)	2.8	-	5.8	V

Typically: VDD(TX) = VDD(UP) - 0.3 V

9.3 TXLDO power level

The strength of the field emitted by the PN7160 is linked to several parameters such as the antenna geometrical characteristics, the antenna matching circuit and the voltage level on TX output buffer.

The voltage level on TX output buffer is coming from VDD(TX) and this pin is powered internally by the PN7160 thanks to the TXLDO block. The output voltage of this TXLDO can be set between 2.7 V to 5.25 V depending on the VDD(UP) voltage.

2 VDD(UP) configurations are considered:

- VDD(UP) connected to a battery (CFG1)
- VDD(UP) connected to an external supply (CFG2)
  - Supplied directly from the external power supply
  - Supplied via DC-DC converter

9.3.1 CFG1

In CFG 1, VDD(UP) and VBAT are connected to a battery (e.g., a cell phone battery). This configuration is optimized for a user case when a battery is used.

For this configuration, the battery voltage monitor " *VBAT_MONITOR_EN_CFG*" and TXLDO check "*PMU_CFG*" should be considered (See the user manual). These features can be useful for monitoring battery discharge.

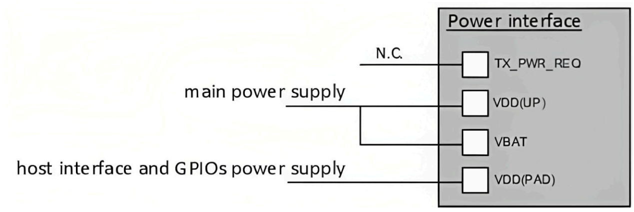

Figure 12. CFG1 - VDD(UP) and VBAT connected to a battery

In this configuration TXLDO voltage possible settings are 2.7 V, 3 V, 3.3 V, 3.6 V.

/!\	For proper operation, the VDD(TX) voltage value set shall be below the VDD(UP) - 0.3 V value. In configuration 1, the voltage is given by the battery then the higher voltages might not be usable.

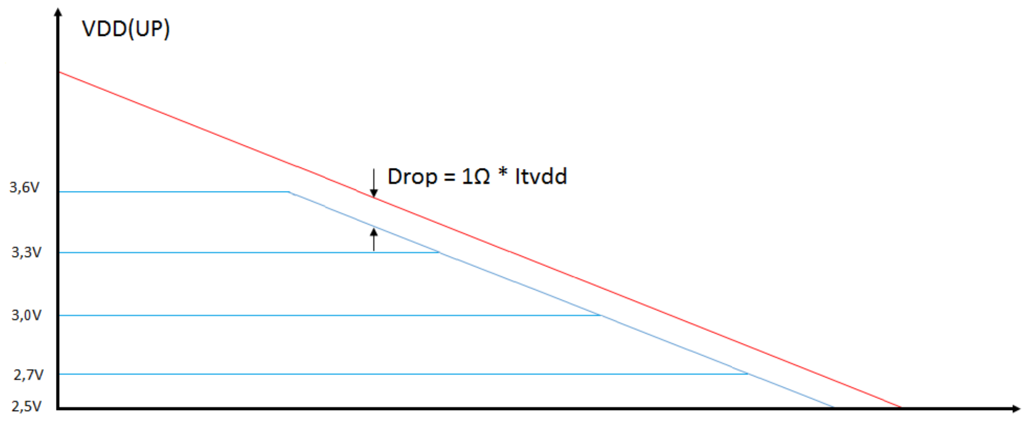

Figure 13. CFG1 - VDD(TX) behavior when supplied from VBAT

/!\	In standby state, TXLDO is always regulated @2.5V

9.3.2 CFG2 - DC-DC converter is not used

In CFG2, the VDD(UP) pin is connected to an external power supply. The internal TXLDO is used to generate configurable VDD(TX). For this configuration, the VDD(UP) and VBAT can also be connected together. This means that you can use the same voltage (e.g. 5 V or 3.3 V) from the same source.

Table 11.

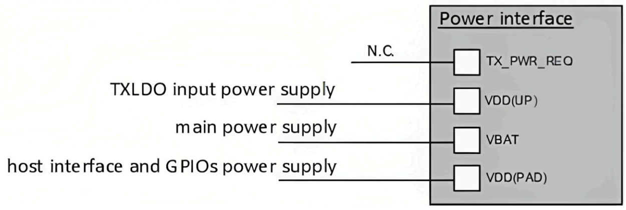

Figure 14. CFG2 - VDD (UP) and VBAT are supplied by an external voltage (DC-DC is not used)

In this configuration TXLDO voltage possible settings are 2.7 V/3 V/3.3 V/3.6 V/3.9 V/4.2 V/4.5 V/4.7 V/4.75 V/5 V/5.25 V.

Table 12.

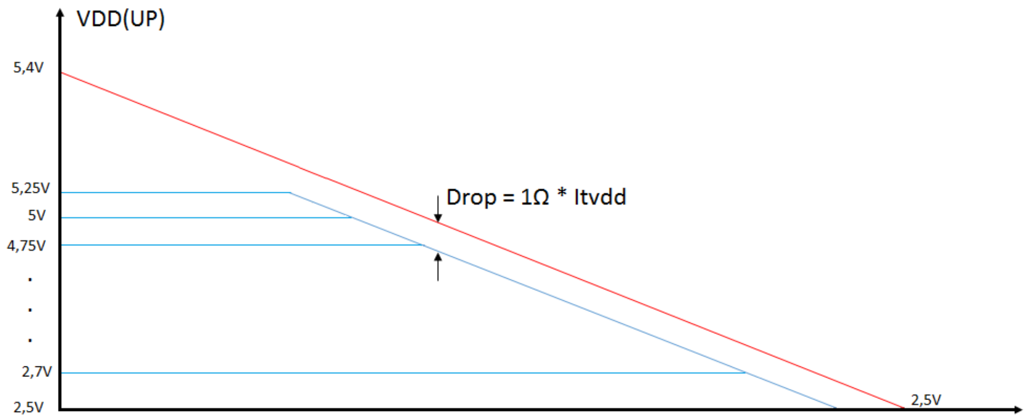

Figure 15. CFG2

/!\	For proper operation, the VDD(TX) voltage value set shall be below the VDD(UP) - 0.3 V value. The maximum VDD(UP) value is 5.8 V in configuration 2

9.3.3 CFG2 - DC-DC converter is used

In CFG2, a DC-DC converter is used in order to increase VDD(UP) voltage the main supply voltage.

NXP proposes several DC-DC references to provide the best in class performances:

- PCA9410A => output voltage =5 V
- PCA9411A => output voltage =5.25 V
- PCA9412A => output voltage =5.4 V

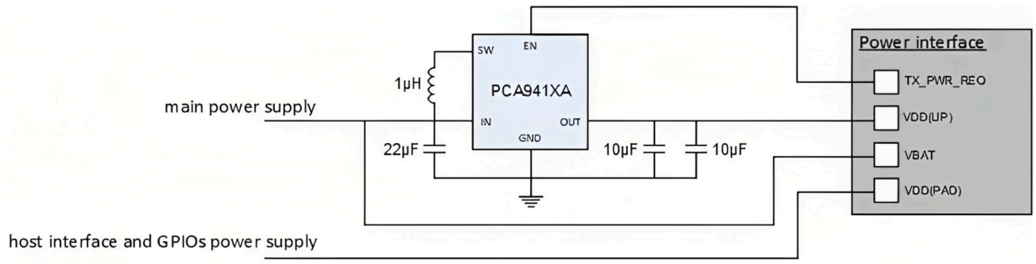

Figure 16. CFG2 - VDD (UP) and VBAT are supplied by an external voltage (VDD(UP) connected to DC-DC converter)

For the DC-DC external components, NXP recommends these parts:

- 10 µF on OUT pin: CL05A106MQ5NUNC
- 22 µF on IN pin: C1608X5R0J226M080AC
- 1 µH on IN pin; ASMPH-0603-1R0M-T

Depending on the chosen DC-DC converter, providing then different output voltage, the following TXLDO voltage can be set:

Table 13. TXLDO voltage in CFG2

DC-DC reference	DC-DC output voltage	TXLDO voltage available
PCA9410A	5 V	2.7V/3V/3.3V/3.6V/3.9V/4.2V/4.5V/4.75V
PCA9411A	5.2 V	2.7V/3V/3.3V/3.6V/3.9V/4.2V/4.5V/4.75V/5V
PCA9412A	5.4 V	2.7V/3V/3.3V/3.6V/3.9V/4.2V/4.5V/4.75V/5V/5.25V*

*For 5.25 V the TXLDO drop (1 Ohm * Itvdd) must be below then 150 mV.

9.3.3.1 Tx_PWR_REQ

To drive the external power supply used by the PN7160, the pin TX_PWR_REQ is available.

The Enable pin input impedance of the DC-DC (driven by the TX_PWR_REQ pin) must be higher than 200 kΩ.

The TX_PWR_REQ pin is rising when the polling phase is starting in reader mode and when an external field is detected in card mode.

/!\	Pay attention that TX_PWR_REQ pin is only available on VFBGA64 PN7160 variant. Alternatively the signal DCDC_EN can be used for the same purpose. This signal is available on both package variants. HVQFN and VFBGA.

9.3.3.2 DC-DC recommendations

The NXP DC-DC PCA941XA is recommended to be used with the PN7160.

If another DC-DC is used it must respect the specification of the table below, additionally the DC-DC must have a pass-through function to be able to always supply at least VDD(UP) > 2.5 V.

Table 14. DC-DC requirements

Parameter	Min	Typ	Max	Unit
Vin	2.5	3.6	5	V
Iout DC-DC	-	350	500	mA
Output voltage accuracy	2	-	4	%
Spurious less frequency range	12.5	-	14.5	MHz
Switching frequency	848	-	-	kHz
Vorms noise (incoherent noise) 100 kHz to 1.5 MHz band	-	-	660	uVrms
Vorms noise (incoherent noise) 12 MHz to 15 MHz band	-		660	uVrms
Output ripple voltage	-100	-	50	mV
Enable pin impedance	200	-	-	kΩ
Start up time	-	500	1000	us

9.4 Power supply configuration example

The picture below shows an example of the power supply configuration. The VDD_PAD is supplied by 3.3 V (host interface voltage reference) and VDD_UP + VBAT by external 5 V (supply voltage). So in this case it is configuration 2 (CFG2).

Table 15.

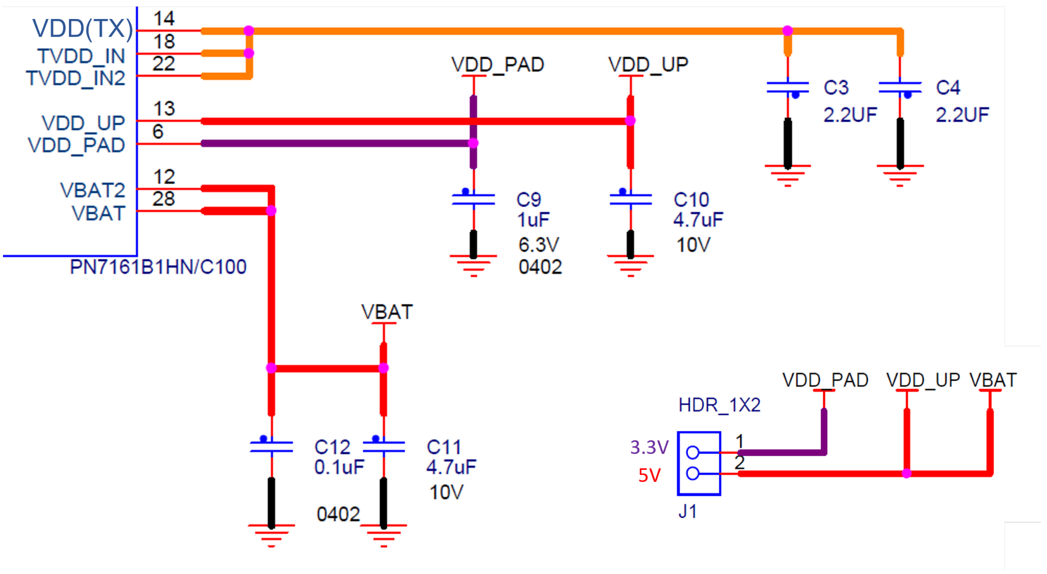

Figure 17. Example of typical application using an external power supply (VDD_PAD =3.3 V, VDD_UP and VBAT = 5 V)

Table 16. Possible power supply range

J1	PN7160 signal
1	VDD(PAD): 1.8 V or 3.3 V host interface voltage reference
2	VDD(UP) and VBAT: 2.8 V to 5.5 V supply voltage

9.5 PMU configuration

The setting of the power management unit is done using the "*PMU_CFG*" which is described in the user manual (Table 113. Core configuration parameters - Configuration of the Power Management Unit (PMU)).

Table 17. PMU Configuration in E²PROM

Name and Rights	Description	Extension Tag	Length	Default Value
PMU_CFG **RW in E²PROM**	Configuration of the Power Management Unit (PMU)	0xA0 0x0E	11	Byte 0: 0x11 Byte 1: 0x01 Byte 2: 0xC2 Byte 3: 0xB2 Byte 4: 0x00 Byte 5: 0xDA Byte 6: 0x1 E(600 µs) Byte 7: 0x14 Byte8: 0x00 Byte 9: 0xD0 Byte 10: 0x0C

Bytes of PMU_CFG parameter define the following:

- Byte1: RFU
- Byte 2 and Byte 3: Power and Clock Configuration per power mode configuration (Byte 2 for device ON, Byte 3 for Device OFF)
- Byte 4: RFU
- Byte 5: DC-DC 0
- Byte 6: DC-DC 1
- Byte 7: TXLDO
- Byte 8: RFU
- Byte 9: TXLDO check
- Byte 10: RFU

Usually bytes 2 and 7 must be changed. The rest depends on the user case (DC-DC usage, TXLDO Check). For the example described in the previous chapter, the configuration looks like this:

```
###############################################################################
# TVDD configurations settings
# Allow NFCC to configure External TVDD
# There are two possible configurations (0x01 or 0x02):
#    CFG1: Vbat is used to generate the VDD(TX) through TXLDO
#    CFG2: external 5V is used to generate the VDD(TX) through TXLDO
NXP_EXT_TVDD_CFG=0x02

# CFG1: TXLDO output voltage set to 3.3V
NXP_EXT_TVDD_CFG_1={20, 02, 0F, 01, A0, 0E, 0B, 11, 01, 01, B2, 00, DA, 1E, 1F, 00, D0, 0C}

# CFG2: TXLDO output voltage set to 4.7V
NXP_EXT_TVDD_CFG_2={20, 02, 0F, 01, A0, 0E, 0B, 11, 01, 02, B2, 00, DA, 1E, BF, 00, D0, 0C}

###############################################################################
```

Byte 2 and Byte 3: Power and Clock Configuration per power mode configuration (Byte 2 for device ON, Byte 3 for Device OFF)

Bit Mask								Description
b7	b6	b5	b4	b3	b2	b1	b0	
X								DC/DC usage in card mode 0b: DCDC bypassed 1b: DCDC is used
	X							DC/DC usage in reader mode 0b: DCDC bypassed 1b: DCDC is used
		X	X					Clock source: 00b: Default configuration given by CLOCK_SEL_CFG (PLL or XTAL) 11b: DLL RF Clock from external RF reader
						X	X	VUP input voltage: 01b: CFG1 10b: CFG2 Others: RFU
				0	0			RFU

Byte 7: TXLDO

Bit Mask								Description
b7	b6	b5	b4	b3	b2	b1	b0	TxLdo output voltage:
X	X	X	X					CFG1 and CFG2 DC/DC bypass 0000b: 3V 0001b: 3.3V 0010b: 3.6V 0011b: 4.5V 0100b: 4.75V 0101b: 5.25V 1000b: 2.7V 1001b: 3.9V 1010b: 4.2V 1011b: 4.7V 1111b: 5.0V Others: RFU
				X	X	X	X	CFG2 except DC/DC bypass 0000b: 3V 0001b: 3.3V 0010b: 3.6V 0011b: 4.5V 0100b: 4.75V 0101b: 5.25V 1000b: 2.7V 1001b: 3.9V 1010b: 4.2V 1011b: 4.7V 1111b: 5.0V Others: RFU

Figure 18. PMU configuration in libnfc-nxp.conf

/!\	In case one wants to use VDD(UP) different than 3.6 V or 5 V (E.g. 3.3 V). The TXLDO Check (Byte 9) has to be disabled. Otherwise the TX Driver (RF Field) does not start.

Byte 9: TXLDO check

Bit Mask								Description
b7	b6	b5	b4	b3	b2	b1	b0	VUP voltage check
X								When VUP expected being set to 5V 0 disabled, 1 enabled
	X							When VUP expecting being set to 3.6v 0 disabled, 1 enabled
		0	1	0	0	0	0	RFU

NOTE: FW automatically knows whether 5 V or 3.6 V is expected on VUP depending on other configuration bytes.

Figure 19. TXLDO Check

10 Antenna interface

Below figure show the way to connect a differential antenna to the PN7160.

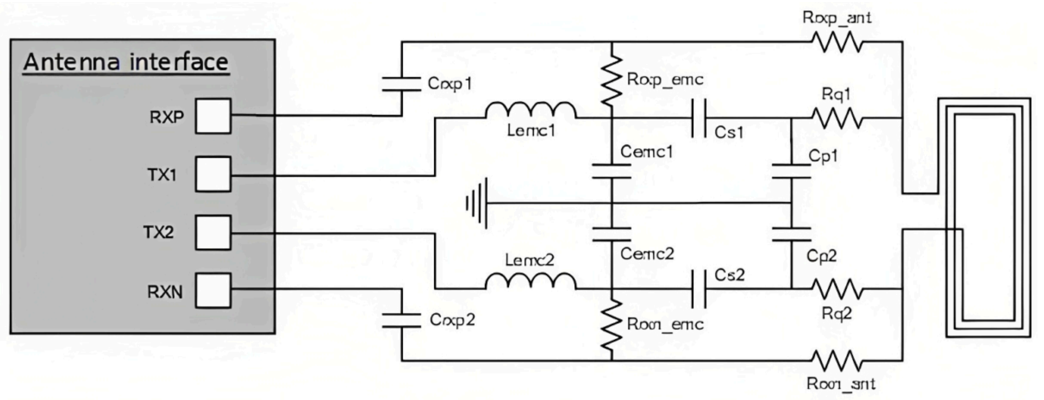

Figure 20. Antenna connection for differential antenna

All the details on the antenna matching and connections are listed in the PN7160 Antenna design guide.

11 Radiated Spurious Emissions

Electromagnetic interference (EMI) is a major concern in many RF Designs. The same applies to the design of the NFC reader. This chapter shows how to minimize the radiated emissions as well as stay below certain limits (E.g., FCC, ETSI, TELEC). And all this without a major drop in RF performance.

Typically the EMI issues (overshooting of given limits) are caused by:

- Incorrect matching network layout and wrong components placement
  - EMI filter (L0 and C0) is too far from the NFCC
  - Generally long RF traces
- Antenna detuning → Too high radiated power

See an example of the EMI friendly and unfriendly reader design.

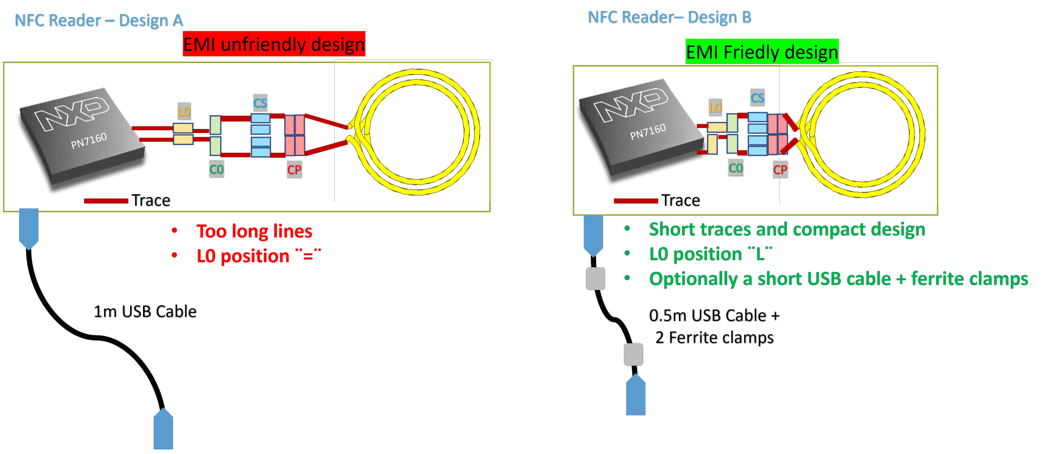

Figure 21. EMI Optimization

Sometimes it is not possible to meet all requirements (E.g., NFCC is in the center of the PCB and an antenna on the edge). Therefore, the following design can also be considered:

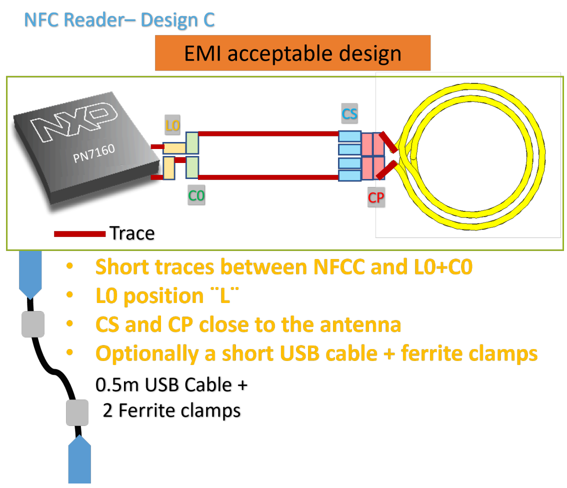

Figure 22. EMI acceptable design

/!\	Always place the L0 and C0 very close to PN7160 to have shorter TX lines!

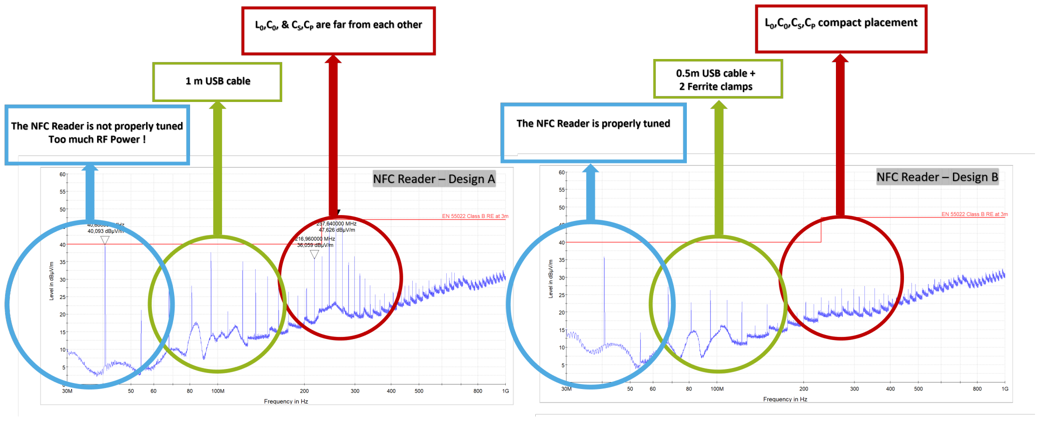

Figure 23. Radiated Emission Test Example

The antenna detuning can easily cause exceeding the radiated emissions. Make sure, that the antenna is correctly tuned. See the example below.

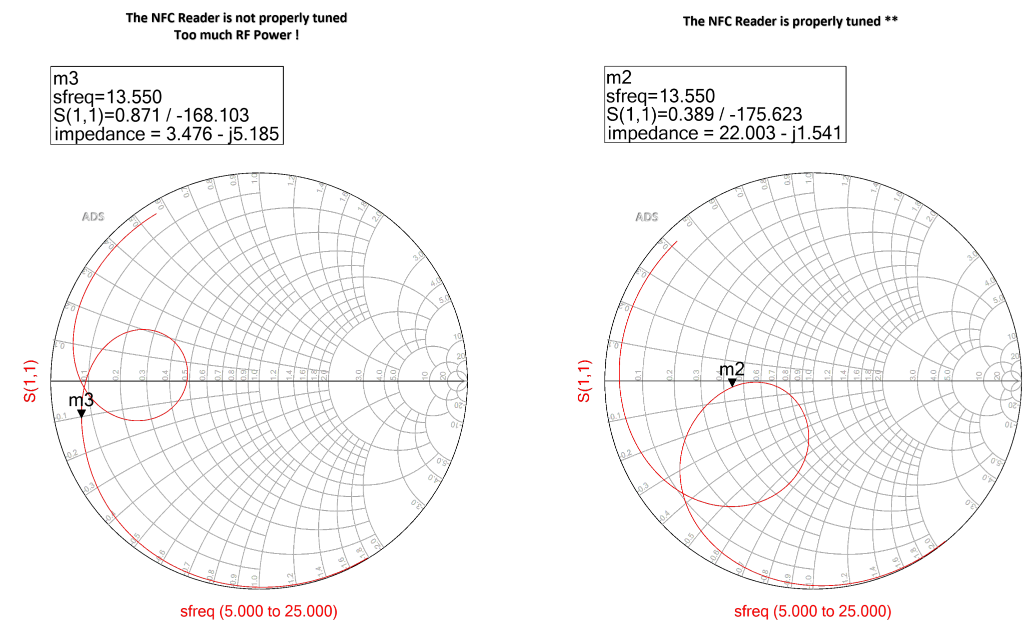

Figure 24. Antenna tuning examples

** Consider that the antenna tuning is given by the antenna parameters and supply voltage. For more details, see the PN7160 antenna design and matching guide.

11.1 Cycle and operating mode during emission tests

To measure the levels of radiated unwanted harmonics, for the ETSI, FCC and TELEC test of an NFC reader device, it is required to enable the RF carrier and send data with a typical modulation. Normally this includes a card being placed into the operating volume to enable a reasonable use case.

Typically, the following modes are required for the radiated emission tests:

- **Functional mode:** This configures the equipment under test in a mode where it generates RF modulated field regularly (about every 1 s) for a short period (about 100 ms).
- **RF ON mode:** To set the equipment under test in a constant unmodulated RF emission mode.
- **PRBS mode:** The test requires the device under test to send an endless PRBS sequence. (For tests in Japan)

All described modes can be activated using the **NFC Factory Test application** (See Figure 25). More details can be found in the *PN7160 Linux porting guide* document.

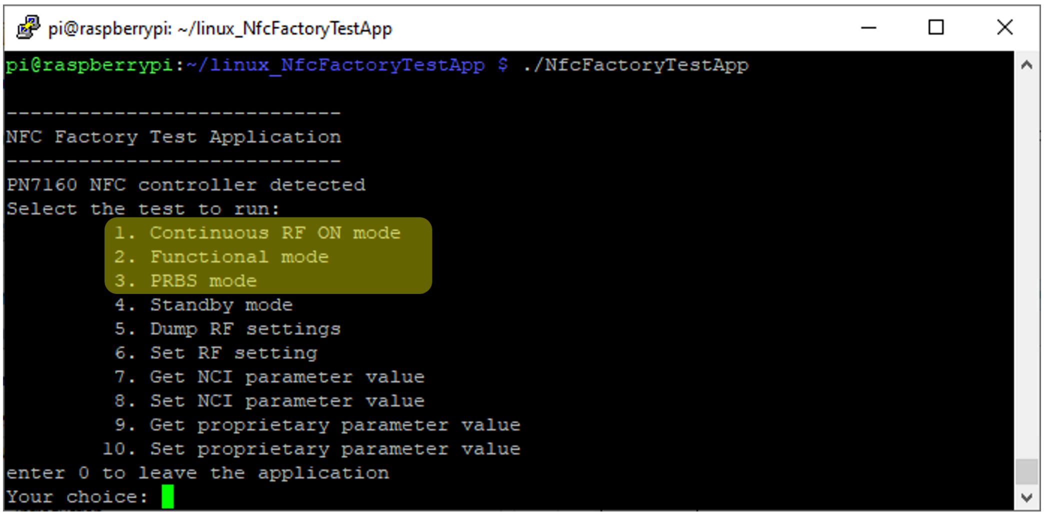

Figure 25. NFC Factory Test application

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