AN13678

i.MX6ULL EVK GenAVB/TSN Rework Application Note

Rev. 2.0 — 28 July 2022 **Application note**

Document information

Information	Content
Keywords	i.MX6ULL Applications Processor Evaluation Kit (MCIMX6ULL-EVK), GenAVB/TSN stack, Audio Video Bridging (AVB), Media Clock Recovery, tunable audio PLL
Abstract	This document describes the required hardware rework to be applied on the i.MX6ULL Applications Processor Evaluation Kit (MCIMX6ULL-EVK) in order to support the NXP GenAVB/TSN stack

1 Introduction

This document describes the required hardware rework to be applied on the i.MX6ULL Applications Processor Evaluation Kit (MCIMX6ULL-EVK) in order to support the NXP GenAVB/TSN stack.

To make MCIMX6ULL-EVK board fully support Audio Video Bridging (AVB), an important aspect is to add support for the Media Clock Recovery mechanism.

The NXP GenAVB/TSN stack supports two methods for media clock recovery depending on the underlying hardware:

- External method: Where an external low-jitter multiplier is needed on the board.
- Internal method: Can be implemented on SoCs with a tunable audio PLL on the fly. No external hardware is needed.

As the i.MX6ULL comes with a tunable audio PLL, the second method is implemented on the board.

2 Required connections

2.1 Media Clock Recovery: overall architecture

The media clock recovery mechanism is mainly implemented on the driver side. The internal of the mechanism is not the purpose of this document, but an overall description is given here.

The internal method relies on a few hardware blocks:

- The ENET 1588 timer in the Ethernet MAC (in Output Compare Mode): A stream of timestamps at a relatively low frequency drives the 1588_EVENT signal.
- GPT timer: The GPT counter clock is connected to the Audio Master clock and the *GPT_CAPTURE* input signal is connected to the *1588_EVENT* from ENET. This arrangement makes drift calculation and adjustments, between the audio master clock and the media master clock (derived from the timestamps), possible on driver side.

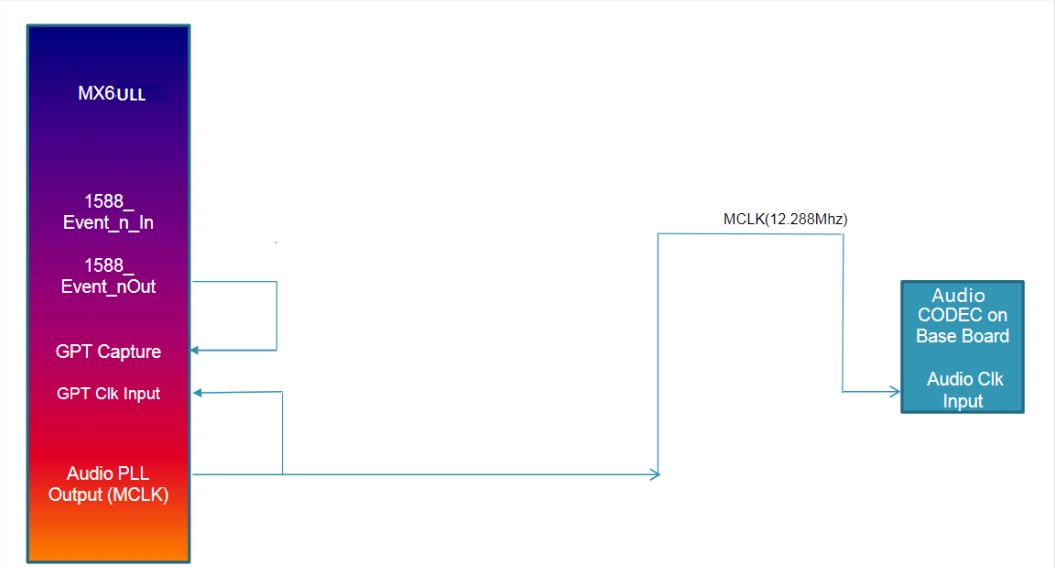

Figure 1. Media clock recovery: internal method

2.2 Detailed connections and possible PAD assignments

For the MCIMX6ULL-EVK board, the mapping between the Linux network device name and the ENET instance number in the SoC is the following:

- ENET2: eth0
- ENET1: eth1

GenAVB/TSN stack works by default on eth0, therefore ENET2 is used.

ENET2_1588_EVENTX_OUT signal from the Ethernet MAC should be connected to the ***GPT2_CAPTUREY*** input capture channel in the General Purpose Timer (Instance 2).

Note:

1. *In signal name **ENET2_1588_EVENTX_OUT**, X represents the number of the IEEE 1588 Channel from 0 to 3, which is configurable in the device tree)*
2. *In signal name **GPT2_CAPTUREY**, Y is one of the possible capture channels 1 or 2, which is configurable in the device tree.*

In addition, **AUDIO MASTER CLOCK** serving the Audio codec, is connected to **GPT2_CLK**. On MCIMX6ULL-EVK board, the audio master clock is on **SAI2_MCLK** pad (However, this may vary for other audio interfaces).

On MCIMX6ULL-EVK, the codec is fed from the **SAI2_MCLK**, which is already set to 12.288 MHz.

The GPT2_CLK requires that its frequency **does not exceed the ¼ of the peripheral clock** (66 MHz). This clock is by default set to 12.288 MHz. (Refer to the paragraph 30.2.1 in the *i.MX6ULL Reference Manual* [1].

Every signal can be routed through one or multiple routing pads. The table below summarizes the available i.MX6ULL signals and routing pads.

Table 1. i.MX6ULL signal availability and routing pads

Signal		Pad (mode)
ENET2	1588_EVENT0_OUT	GPIO1_IO05(ALT6)
	1588_EVENT1_OUT	UART1_RTS_B(ALT4)
	1588_EVENT2_OUT	LCD_DATA05(ALT3)
	1588_EVENT3_OUT	LCD_DATA07(ALT3)
SAI2	MCLK	JTAG_TMS (ALT2)
		SD1_CLK (ALT2)
GPT2	CAPTURE1	JTAG_TMS(ALT1)
		SD1_DATA2(ALT1)
	CAPTURE2	JTAG_TDO(ALT1)
		SD1_DATA3(ALT1)
	CLK	JTAG_MOD(ALT1)
		SD1_DATA1(ALT1)

3 Implementation example

This section describes one of the possible combinations specified below. This implementation was tested for the Media Clock Recovery with the NXP GenAVB/TSN stack.

The needed steps are the following:

1. Software changes: Configure the GPIO1_IO05 Pad (TP2120) to the ENET2_1588_EVENT0_OUT signal.
2. Software changes: Configure the SD1_DATA2 Pad (R1728) to the GPT2_CAPTURE1 signal.
3. Hardware changes: Connect R1728 to TP2120 (Refer to Connecting GPT CAPTURE to ENET EVENT OUT).
4. Software changes: Configure the JTAG_MOD Pad (R1023) to the GPT2_CLK signal.
5. Software changes: Configure the JTAG_TMS Pad (JTAG Pin 7) to the SAI2_MCLK signal.
6. Hardware changes: Connect R1023 to JTAG Pin 7 (Refer to figures Figure 3 and Figure 4).

Note: *Software changes (IOMUX pin control) are implemented in the Board AVB-specific Device Tree.*

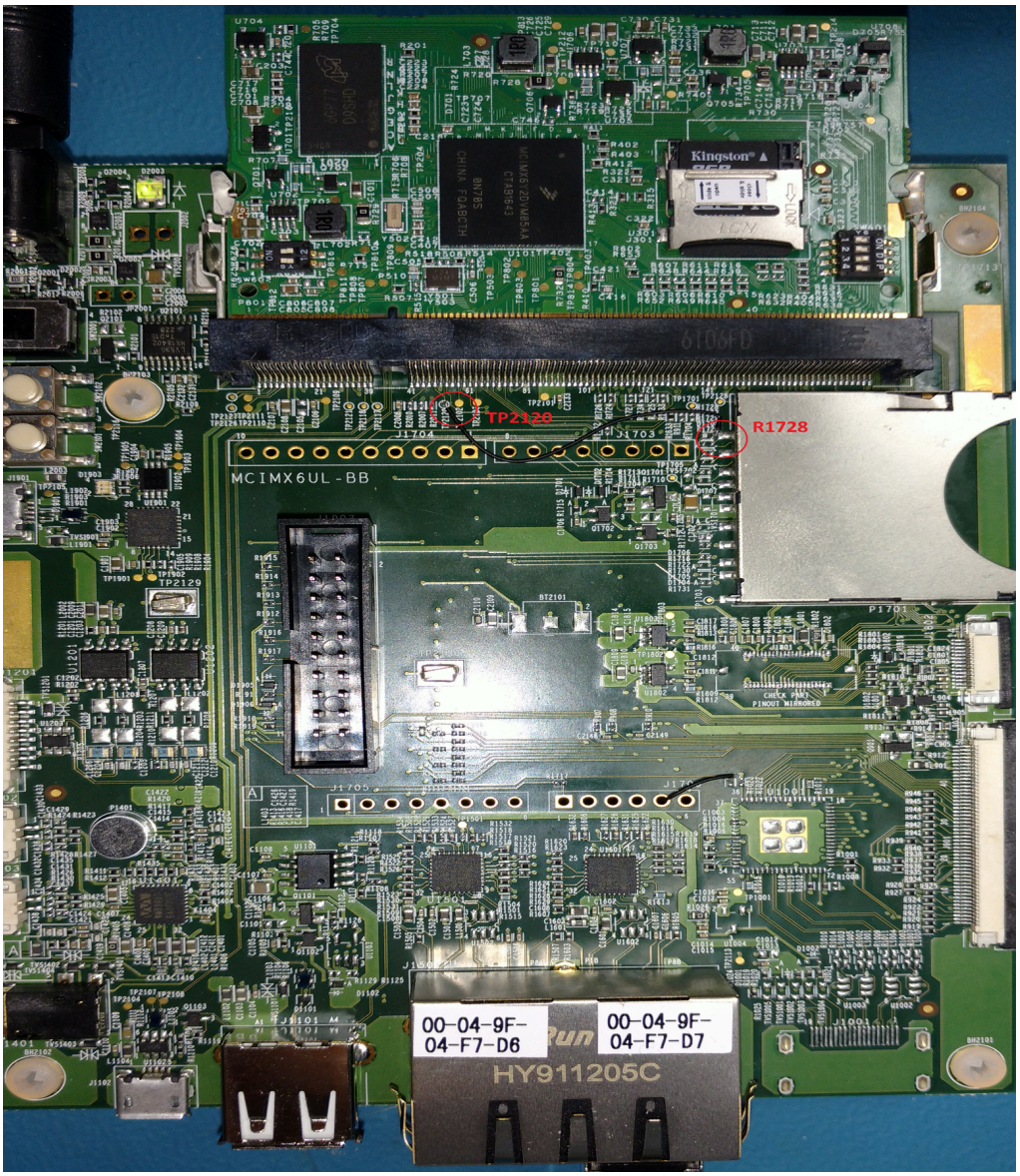

Figure 2. Connecting GPT CAPTURE to ENET EVENT OUT

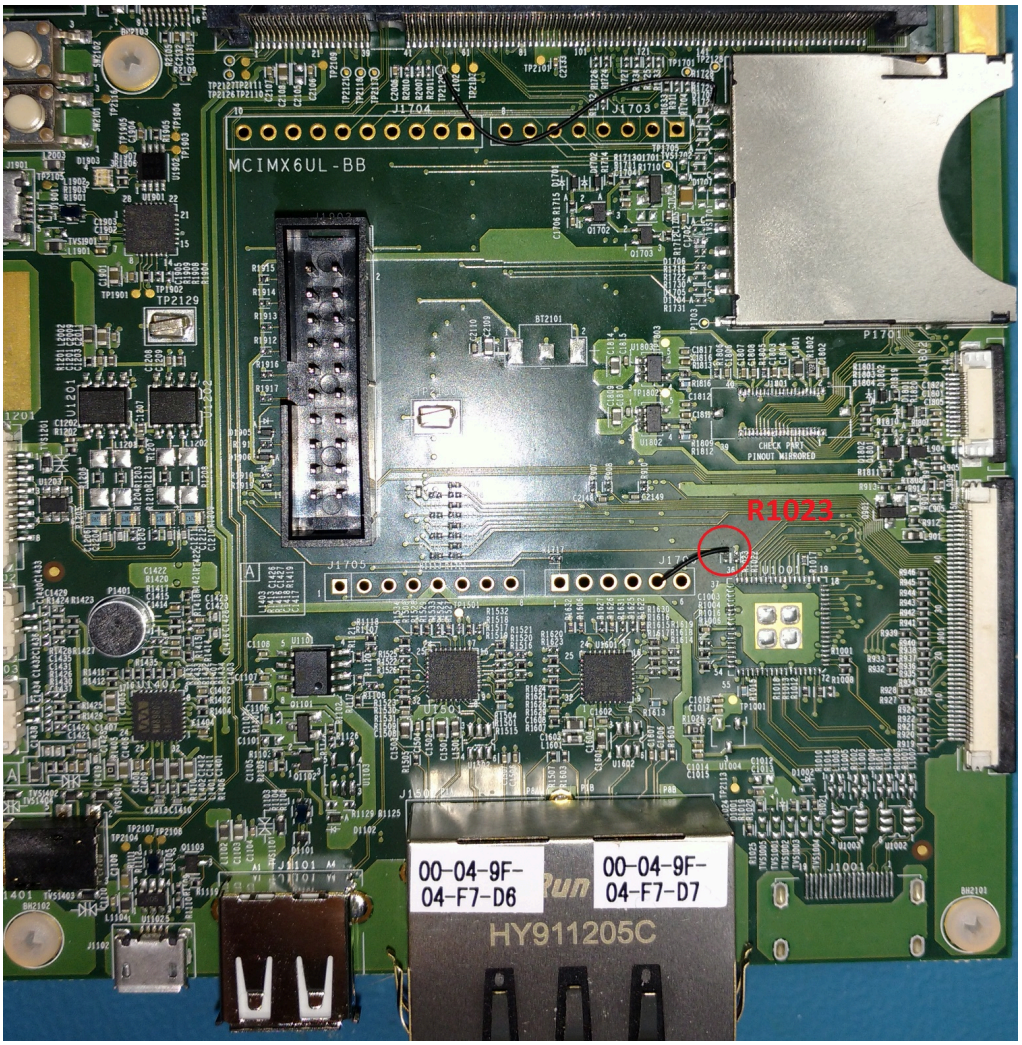

Figure 3. Connecting AUDIO MCLK to GPT CLK (Top Side)

Figure 4. Connecting R1023 to JTAG Pin 7

4 References

1. https://www.nxp.com/docs/en/reference-manual/IMX6ULLRM.pdf
2. GenAVB/TSN Stack Evaluation User Guide (GenAVBTSNUG) available on Real Time Edge Software Documentation

5 Revision history

Table 2. Document revision history

Revision Number	Date	Description
2	28 July 2022	Updated for Real-Time Edge software version 2.3 release
1	May 2018	Resistor Number of JTAG_MOD Pad fixed
0	January 2018	Initial Release

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