AN13761

PSI5 programming mode procedures for FXLS9xxxx sensors

Rev. 1.1 — 29 November 2023 Application note

Document information

Information	Content
Keywords	FXLS93xxx, FXLS93xx0, OTP, one time programmable memory, sensor, single channel, dual-channel, inertial sensor, PSI5.
Abstract	AN13761 describes procedures to perform one time programmable (OTP) memory of the FXLS93xxx single and dual- channel inertial sensor using the PSI5 programming mode.

1 Introduction

This document describes the recommended procedures to program the One Time Programmable (OTP) memory of the FXLS93xxx single and dual-channel inertial sensors using PSI5 programming mode. It describes the recommended procedures for initializing and configuring FXLS93xxx devices on a PSI5 bus transmission using PSI5 programming mode.

2 Applicable parts

This document applies to the NXP sensors listed in Table 1.

Table 1. Applicable parts

Part	Description
FXLS93xxx	Dual-channel PSI5 Inertial Sensor
FXLS93xx0	Single-channel PSI5 Inertial Sensor

3 Application schematic and device connections

The procedures outlined in this document assume that one sensor is connected to a PSI5 controller. The PSI5 controller provides both power and communication via the BUS_I and BUSRTN pins through the recommended PSI5 network shown in Figure 1 and Table 2.

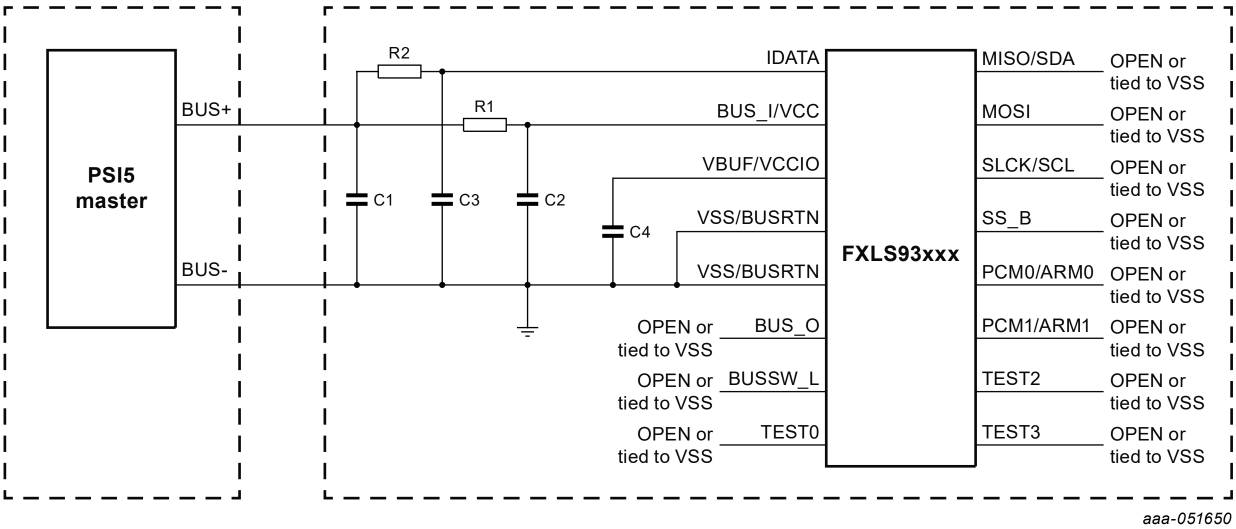

Figure 1. Application schematic

Table 2. PSI5 OTP Programming of a PSI5 application device

Recommended Components			
Ref. Designator	Type	Description	Purpose
C1	Ceramic	2.2 nF, 10 %, 50 V minimum, X7R	V_{CC} power supply decoupling and signal damping
C2	Ceramic	15 nF, 10 %, 50 V minimum, X7R	V_{CC} power supply decoupling

Table 2. PSI5 OTP Programming of a PSI5 application device*...continued*

Recommended Components			
Ref. Designator	Type	Description	Purpose
C3	Ceramic	470 pF, 10 %, 50 V minimum, X7R	I_{DATA} power supply decoupling
C4	Ceramic	0.47 µF, 10 %, 10 V minimum, X7R	Buffer regulator output capacitor for micro-cut immunity
R1	General Purpose	82 Ω, 5 %, 200 PPM	V_{CC} filtering and signal damping
R1	General Purpose	27 Ω, 5 %, 200 PPM	I_{DATA} filtering and signal damping

4 Device power restrictions

Power must be applied to the FXLS93xxx with the ramp rates specified in the data sheet. The supply voltage for the device is applied through the PSI5 network shown in Figure 1. As specified in the data sheet, the voltage at the IDATA pin during OTP memory programming must be between 9 V and 11 V. The source must be able to supply the full current draw of the bus plus an additional 5 mA without dipping below 9 V. The applied voltage must consider the voltage drop across the PSI5 network resistor, R1 as shown in the equations below:

$$VSUP_{MIN} \geq BUS\_I_{VPPMIN} + I_{VPP} \times R2_{MAX}$$
$$VSUP_{MIN} \geq 9\ V + (9\ mA + 5\ mA) \times 72\ \Omega = 10.3\ V$$
$$VSUP_{MAX} \leq BUS\_I_{VPPMAX} + I_{VPP} \times R1_{MIN}$$
$$VSUP_{MAX} \leq 11\ V + (4\ mA) \times 92\ \Omega = 11.3\ V$$

The example in this document uses a supply voltage of 11.0 V with a current limit of 125 mA. The supply ramp is shown in Figure 2.

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Figure 2. Programming Voltage Supply Ramp

5 Bidirectional communication via PSI5 programming mode

The following sections describe PSI5 Programming Mode and its use to configure, program, and test an FXLS93xxx device. All communication in PSI5 Programming Mode uses the following settings and timing.

Table 3. PSI5 parameters and values

Parameter	Value
Sync pulse rate	4 kHz (250 µs)
Response time slot	Time Slot 1: 46 µs
Response data size	10-bit
Response error checking	Even parity
Response bit rate	125 kbit/s (8 µs)

All PSI5 Programming Mode Commands use either the Short or Extra Long format and must include sync bits (logic 1) every fourth bit as shown in Figure 3 and Figure 4.

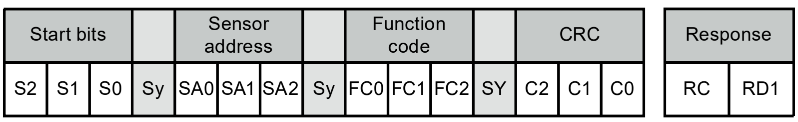

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Figure 3. PSI5 Programming Mode Short Command and Response Format

Start bits				Sensor address				Function code				Register address										Data											CRC				Response		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	SY	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	RA6	RA7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0	RC	RD1	RD0

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Figure 4. PSI5 Programming Mode Extra Long Command and Response Format

5.1 Power on PSI5 programming mode communication delay

A PSI5 programmed device will decode Programming Mode Entry commands from 6 ms to 133 ms after power is applied to the sensor. The PSI5 controller must provide at least 6 ms prior to sending the PSI5 Programming Mode Entry Start Condition as shown in Figure 5.

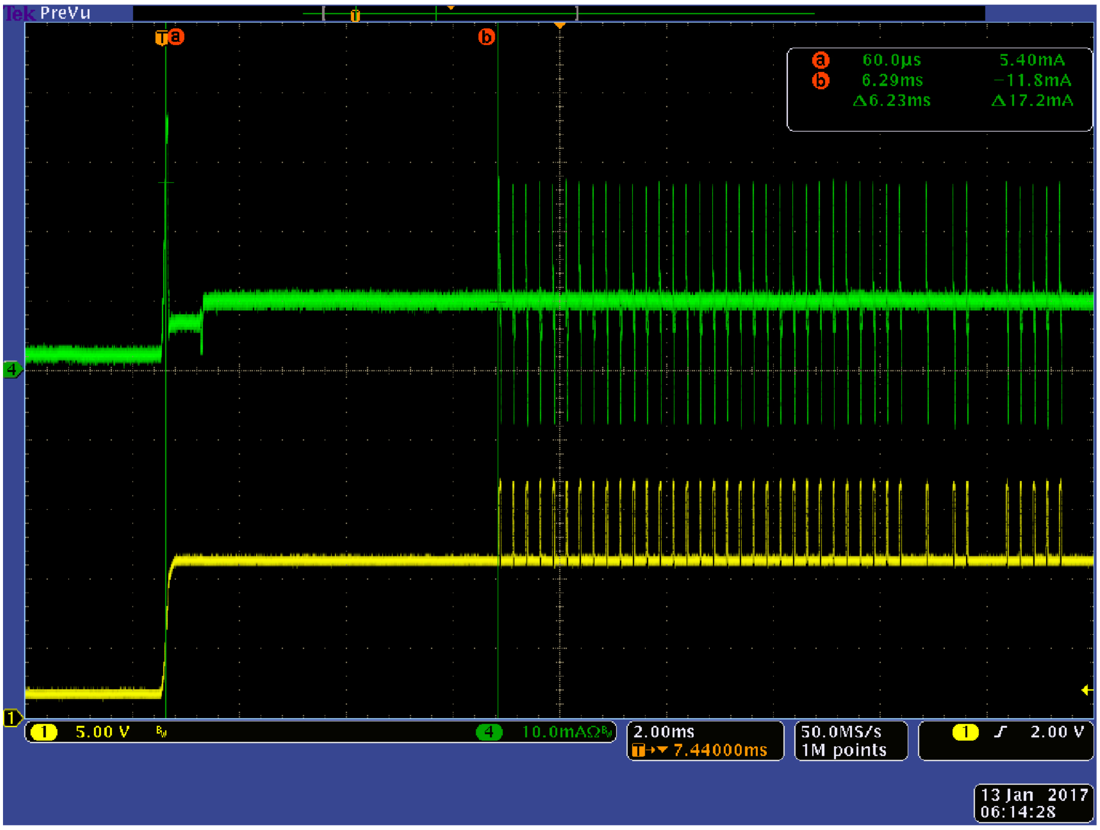

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Figure 5. Power On PSI5 Programming Mode Communication Delay

5.2 PSI5 programming mode entry start condition

Precede the Programming Mode Entry command with a start condition consisting of 31 consecutive logic 1s (sync pulses) as shown in Figure 6.

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Figure 6. PSI5 Programming Mode Entry Start Condition, 31 Sync Pulses

5.3 PSI5 programming mode entry command

The PSI5 Programming Mode Entry (PME) Command is a short command with the format shown in Figure 3 and settings shown in Table 4 and Table 5. Figure 7 and Figure 8 show the PSI5 PME command and response.

Table 4. PSI5 programming mode entry command parameters and values

Parameter	Value
Command Type	Short
Start Bits (Start)	010
Sensor Address (SAdr)	001
Function Code (FC)	111
CRC (CRC)	001

Table 5. PSI5 programming mode entry settings

Start Bits				Sensor Address				Function Code				CRC				Response	
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	C2	C1	C0		RC	RD1
0	1	0	1	0	1	0	1	1	1	1	1	0	0	1		1E1	0CA

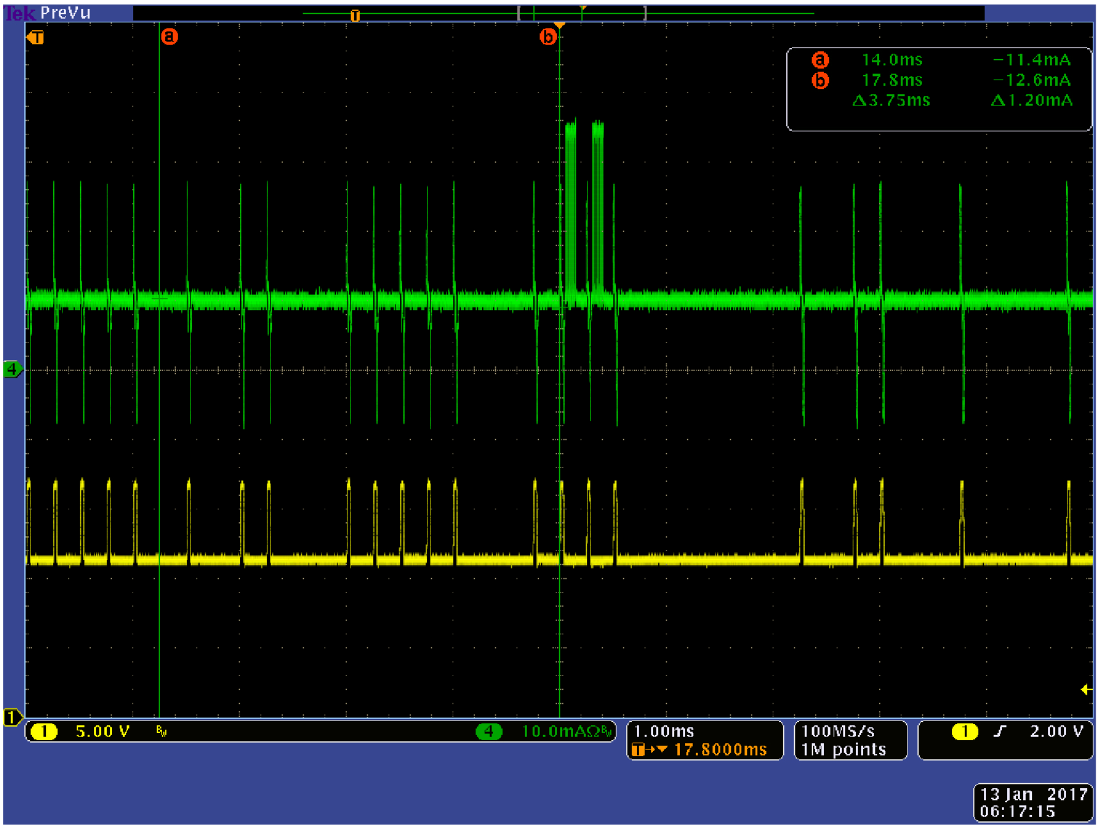

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Figure 7. PSI5 Programming Mode Entry Command

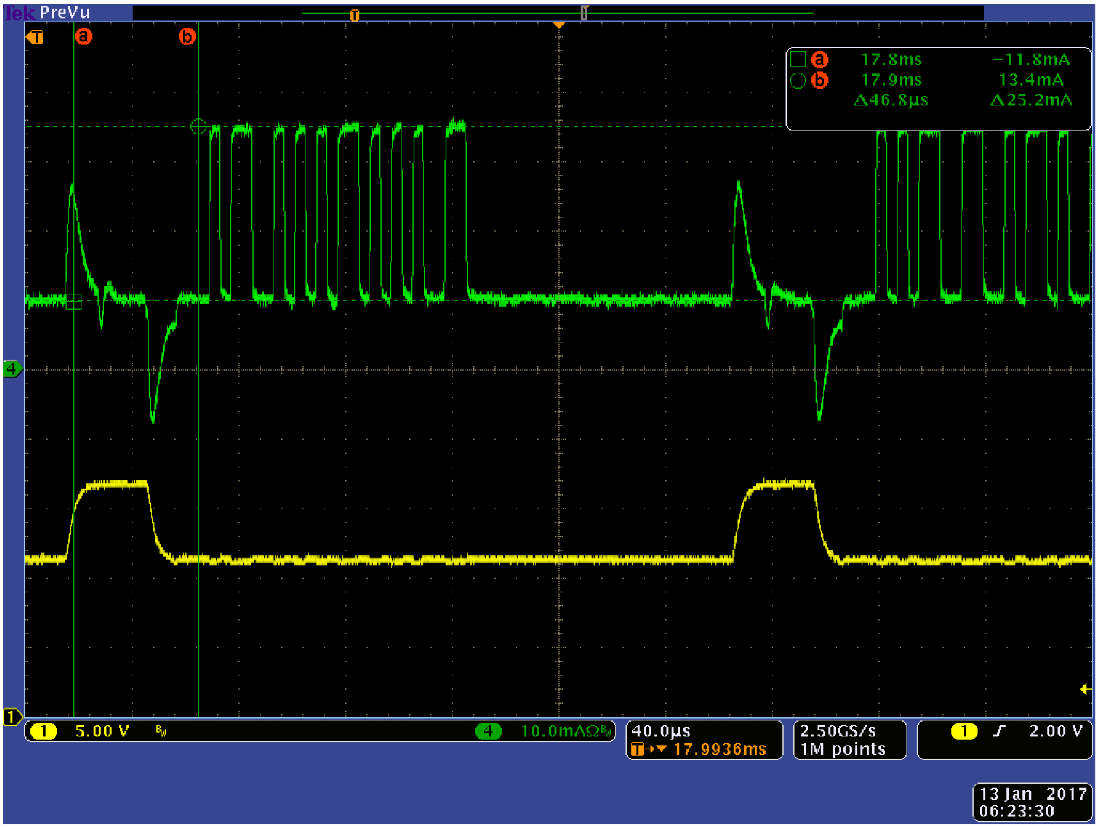

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Figure 8. PSI5 Programming Mode Entry Response

5.4 PSI5 programming mode normal command start condition

Once the PME is received, all PSI5 Programming Commands must be preceded using one of the following start conditions:

- A minimum of 5 consecutive logic ‘0’s (with no sync bits)
- A minimum of 31 consecutive logic ‘1’s (this includes logic ‘1’s transmitted for the previous response)

Figure 9 shows an example start condition with 6 nSync bits.

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Figure 9. PSI5 Programming Mode Command Start Condition, 6 nSync Bits

5.5 PSI5 programming mode normal commands and responses

All PSI5 Programming Mode commands after the PME use the Extra Long Command Format shown in Figure 4. Only two commands are supported: Register Read and Register Write. Table 6 and Table 7 show the command settings for the 2 commands. Figure 10 and Figure 11 show the read and write command and response formats for PSI5 programming mode.

Table 6. PSI5 programming register read parameters and values

Parameter	Value
Command Type	XLONG Read
Start Bits (Start)	010
Sensor Address (SAdr)	001
Function Code (FC)	000
CRC (CRC)	Variable

Start bits				Sensor address				Function code				Register address										Register data											CRC					Response		
S2	S1	S0	Sy	SA 0	SA 1	SA 2	Sy	FC 0	FC 1	FC 2	Sy	RA 0	RA 1	RA 2	Sy	RA 3	RA 4	RA 5	Sy	RA 6	RA 7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0		RC	RD 1	RD 2
0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1		1E1	C0	D4

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Figure 10. PSI5 programming mode read register command and response format

Table 7. PSI5 programming register write parameters and values

Parameter	Value
Command Type	XLONG Write
Start Bits (Start)	010
Sensor Address (SAdr)	001
Function Code (FC)	001
CRC (CRC)	Variable

Start bits				Sensor address				Function code				Register address										Register data											CRC					Response		
S2	S1	S0	Sy	SA 0	SA 1	SA 2	Sy	FC 0	FC 1	FC 2	Sy	RA 0	RA 1	RA 2	Sy	RA 3	RA 4	RA 5	Sy	RA 6	RA 7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0		RC	RD 1	RD 2
0	1	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0		1E1	76	12

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Figure 11. PSI5 programming mode write register command and response format

Figure 12 is an example PSI5 programming mode command and response.

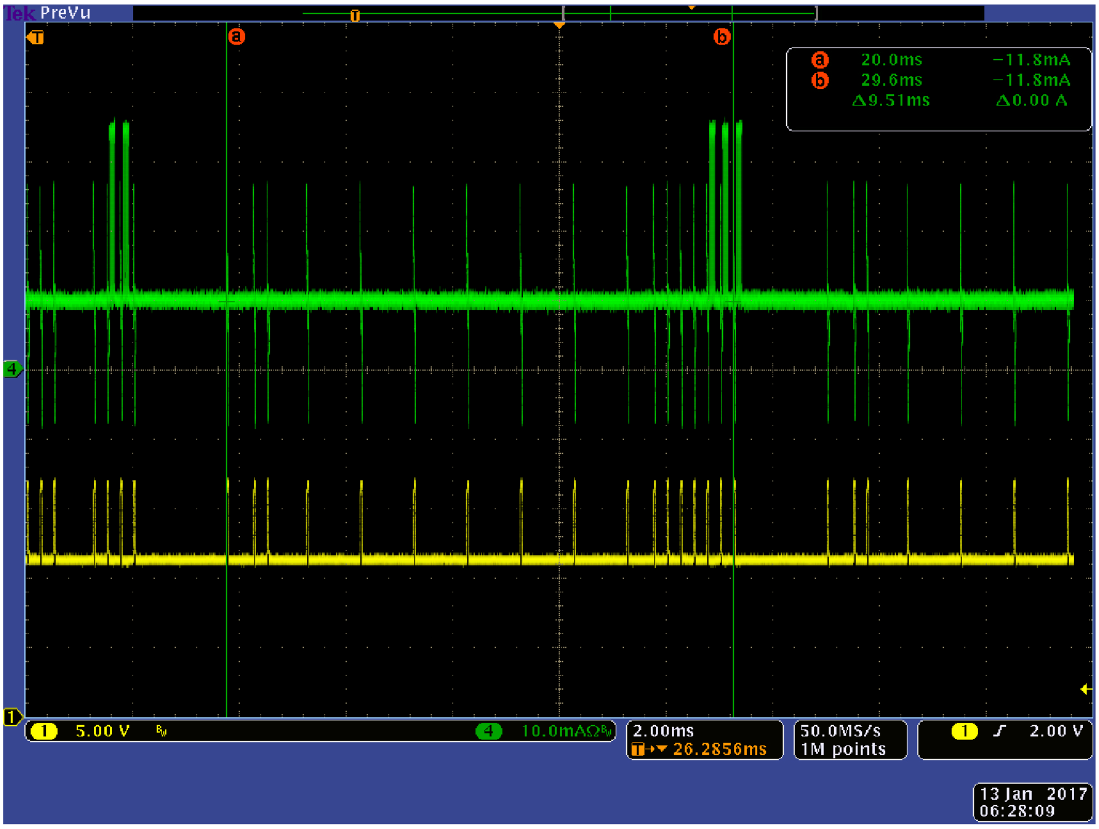

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Figure 12. PSI5 programming mode command and response example

6 User OTP array programming via PSI5 programming mode

Figure 13 shows an overview of the User OTP array programming procedure. Each procedure block is covered by a separate subsection.

Note that in the examples, some register writes to the value 0x00 are included for completeness. If a desired register value is 0x00, the write command need not be executed.

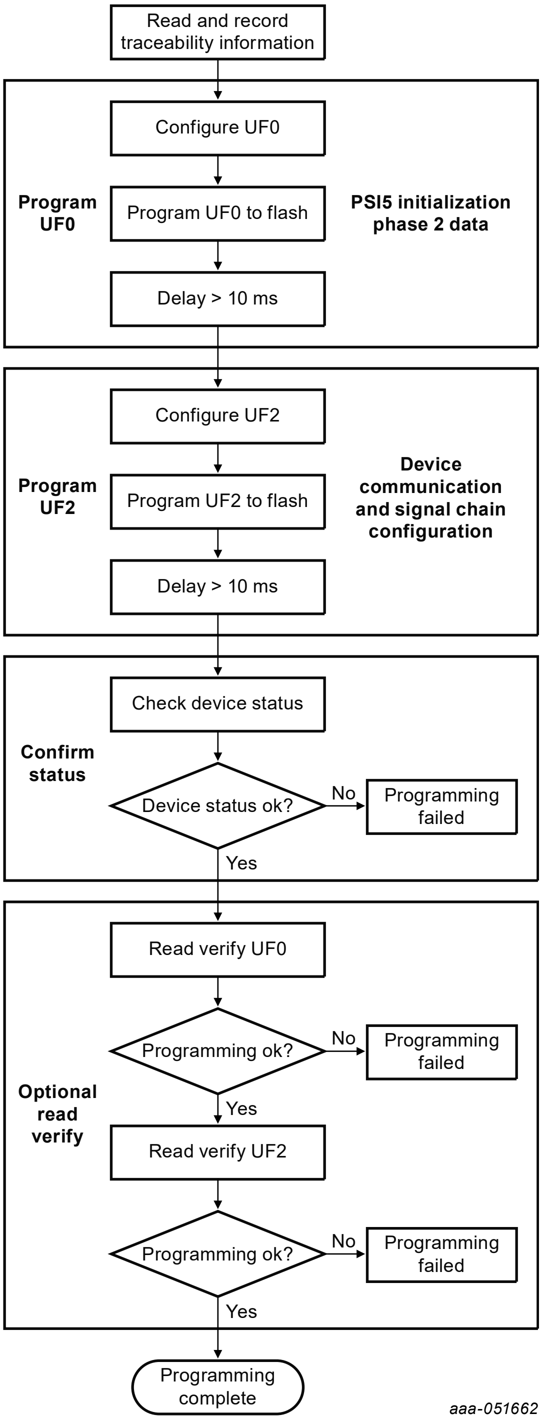

Figure 13. PSI5 programming mode OTP programming procedure for FXLS93xxx

6.1 Optional read and record traceability information

Prior to programming the OTP of the device, the user can optionally read and record the device level traceability information, and confirm that the device part number is correct.

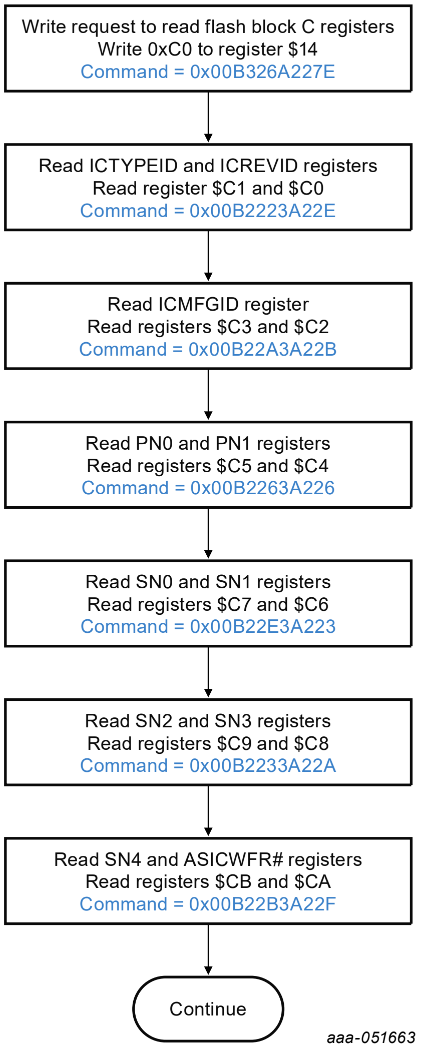

Figure 14. PSI5 Programming Mode - Read and Record Traceability Information

6.2 Program UF0: PSI5 initialization phase 2 data

The UF0 block of memory includes fifteen 8-bit user programmable registers from address $E0 to $EE that map to the PSI5 Initialization Phase two transmission data. The data mapping to initialization phase two data fields is shown in Table 8.

Table 8. UF0 register to PSI5 initialization phase 2 data field mapping

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$E0	USERDATA_0	Channel 1 F1:D1				Channel 0 F1:D1			
$E1	USERDATA_1	Channel 0 F3:D5				Channel 0 F3:D4			
$E2	USERDATA_2	Channel 0 F4:D7				Channel 0 F4:D6			
$E3	USERDATA_3	Channel 0 F5:D9				Channel 0 F5:D8			
$E4	USERDATA_4	Channel 0 F6:D11				Channel 0 F6:D10			
$E5	USERDATA_5	Channel 0 F7:D13				Channel 0 F7:D12			

Table 8. UF0 register to PSI5 initialization phase 2 data field mapping*...continued*

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$E6	USERDATA_6	Channel 0 F9:D32				Channel 0 F7:D14			
$E7	USERDATA_7	Channel 0 F8:D16 = Channel 1 F8:D16				Channel 0 F8:D15 = Channel 1 F8:D15			
$E8	USERDATA_8	Channel 0 F8:D18 = Channel 1 F8:D18				Channel 0 F8:D17 = Channel 1 F8:D17			
$E9	USERDATA_9	Channel 1 F3:D5				Channel 1 F3:D4			
$EA	USERDATA_A	Channel 1 F4:D7				Channel 1 F4:D6			
$EB	USERDATA_B	Channel 1 F5:D9				Channel 1 F5:D8			
$EC	USERDATA_C	Channel 1 F6:D11				Channel 1 F6:D10			
$ED	USERDATA_D	Channel 1 F7:D13				Channel 1 F7:D12			
$EE	USERDATA_E	Channel 1 F9:D32				Channel 1 F9:D14			
Factory Default		0	0	0	0	0	0	0	0

Figure 15 sets the PSI5 Initialization phase two data as shown in Table 9.

Table 9. Example PSI5 initialization phase 2 data

Channel	PSI5 Field ID#	PSI5 Nibble ID #	Description	Value	Register
0	F1	D1	Protocol Revision 1.3	0x4	E0[3:0]
	F2	D2	Number of Data Blocks = 32	0x2	N/A
		D3	Number of Data Blocks = 32	0x0	N/A
	F3	D4	0xFF Supplier Code	0xF	E1[3:0]
		D5	0xFF Supplier Code	0xF	E1[7:4]
	F4	D6	High g Sensor	0x0	E2[3:0]
		D7	High g Sensor	0x1	E2[7:4]
	F5	D8	120 g Sensor	0x0	E3[3:0]
		D9	120 g Sensor	0x8	E3[7:4]
	F6	D10	Sensor Specific Information = 0x0	0x0	E4[3:0]
		D11	Sensor Specific Information = 0x0	0x0	E4[7:4]
	F7	D12	Sensor Specific Information = 0x0	0x0	E5[3:0]
		D13	Sensor Specific Information = 0x0	0x0	E5[7:4]
		D14	Sensor Specific Information = 0x0	0x0	E6[3:0]
	F8	D15	Date Code = April 22, 2016	0x2	E7[3:0]
		D16	Date Code = April 22, 2016	0x0	E7[7:4]
		D17	Date Code = April 22, 2016	0x9	E8[3:0]
		D18	Date Code = April 22, 2016	0x6	E8[7:4]
1	F1	D1	Protocol Revision 1.3	0x4	E0[7:4]
	F2	D2	Number of Data Blocks = 32	0x2	N/A
		D3	Number of Data Blocks = 32	0x0	N/A
	F3	D4	0xFF Supplier Code	0xF	E9[3:0]

Table 9. Example PSI5 initialization phase 2 data*...continued*

Channel	PSI5 Field ID#	PSI5 Nibble ID #	Description	Value	Register
		D5	0xFF Supplier Code	0xF	E9[7:4]
	F4	D6	High g Sensor	0x0	EA[3:0]
		D7	High g Sensor	0x1	EA[7:4]
	F5	D8	120 g Sensor	0x0	EB[3:0]
		D9	120 g Sensor	0x8	EB[7:4]
	F6	D10	Sensor Specific Information = 0x0	0x0	EC[3:0]
		D11	Sensor Specific Information = 0x0	0x0	EC[7:4]
	F7	D12	Sensor Specific Information = 0x0	0x0	ED[3:0]
		D13	Sensor Specific Information = 0x0	0x0	ED[7:4]
		D14	Sensor Specific Information = 0x0	0x0	EE[3:0]
	F8	D15	Date Code = April 22, 2016	0x2	E7[3:0]
		D16	Date Code = April 22, 2016	0x0	E7[7:4]
		D17	Date Code = April 22, 2016	0x9	E8[3:0]
		D18	Date Code = April 22, 2016	0x6	E8[7:4]

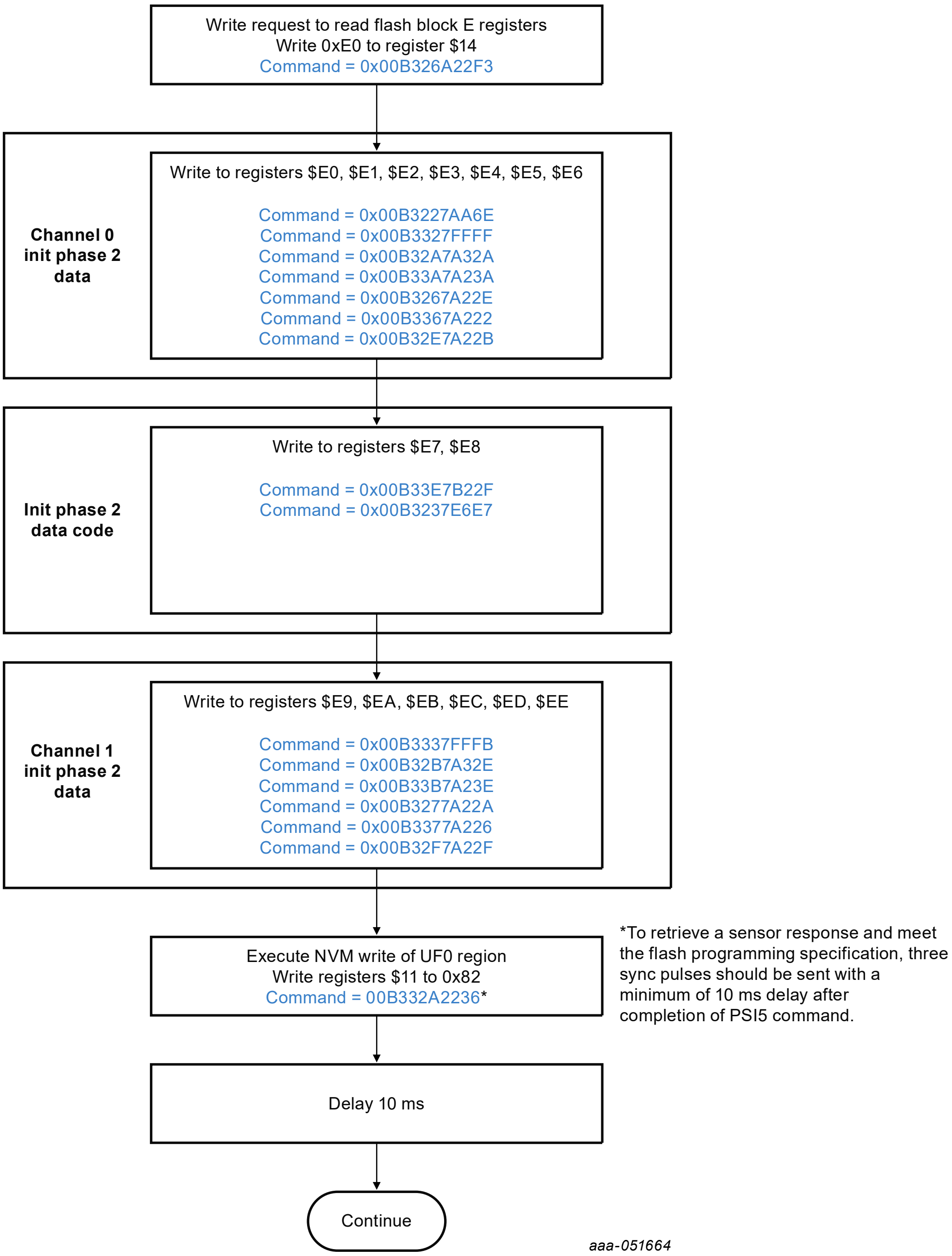

Figure 15. PSI5 programming mode – program initialization phase 2 data

6.3 Program UF2: device configuration

The UF2 block of memory includes the user programmable communication and sensor signal chain configuration information.

6.3.1 Enable and Configure the Data Sources

Each channel of the FXLS93xxx devices is capable of two independently configurable data sources. Data source types include:

- Acceleration data with offset cancellation enabled
- Acceleration data with offset cancellation disabled (bypassed)
- Temperature sensor data

Figure 16 shows a pictorial mapping of the sources to their source identifiers and associated data.

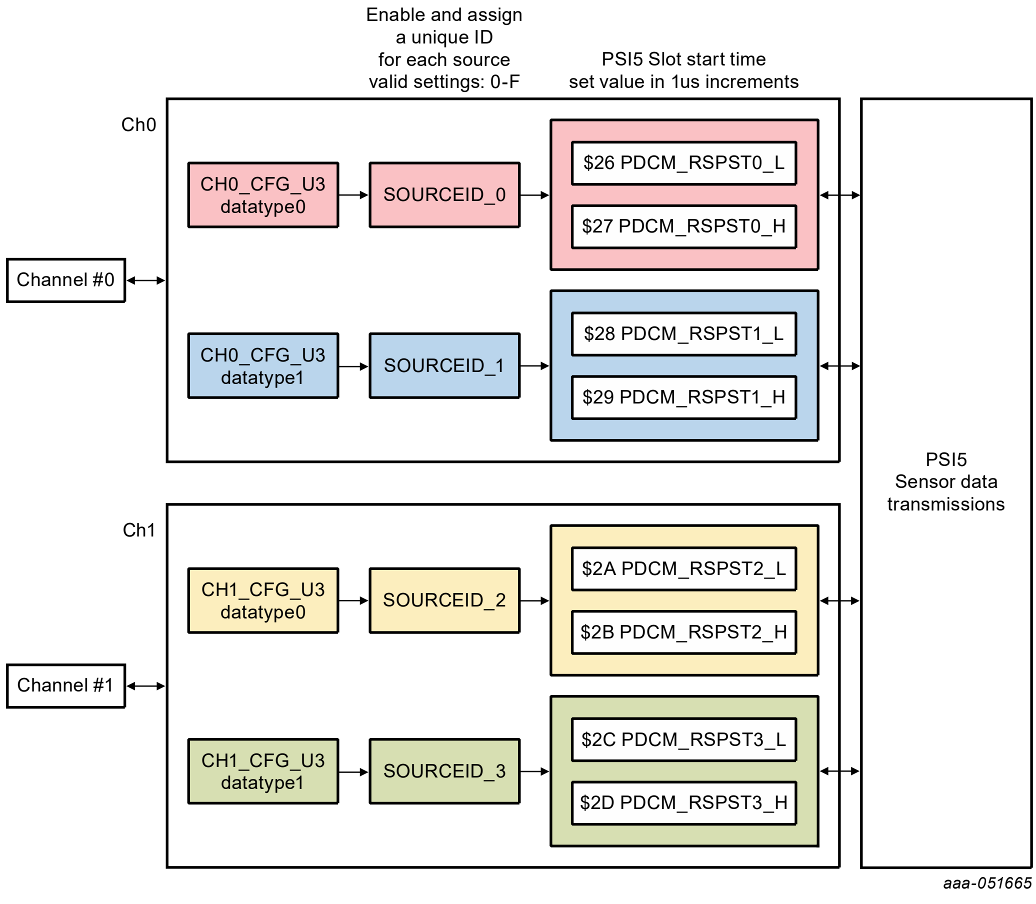

Figure 16. Data source mapping diagram

In addition to data source transmission configuration, other PSI5 transmission configurations are possible by writes to the CHIPTIME register and the PSI5_CFG register. Some possible configurations include:

PSI5 bit rate:	125 kbit/s or 189 kbit/s
PSI5 error checking:	parity or 3-bit CRC
PSI5 Sync Pulse Blanking:	Default set for 500 µs Sync pulse rate
PSI5 Daisy Chain mode or Asynchronous mode	
PSI5 Low-power mode	

Figure 17 shows one example configuration enabling acceleration data with offset cancellation enabled for each channel.

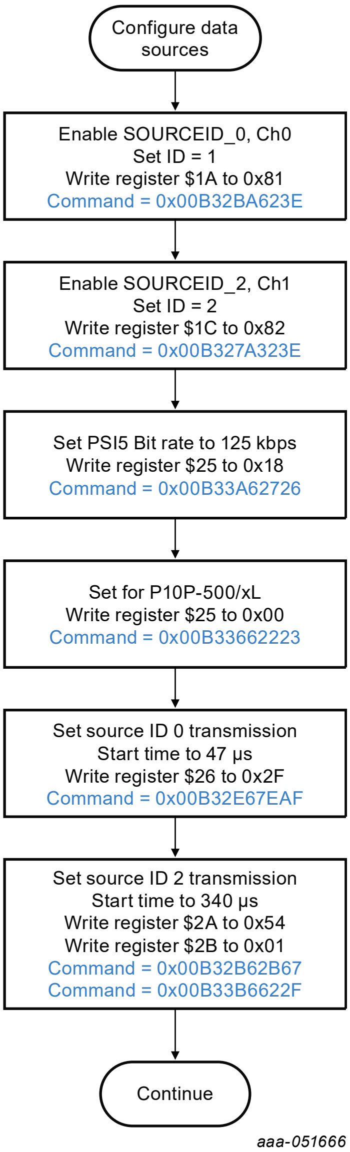

Figure 17. Configure the Data Sources

6.4 Configure the sensor signal chain

For specific use cases, the user can configure the sensor signal chain for each channel. Figure 18 shows an example typical configuration for PSI5. Section 6.4.1, Section 6.4.2, and Section 6.4.3 describe the user configurable options for the signal chain that apply to PSI5 transmissions.

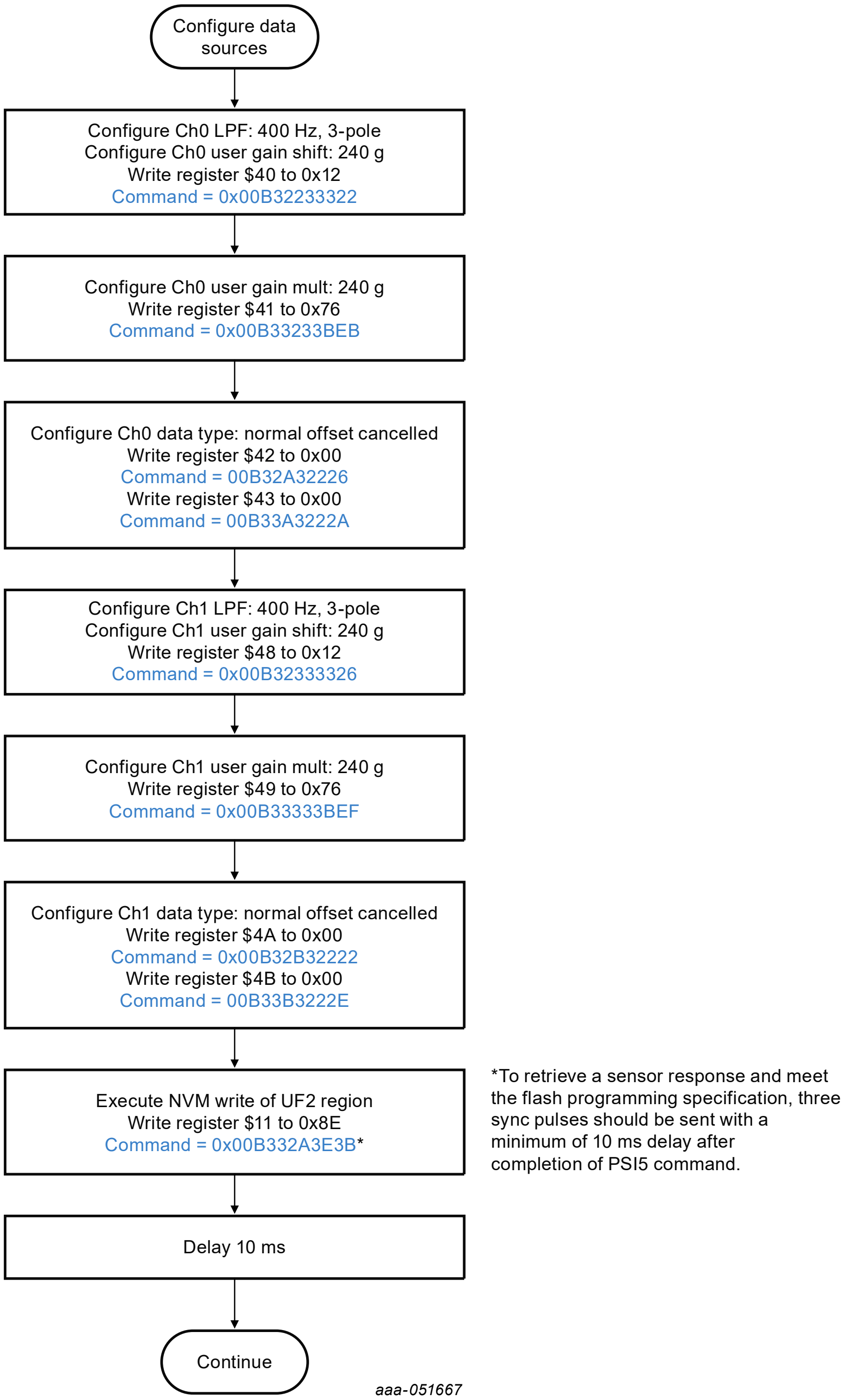

Figure 18. Configure the Sensor Signal Chain

6.4.1 Signal chain low-pass filter selection

A combinaton of the LPF bits and the SAMPLERATE bits in the CHx_CFG_U1 register selects the signal chain low-pass filter as shown in the datasheet. The LPF selection table is shown in Table 10.

Table 10. Signal chain low-pass filter selection

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low-pass filter type		
				SAMPLERATE = 00, 01	SAMPLERATE = 10	SAMPLERATE = 11
				16 µs	32 µs	64 µs
0	0	0	0	400 Hz, 4-Pole	200 Hz, 4-Pole	100 Hz, 4-Pole
0	0	0	1	400 Hz, 3-Pole	200 Hz, 3-Pole	100 Hz, 3-Pole
0	0	1	0	400 Hz, 4-Pole	200 Hz, 4-Pole	100 Hz, 4-Pole
0	0	1	1	400 Hz, 3-Pole	200 Hz, 3-Pole	100 Hz, 3-Pole
0	1	0	0	325 Hz, 3-Pole	162.5 Hz, 3-Pole	81.25 Hz, 3-Pole
0	1	0	1	370 Hz, 2-Pole	185 Hz, 2-Pole	92.5 Hz, 2-Pole
0	1	1	0	180 Hz, 2-Pole	90 Hz, 2-Pole	45 Hz, 2-Pole
0	1	1	1	100 Hz, 2-Pole	50 Hz, 2-Pole	25 Hz, 2-Pole
1	0	0	0	1500 Hz, 4-Pole	750 Hz, 4-Pole	375 Hz, 4-Pole
1	0	0	1	500 Hz, 3-Pole	250 Hz, 3-Pole	125 Hz, 3-Pole
1	0	1	0	800 Hz, 4-Pole	400 Hz, 4-Pole	200 Hz, 4-Pole
1	0	1	1	1200 Hz, 4-Pole	600 Hz, 4-Pole	300 Hz, 4-Pole
1	1	0	0	120 Hz, 3-Pole	60 Hz, 3-Pole	30 Hz, 3-Pole
1	1	0	1	20 kHz, 2-Pole	10 kHz, 2-Pole	5 kHz, 2-Pole
1	1	1	0	120 Hz, 2-Pole	60 Hz, 2-Pole	30 Hz, 2-Pole
1	1	1	1	50 Hz, 4-Pole	25 Hz, 4-Pole	12.5 Hz, 4-Pole

6.4.2 Signal chain user gain selection

A combination of the U_SNS_SHIFT bits in the CHx_CFG_U1 register and the U_SNS_MULT bits in the CHx_CFG_U2 register selects the signal chain user gain. The equation and some example user range and sensitivities are included in the data sheet. The process and equations for determining the U_SNS_SHIFT and U_SNS_MULT settings from desired range and sensitivity values is listed below along with a typical high g PSI5 example.

1. Determine the overall sensitivity adjustment factor:
   - Desired Typical User Range = ±240 g with 10-bit data
   - Calculate Desired Sensitivity:

$$Sense_{Typical\ Desired} = \frac{2^9\text{-}32}{Range_{Typical\ Desired}} = \frac{480}{240} = 2.00\ LSB \Big/ g$$

   - Calculate the required sensitivity adjustment for a High g device:

$$SENSE_{Adjust\ Total} = \frac{Sense_{Typical\ Desired}}{Sense_{Typical\ NXP\ Trim}} = \frac{2.00}{\left(\frac{10.9465}{4}\right)} = 0.7308$$

2. Determine the best U_SNS_SHIFT setting:

$Sense_{AdjustTotal}$	U_SNS_SHIFT Gain	U_SNS_SHIFT Setting
$Sense_{AdjustTotal} < 0.25$	Invalid Range	Invalid Range
$0.25 \le Sense_{AdjustTotal} < 0.50$	0.25	00
$0.50 \le Sense_{AdjustTotal} < 1.00$	0.50	01

$Sense_{AdjustTotal}$	U_SNS_SHIFT Gain	U_SNS_SHIFT Setting
$1.00 \leq Sense_{AdjustTotal} < 2.00$	1.00	10
$2.00 \leq Sense_{AdjustTotal} < 4.00$	2.00	11
$4.00 \leq Sense_{AdjustTotal}$	Invalid Range	Invalid Range

3. Determine the U_SNS_MULT setting:

$$U\ SNS\ MULT = ROUND\left[\left(\frac{Sense_{Typical\ Desired}}{Sense_{Typical\ NXP\ Trim}{*}U\ SNS\ SHIFT} - 1\right) \times 256\right] = \left(\frac{0.7308}{0.50} - 1\right) \times 256 = 118\ decimal$$

$$U\_SNS\_MULT = 0X76$$

6.4.3 Signal chain data type configuration

Each source enabled (as described in Section 6.3.1) must have its data type configured. Datatype configuration is described in the data sheet. Table 11 is a simplified table.

Table 11. Simplified signal chain data type configuration

CHx DATATYPEx[1:0]		Sensor data description
0	0	Offset Cancelled Data as Configured by the OC_FILT bits
0	1	Raw Data (No Offset Cancellation)
1	0	Temperature Sensor Data
1	1	Temperature Sensor Data

6.5 Confirm device status

Once programming is complete, the device reads back the new data from the OTP array and completes the memory verification. If the OTP write fails, the device status includes an error. Figure 19 shows the procedure to confirm the device status.

Note that self-test is not automatically run in PSI5 Programming Mode so the Chx_ERR bits are set due to the ST_INCMPLT bit being set.

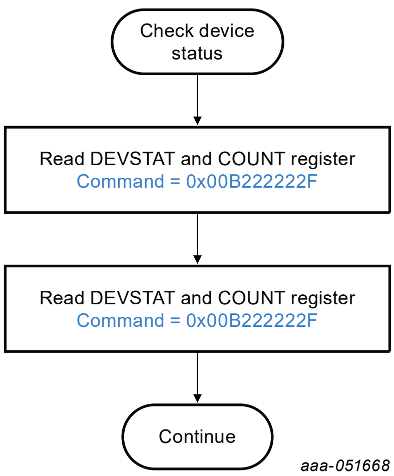

Figure 19. Confirm Device Status

6.6 Optional read verify

If no memory errors are present after the OTP write and register values were verified after each register write during the programming process, then the programming process is complete. An additional read verify can be completed to confirm post OTP programming register values. Figure 20 shows the read verify process.

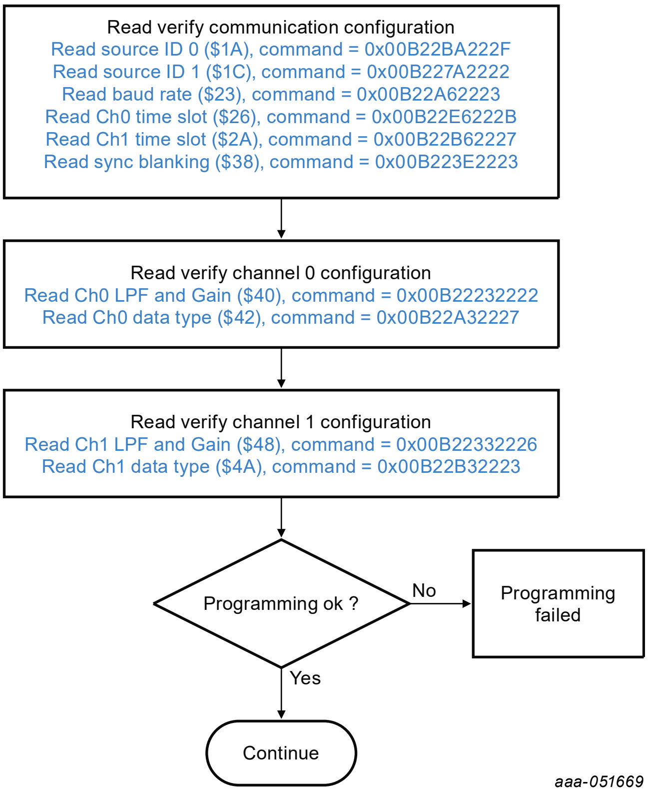

Figure 20. Optional Read Verify

6.7 Optional complete self-test

A self-test procedure will be added to the next revision of this application note.

7 Glossary

Table 12. Glossary of terms

Term	Definition
Analog self-test	A method to test the acceleration signal chain by electrostatically deflecting the transducer proof mass and measuring the device output.
Digital self-test	A method to test the digital portion of the acceleration signal chain by forcing a value or a sequence of values at the output of the analog-to-digital converter and measuring the device output.
DSP	Digital Signal Processing Block
OTP	One Time Programmable Memory
POR	Power-On Reset
PSI5	Peripheral Sensor Interface, fifth Generation. A single controller, multiple secondary communication interface that provides both secondary power and communication on a 2-wire bus.

8 References

[1] FXLS9xxxx, Dual-channel inertial sensor, data sheet, https://www.nxp.com/docs/en/data-sheet/FXLS9xxxx.pdf

[2] FXLS9xxx0, Single channel inertial sensor, data sheet, https://www.nxp.com/docs/en/data-sheet/FXLS9xxx0.pdf

[3] PSI5 Technical Specification Version 2.1, Dated October 8, 2012, https://www.psi5.org/specification

9 Revision history

Table 13. Revision History

Rev	Date	Description
1.1	20231129	• Section 6.2, Figure 15, revised the image adding a note. • Section 6.4, Figure 18, revised the image adding a note. • Section 9, relocated the revision history from the start to the end of the document to conform to NXP's document content hierarchy.
1	20230615	Initial Release

10 Appendix

10.1 Example PSI5 Programming Mode Sequence with Timing

Delta Time (ms)	Time from POR (ms)	Command Type		Register Addr	Register Data	Comment	Full Command (Hex)
6	6	POR Delay	Delay			POR Delay	
7.75	13.75	Startup Delay	Delay			Startup Delay pluse 31 Sync Pulses	FFFFFFFF
3.6	17.35	PME	PME				ACF9
11.25	28.6	XLONG	Write	1A	81	Enable Channel 1 Data	00B32BA623E
11.25	39.85	XLONG	Write	1C	82	Enable Channel 2 Data	00B327A323E
11.25	51.1	XLONG	Write	23	18	Set baud rate to 125 kbit/s	00B33A62726
11.25	62.35	XLONG	Write	26	2F	Channel 0 Timeslot = 47 µs	00B32E67EAF
11.25	73.6	XLONG	Write	27	00	Channel 0 Timeslot = 47 µs	00B33E62226
11.25	84.85	XLONG	Write	2A	54	Channel 1 Timeslot = 340 µs	00B32B62B67
11.25	96.1	XLONG	Write	2B	01	Channel 1 Timeslot = 340 µs	00B33B6622F
11.25	107.35	XLONG	Write	40	12	Channel 0 400 Hz, 3-Pole LPF, 120 g High g	00B32233322
11.25	118.6	XLONG	Write	41	76	Channel 0 400 Hz, 3-Pole LPF, 120 g High g	00B33233BEB
11.25	129.85	XLONG	Write	42	00	Channel 0 Offset cancellation with 0.04 Hz, 1-Pole LPF	00B32A32226
11.25	141.1	XLONG	Write	43	00	Channel 0 Offset cancellation with 0.04 Hz, 1-Pole LPF	00B33A3222A
11.25	152.35	XLONG	Write	48	12	Channel 1 400 Hz, 3-Pole LPF, 120 g High g	00B32333326
11.25	163.6	XLONG	Write	49	76	Channel 1 400 Hz, 3-Pole LPF, 120 g High g	00B33333BEF
11.25	174.85	XLONG	Write	4A	00	Channel 1 Offset cancellation with 0.04 Hz, 1-Pole LPF	00B32B32222

Delta Time (ms)	Time from POR (ms)	Command Type		Register Addr	Register Data	Comment	Full Command (Hex)
11.25	186.1	XLONG	Write	4B	00	Channel 1 Offset cancellation with 0.04 Hz, 1-Pole LPF	00B33B3222E
11.25	197.35	XLONG	Write	14	E0	Enable writes to the PSI5 Init Phase 2 Data Section	00B326A22F3
11.25	208.6	XLONG	Write	E0	44	Protocol = V1.3	00B3227AA6E
11.25	219.85	XLONG	Write	E1	FF	0xFF Supplier Code	00B3327FFFF
11.25	231.1	XLONG	Write	E2	10	High g Sensor	00B32A7A32A
11.25	242.35	XLONG	Write	E3	80		00B33A7A23A
11.25	253.6	XLONG	Write	E4	00		00B3267A22E
11.25	264.85	XLONG	Write	E5	00		00B3367A222
11.25	276.1	XLONG	Write	E6	00		00B32E7A22B
11.25	287.35	XLONG	Write	E7	02	Set Data Code: April 22, 2016	00B33E7B22F
11.25	298.6	XLONG	Write	E8	69	Set Data Code: April 22, 2016	00B3237E6E7
11.25	309.85	XLONG	Write	E9	FF	0xFF Supplier Code	00B3337FFFB
11.25	321.1	XLONG	Write	EA	10	High g Sensor	00B32B7A32E
11.25	332.35	XLONG	Write	EB	80	120 g Sensor	00B33B7A23E
11.25	343.6	XLONG	Write	EC	00		00B3277A22A
11.25	354.85	XLONG	Write	ED	00		00B3377A226
11.25	366.1	XLONG	Write	EE	00		00B32F7A22F
11.25	377.35	XLONG	Write	11	80	Write the PSI5 Initialization Phase 2 data to OTP	00B332A2236
8.75	386.1	Delay	Delay			Delay 10 ms	
11.25	397.35	XLONG	Write	11	8E	Write the Configuration Information to OTP	00B332A3E3B
8.75	406.1	Delay	Delay			Delay 10 ms	
11.25	417.35	XLONG	Read	00	00	Check Status	00B2222222F
11.25	428.6	XLONG	Read	00	00	Check Status	00B2222222F

10.2 PSI5 3-Bit CRC Calculation Examples

10.2.1 3-Bit CRC

Figure 21 shows some example visual basic to calculate the PSI5 XLONG 3-bit CRC.

- Function PSI5XLONGCRC3(SnsAdr As String, FunctionCode As String, RegAdr As String, RegData As String, SEED As String, Poly As String) As String
  - The data is composed of the following concatenated fields:
    - 3-Bit Reversed SnsAdr 100
    - 3-Bit Reversed FunctionCode: 100
    - 8-Bit Reversed RegAdr: 0x40 0000 0010
    - 8-Bit Reversed RegData: 0x12 0100 1000
  - Example: Command = 100 100 0000 0010 0100 1000
  - Example with Start and Sync Bits Command = 010 1 100 1 100 1 000 1 000 1 100 1 100 1 100 1 000 1 0
  - Poly is the 4-bit CRC polynomial in binary
    Example: Polynomial = $X^3 + X + 1$ Poly = 1011

– SEED is the 3-bit CRC Initial value in binary
  Example: Seed = 0 x 7 SEED = 111

In this example, the CRC = 0x0.

```
Function PSI5XLONGCRC3(SnsAdr As String, FunctionCode As String, RegAdr As String, RegData As String, SEED As String, Poly As String) As String

Dim i As Integer
Dim m As Integer
Dim n As Integer
Dim k As Integer
Dim bit As Integer
i = 1
m = 1
n = 1
k = 1
bit = 0
Dim RTest As String
Dim Data As String
Dim CRC(1 To 3) As String
Dim CRC_old(1 To 3) As String
Data = SnsAdr & FunctionCode & RegAdr & RegData & "000"
For i = 1 To 3
   CRC(i) = Mid(SEED, i, 1)
   CRC_old(i) = Mid(SEED, i, 1)
Next i

For n = 1 To 25
   RTest = CRC(1) & CRC(2) & CRC(3)
   bit = Mid(Data, n, 1)
   For k = 1 To 3
      CRC_old(k) = CRC(k)
   Next k
```

```
For m = 1 To 3
      If Mid(Poly, m + 1, 1) = 0 Then
         If m = 3 Then
            CRC(m) = bit
         Else
            CRC(m) = CRC_old(m + 1)
         End If
      Else
         If m = 3 Then
            If CRC_old(1) = 1 Then
               If bit = 1 Then
                  CRC(m) = 0
               Else
                  CRC(m) = 1
               End If
            Else
               If bit = 1 Then
                  CRC(m) = 1
               Else
                  CRC(m) = 0
               End If
            End If
         Else
            If CRC_old(1) = 1 Then
               If CRC_old(m + 1) = 1 Then
                  CRC(m) = 0
               Else
                  CRC(m) = 1
               End If
            Else
               If CRC_old(m + 1) = 1 Then
                  CRC(m) = 1
               Else
                  CRC(m) = 0
               End If
            End If

         End If
      End If
   Next m
Next n
PSI5XLONGCRC3 = CRC(1) & CRC(2) & CRC(3)
End Function
```

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Figure 21. PSI5 XLONG, 3-Bit CRC Visual Basic

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Tables

Figures

Contents

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