AN13768

Switch LCD Display On/Off in Low-Power Mode on i.MX RT1170

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Document information

Information	Content
Keywords	AN13768, RT1170, MIPI DSI, Low-power mode
Abstract	This application note describes how to add low-power mode operation on the MIPI DSI host controller and LCDIFv2 controller.

1 Introduction

This application note describes how to add low-power mode operation on the Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) host controller and LCDIFv2 controller. It is done to drive a DSI-compliant LCD panel on i.MX RT1170 to switch off and then back on again.

In this application note, software mode is used to enter and exit from the sleep mode and DISPLAY MIX is switched off to save maximum power. This document uses SSARC to save and restore LCDIFV2 and Video mux related registers when it is switched off and switched on back. Here, we have modified the `clock_freertos (vglite_examples)` included with the SDK to understand how to power up and power down the display. The `clock_freertos` project shows how to drive the TFT panel using the LCDIFv2 driver. The example toggles between display off and on for certain interval in an infinite loop.

Note: *The code is simple and not extensive since it focuses on how to power on and off display rather than providing an implementation for product. For GPU internal low-power mode, an API is added to power on GPU from deep sleep.*

2 MIPI DSI host controller

The MIPI DSI is a versatile, high-speed interface for LCD displays in smartphones, automotive, and other platforms.

MIPI DSI controller of i.MX RT1170 implements all protocol functions defined in MIPI DSI specification. It provides an interface that allows communication between MCUs and MIPI DSI-compliant LCDs.

MIPI DSI D-PHY of i.MX RT1170 is a high-frequency and low-power physical layer that supports the MIPI Alliance Standard for D-PHY and provides a physical implementation for DSI.

2.1 DSI host controller core

Figure 1 shows the DSI layer definitions of DSI specification. The MIPI DSI controller of the i.MX RT1170 implements all three DSI layers (lane management, low-level protocol, and application).

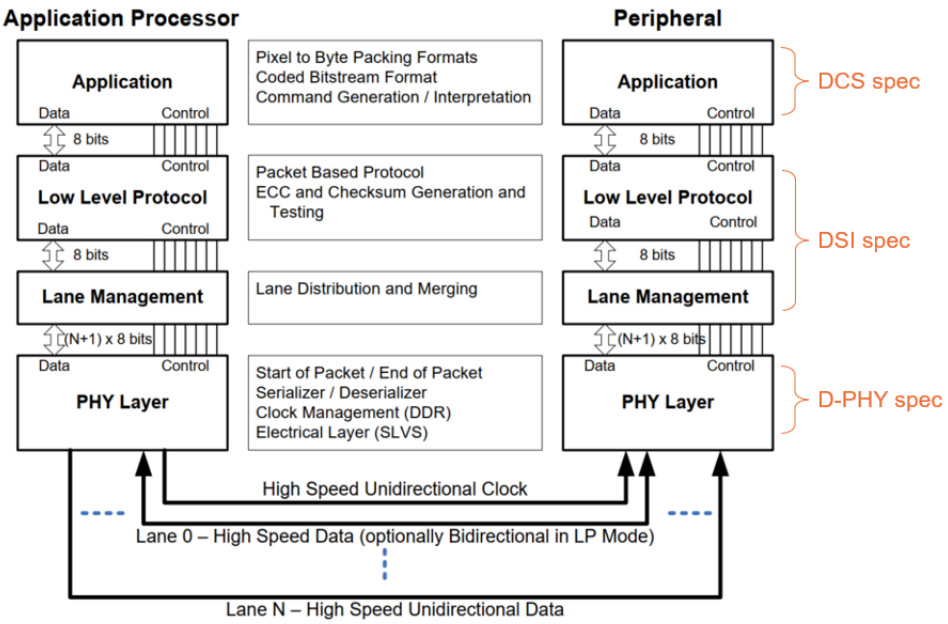


Figure 1. DSI layers

MIPI DSI uses differential signals to transmit clock and data between DSI host and display module. It includes 1 clock lane and 1~4 data lanes. For DSI controller in i.MX RT1170, it can support 1 clock lane and up to 2 data lanes. DSI greatly reduces the number of data and signal lines compared to the parallel interface, which saves hardware resources.

DSI-compliant LCD supports two basic modes of operation: Command mode and Video mode. The architecture and capabilities of the LCD decide which mode is used.

Command mode refers to an operation in which transactions primarily send commands and data to a display module. The display module may include local registers and a compressed or an uncompressed frame buffer.

Video mode refers to an operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. Video information should be transmitted using high-speed mode. Figure 2 shows examples for Command and Video modes.

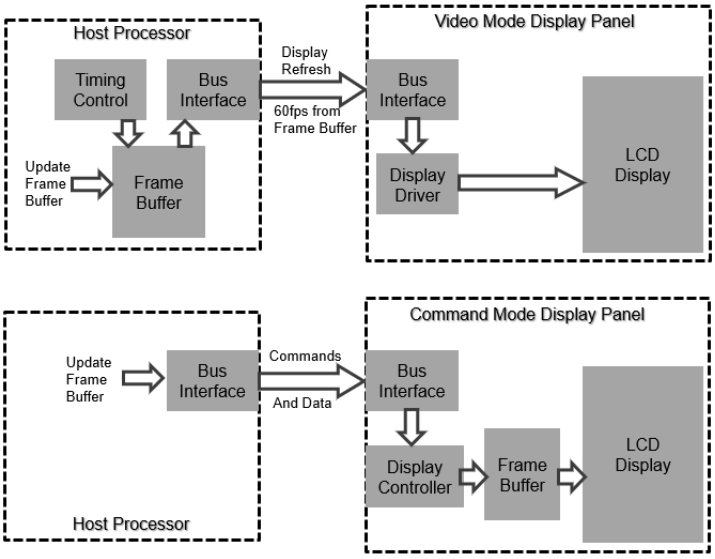


Figure 2. Examples for Command and Video modes

In general, MIPI DSI controller provides the following key features:

- Supports for Command and Video modes
- Scalable data lane support, 1 to 2 data lanes
- Supports high-speed and low-power operation
- Flexible packet-based user interface
  - APB interface option (status and control)
  - Display Pixel Interface Core (DPI-2) option

Figure 3 shows the DSI host controller core structure.

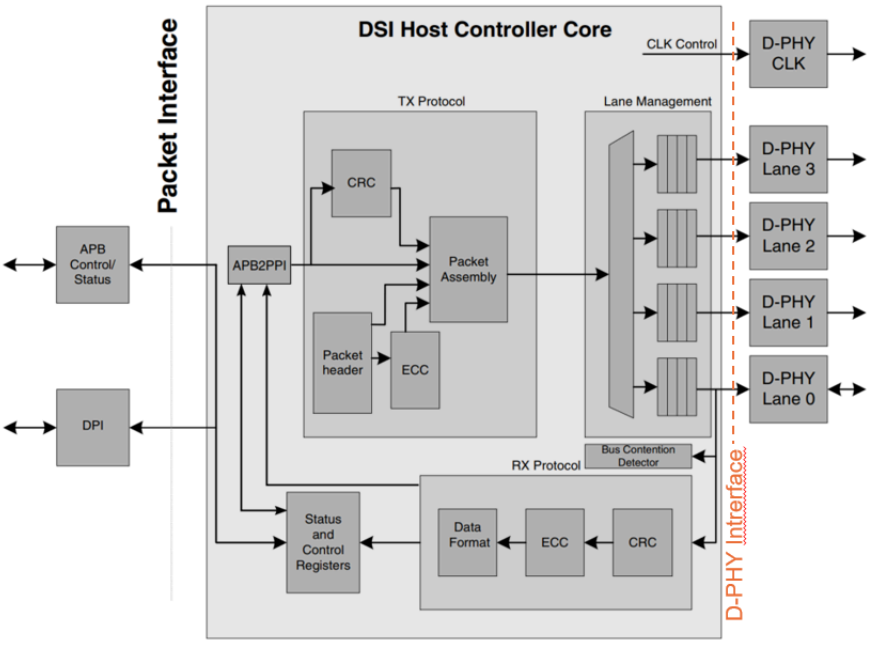


Figure 3. DSI host controller core block diagram

D-PHY interface connects directly to MIPI PPI-compliant D-PHYs, described in further sections.

DSI host controller core sends and receives DSI commands and data via packet interface. There are two packet-based interfaces: APB interface and Display Pixel (DPI-2) interface.

3 LCDIFv2 controller

The i.MX RT1170 includes the enhanced Liquid Crystal Display Interface (eLCDIF) and the LCDIF Interface version 2 (LCDIFv2). They are both display controllers used to fetch graphics stored in memory and display them on an LCD panel.

This chapter mainly introduces LCDIFv2 controller. LCDIFv2 includes the following features:

- Support RGB interface only
- Display layers can support up to maximum 8 layers of alpha blending
- Support one parallel camera interface input and typical data formats of CSI-2: 16 bpp (YUV422 8-bit), 24 bpp (RGB888), 18 bpp (RGB666), 16 bpp (RGB565), 15 bpp (RGB555), 12 bpp (RGB444)

3.1 RGB interface

RGB interface is the mode used in moving picture displays. It includes VSYNC, HSYNC, DOTCLK, and ENABLE signals.

LCD (TFT) display with RGB interface can drive three segments (1 pixel) per clock with variable electric field strength. The RGB interface provides the following features:

- Supports many colors
- Always supports 1 pixel per clock (three segments of Red, Green, and Blue)
- Contains the color levels depending on the number of data lines on the LCD panel and the number of LCD controller data output signals. It may be 24 lines, 24 bits per pixel (bpp), or 18 bpp, 16 bpp
- Supports the parallel data interface. 1 clock requires 24 bits (or other formats) for 1 pixel

For the LCD RGB interface, on every pixel clock edge (rising or falling) and within the LCD active area, the controller fetches one-pixel of data from its FIFO. Then, the controller converts it to the pixel panel format (coded in the RGB888 or other formats), puts it in the signal generator unit, and drives out to the RGB interface. The pixel data is then displayed on the screen.

To drive correct picture on LCD, some timing parameters should be considered for a size of LCD display. The parameters should be programmed to match the display specifications.

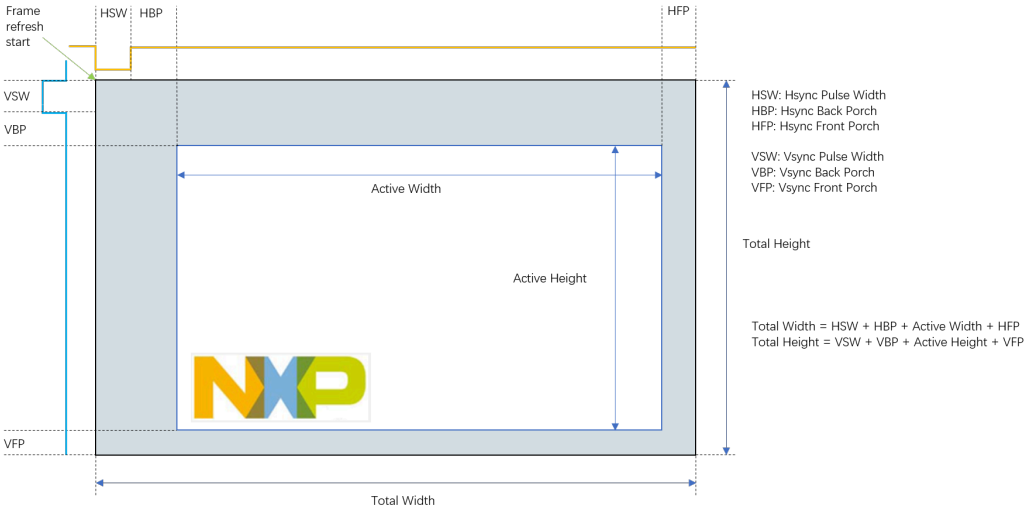


Figure 4. Programmable timings and resolution

4 Video mux controller

The i.MX RT1170 supports various LCD/camera interfaces and display controllers, so a video mux controller is used to provide mux control between interfaces and controllers.

Figure 5 shows the video mux block. For example, LCDIFv2 can be selected to control MIPI DSI.

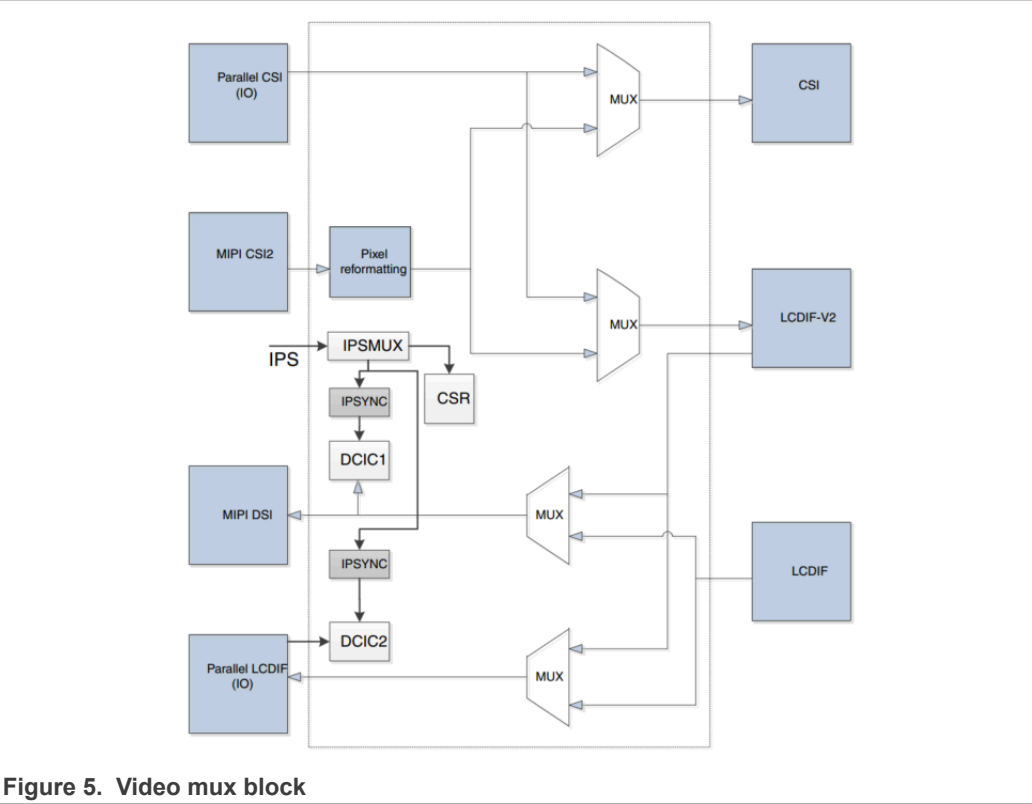


Figure 5. Video mux block

5 Low-power modes

The i.MX RT1170 provides new power and clock architecture design. Compared to the previous i.MX RT10xx family MCUs, software, hardware, or a combination of both can control the i.MX RT1170 power and clock state.

Software or hardware can control each module. For most of the modules, a combination of hardware and software control is allowed (PGMC, SRC, CCM, and PMU). The rest of the modules allows exclusive control by software or hardware (DC-DC).

5.1 Software control mode

When the software control mode is selected for the appropriate module, the application code becomes responsible for the module settings and module behavior. The application code must follow all the recommendations, such as the power-up and power-down sequences, PLL enable sequences, and so on. When any changes of the clock or power settings are requested, the application code must check if the planned change is valid and ensure that all the changes are executed in a correct order. Otherwise, the chip behavior can be unpredictable or unstable. The software control is the default control mode of all modules.

5.2 Hardware control mode

When the hardware control mode is selected, the application code determines the hardware control mechanism used for each resource. The i.MX RT1170 controls the resources (modules) via the CPU mode control, Setpoint mode control, or Standby mode control. The state of the CPUs, preconfigured setpoint, and enabled or disabled Standby mode defines the final power mode of the whole MCU. There are 4 states of the CPU (Run, Wait, Stop, or Suspend) and 16 preconfigured setpoints.

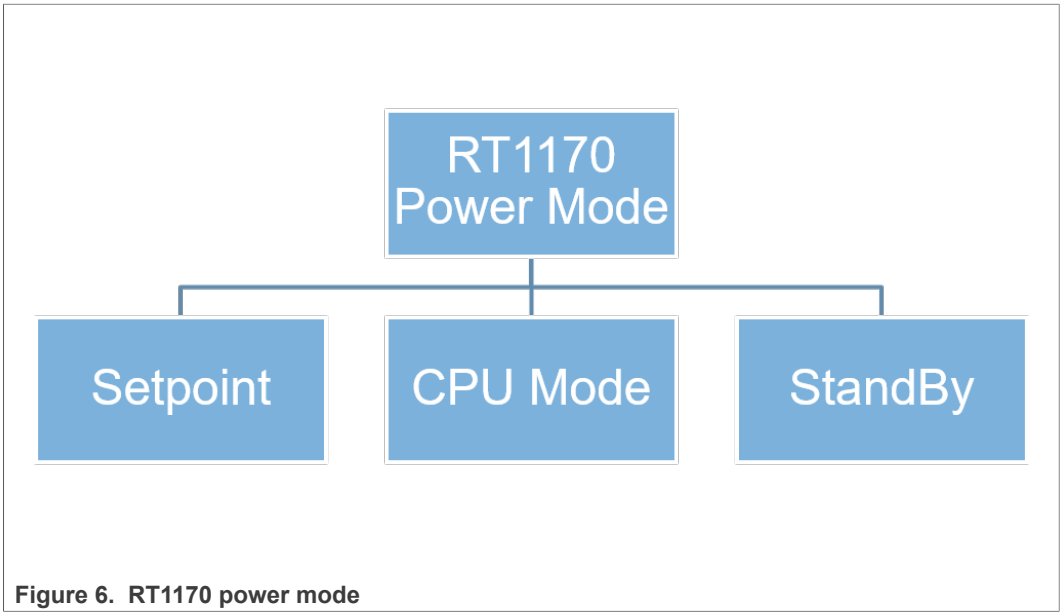


Figure 6. RT1170 power mode

The advantages of this mode are that the General Power Controller (GPC) takes responsibility for correct power-up and power-down sequences, setpoints transition sequences, and so on. Even in the hardware control mode, incorrect settings can be

created, but the chip hardware can check most of the consequences. It does not allow the mode transition into an invalid configuration.

5.3 Power Gating and Memory Controller (PGMC) settings

The PGMC consists of three submodules which control each power domain. These submodules are the Basic Power Controller (BPC), CPU Power Controller (CPC), and PMIC Power Controller (PPC). Table 1 shows the general PGMC control options. For more information about domain assignment, see section 20 of *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM).

Table 1. PGMC general control settings

	CPU mode control CM7 domain	CPU mode control CM4 domain	Setpoint mode control	Standby mode control	Software control mode
BPC0 - MEGAMIX	√	√	√		√
BPC1 - DISPLAYMIX	√	√	√		√
BPC2 - WAKEUPMIX	√	√	√		√
BPC3 - LPRSMIX	√	√	√		√
BPC4 - MIPIPHY	√	√	√		√
CPC0 - CM7 core platform	√		√ (MLPL only)		√
CPC1 - CM4 core platform		√	√ (MLPL only)		√
PPC0 - PMIC control			√	√	√

6 State Save and Restore Controller (SSARC)

The SSARC saves the registers of functional modules in a memory (Located in the LPSR domain) before powering down and restores the registers from memory after the module is powered up. This module configures a peripheral before the CPU wakes up. Once the CPU wakes up, it can use the peripheral without initialization. Figure 7 shows the basic functions of SSRAC.

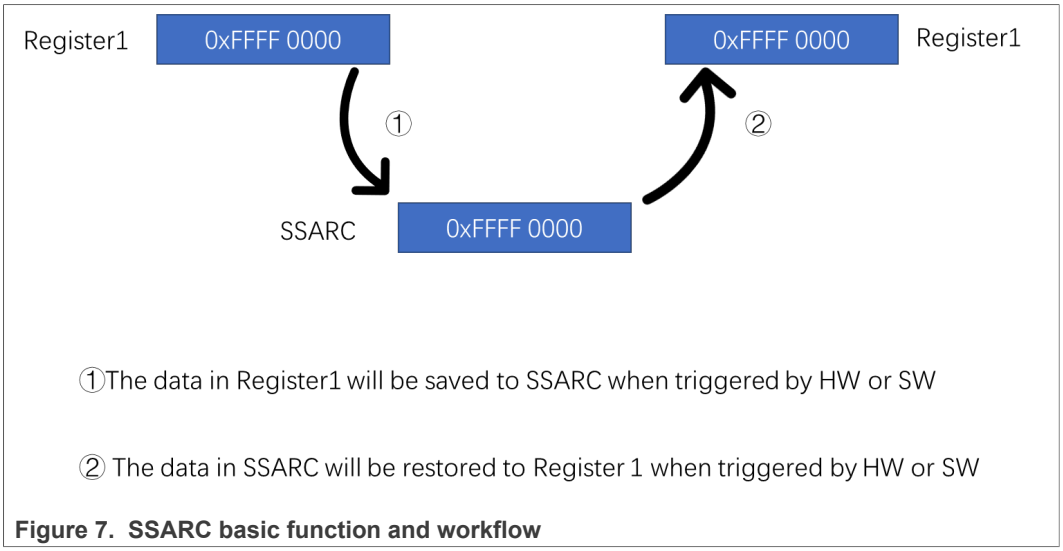


Figure 7. SSARC basic function and workflow

6.1 Descriptor

Descriptor is the most basic element in SSARC. The SSARC has up to 1024 descriptors. The descriptor supports most operations like CPU, such as write, read, delay, and polling.

It supports 4 operations and 7 types of operation:

Operations:

- Save disable and restore disable
- Save enable and restore disable
- Save disable and restore enable
- Save enable and restore enable

Type of operation:

- Read value and write back
- Write a fixed value
- Read a register or with a value then write it back (OR)
- Read a register and with a value then write it back (AND)
- Delay several cycles (delay)
- Read a register until the bit or bits in it changed to 0 (polling 0)
- Read a register until the bit or bits in it changed to 1 (polling 1)

6.2 Group

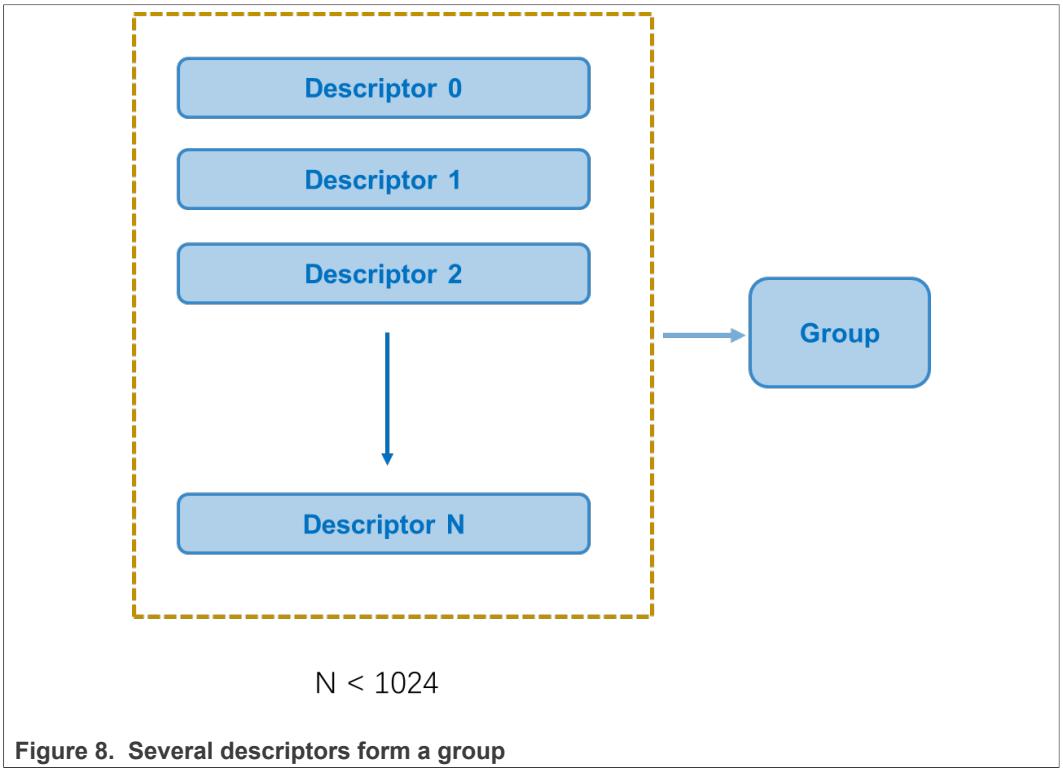


Figure 8. Several descriptors form a group

The 1024 descriptors can be divided into 16 groups that control the descriptors. Each group contains a number of continuous descriptors. The group can be triggered by software or hardware. Each group has its own priority for both saving and restoring. There are 16 priority settings from 0 to 15, and 0 has the highest priority. Usually, the save operation does not need to care about the priority, but the restore operation must care. Such as, if a peripheral needs to use a pin, the initialization of the pins should have a higher priority than other settings.

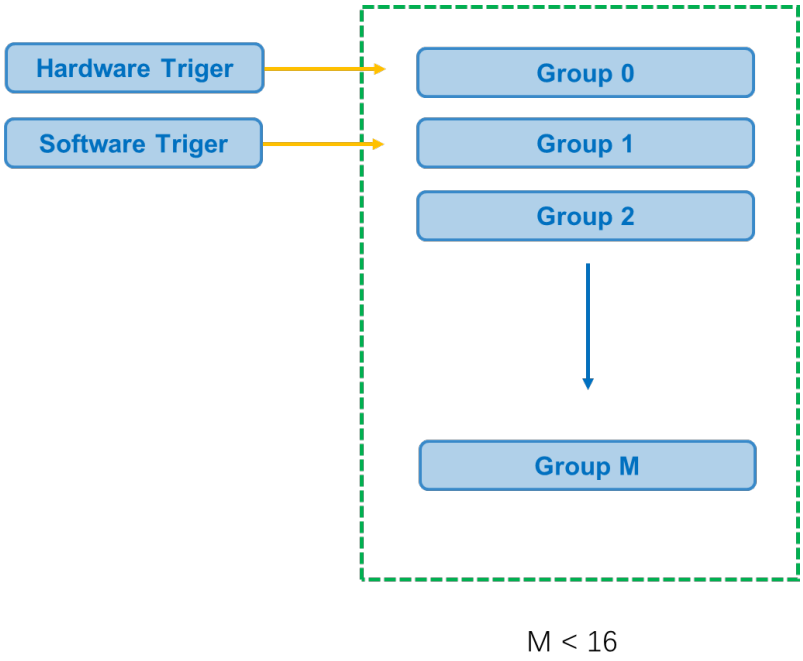
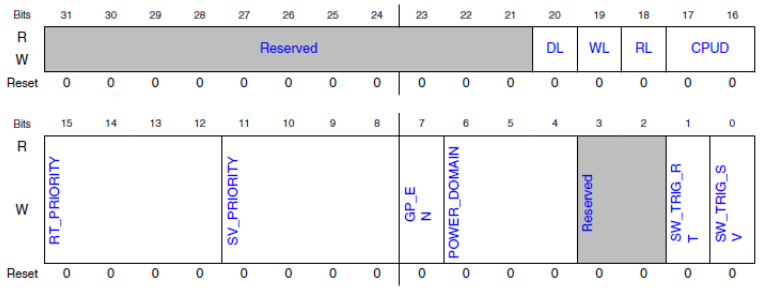


Figure 9. Hardware or software triggering a group

6.2.1 Group trigger by software

The software trigger method can be used to verify whether the SSARC settings are correct or not before entering the low power. The bit 0 and bit 1 in `DESC_CTRL1_x` (x means index for each group) can use software trigger for saving and restoring operations.

Figure 10. SW trigger group register in `DESC_CTRL1_x`



Besides this register, there is an API for save and restore:

```
void SSARC_TriggerSoftwareRequest(SSARC_LP_Type *base, uint8_t
 groupID, ssarc_software_trigger_mode_t mode)
```

See the software trigger example in SDK at `boards\evkmimxrt1170\driver_examples\ssarc\software_trigger`.

7 API added to application for display on and off scenario

7.1 API added at application

Display power down:

Display power down is achieved by using `Display_Powerdown` API. As part of this API, SSARC module is requested to save all required registers needed by LCDIFV2 and Video mux module using API `SSARC_TriggerSoftwareSave`. PGMC module is requested to power off the domain: DISPLAY_MIX (BPC 1) and MIPIPHY (BPC 4) using API `PGMC_BPC_ControlPowerDomainBySoftwareMode`.

Display power up:

Display power up is achieved by using `Display_Powerup` API. As part of this API, first PGMC module is requested to switch on power for DISPLAY_MIX (BPC 1) domain followed by resetting display mix using API `BOARD_ResetDisplayMix`. Then, the SSARC module is called to restore registers for LCDFIV2, and Video mux using API `SSARC_TriggerSoftwareRestore`. Then, the GPU is powered up calling API `GPU_Powerup` which resets and re-initialize GPU after power on from deep sleep. At the end, MIPI is powered up using `MIPI_Powerup` API. For powering on MIPI module, first Video mux and MIPI clocks are enabled, and MIPI is powered on. This process is followed by asserting MIPI software reset (MIPI DSI APB clock domain, MIPI DSI Byte clock domain, MIPI DSI Pixel clock domain, and MIPI DSI Escape clock domain). Afterward, deassert software reset for the MIPI DSI APB clock domain and ESC clock domain, configure the peripherals, and deassert software reset for the MIPI DSI Byte clock domain and MIPI DSI Pixel clock domain. The last part is to configure the LCD.

Note: *Remember the sequence in which LCDIFV2 and Video mux registers are saved and should be followed as provided in the application note software.*

8 Run the demo

There is a project named `clock_freertos` in the i.MX RT1170 SDK package provided as part of this application note software. The project demonstrates the LCDIFv2 controller, MIPI DSI host controller functionalities, and vglite driver.

8.1 clock_freertos

The `clock_freertos` demo can be found in the `boards\evkmimxrt1170\vglite_examples\clock_freertos` directory for i.MX RT1170 SDK provided with the software package for this application note. The project can also be imported using MCUXpresso IDE import projects from the file system option. The demo application displays a clock with high render quality on the screen, and the screen is switched on and off continuously.

Build, download, and run the demo on i.MX RT1170-EVK to drive a 720 × 1280 LCD panel. The LCD is connected to the board via the MIPI DSI interface. Once the board is switched on, notice a high-render quality clock on display, with display being switched on and off at a particular interval.

9 Conclusion

This application note describes the use case of adding low-power mode operation to display. For more information, refer to:

- *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM)

- The `readme.txt` file in the `clock_freertos` demo

10 References

- *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM)
- *Use Case of RT1170 LCD Display System based on MIPI DSI* (document AN12940)
- *I.MXRT1170 Low-Power Modes* (document AN13148)

11 Revision history

Table 2 summarizes the changes done to this document since the initial release.

Table 2. Revision history

Revision number	Date	Substantive changes
0	05 December 2022	Initial release

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