AN13863

NXP PMIC Solution for Black Sesame A1000L/A1000 Processor

Rev. 1.1 — 13 June 2023 Application note

Document Information

Information	Content
Keywords	Power solution, BYLink, Black Sesame, BST, A1000L, A1000, PF81, PF82, FS56, FS86
Abstract	This application note presents how to use NXP Power Management Integrated Circuit (PMIC) PF81/82 to power the Black Sesame A1000L/A1000 processor system.

1 Revision history

Revision history

Rev	Date	Description
1.1	20230613	Replaced all occurrences of "SC33PF8200JZES" to "SC33PF8200KCES"
1.0	20230417	Initial release

2 Introduction

NXP PF8x00 family of high-integration/high-performance Power Management ICs (PMIC) is designed for high-performance processing applications, such as infotainment, telematics, clusters, vehicle networking, Advanced Driving Assistance Systems (ADAS), vision, and sensor fusion. The devices provide a power solution that meets all Black Sesame A1000L/A1000 power rails and functional safety features requirements. A wide range of customers have already selected PF8x00 as the PMIC of choice in their Black Sesame A1000L/A1000 system designs.

This application note shows the power solution using NXP PF81/82 to power Black Sesame A1000L/A1000 devices. This document also introduces the total power tree for an A1000L/A1000 system that includes the SOC and its associated peripherals with one DCDC that powers its core voltage.

3 Black Sesame A1000L/A1000 SOC and NXP PMIC Overview

Black Sesame Technology (BST) is an autonomous driving computing chip manufacturer. Black Sesame's A1000L/A1000 System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS) and Autonomous Driving System (ADS). The A1000 family is a design solution for heterogenous multi-core architecture with self-developed DynamAI NN and NeuralIQ ISP integration. A1000L is the Lite version. Furthermore, the built-in GPU, DSP, and Safety and Security MCU constitute an optimal function combination for an ADAS/ADS domain controller. With the multi-perception fusion, low power consumption and powerful AI computing capability, the A1000L/A1000 platform enables comprehensive board level ADAS/ADS applications to be implemented.

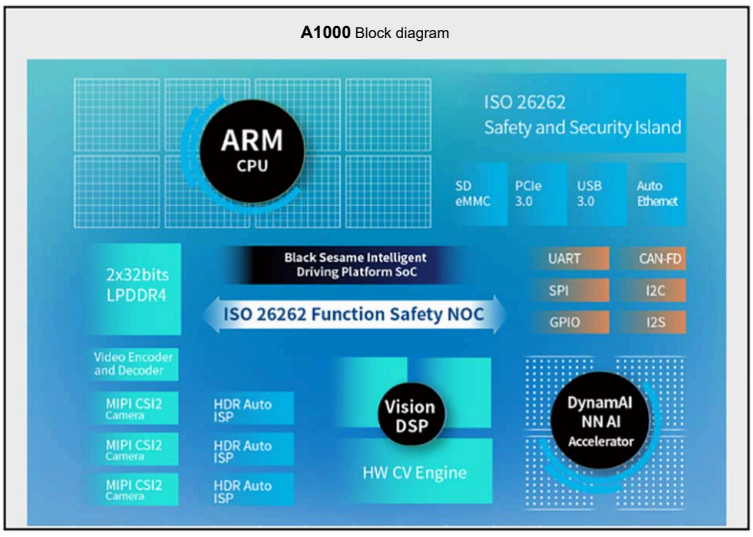

Figure 1. A1000 Block Diagram

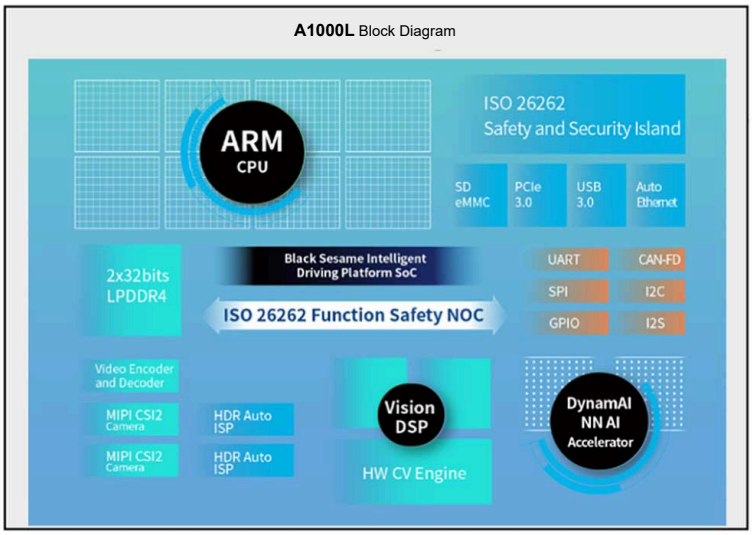

Figure 2. A1000L Block Diagram

PF81/82 devices are high-integration PMICs designed for high-performance processor-based systems. These devices belong to the LV PMIC family. LV PMICs have a similar design structure and can be used to work together in system by logic connection and power companion. PF81 is a QM device, and PF82 is an AsilB level device, which have safety features such as self-test, fail-safe state, secure I^2C, etc. The block diagram for PF81/82 family device is shown in Figure 3.

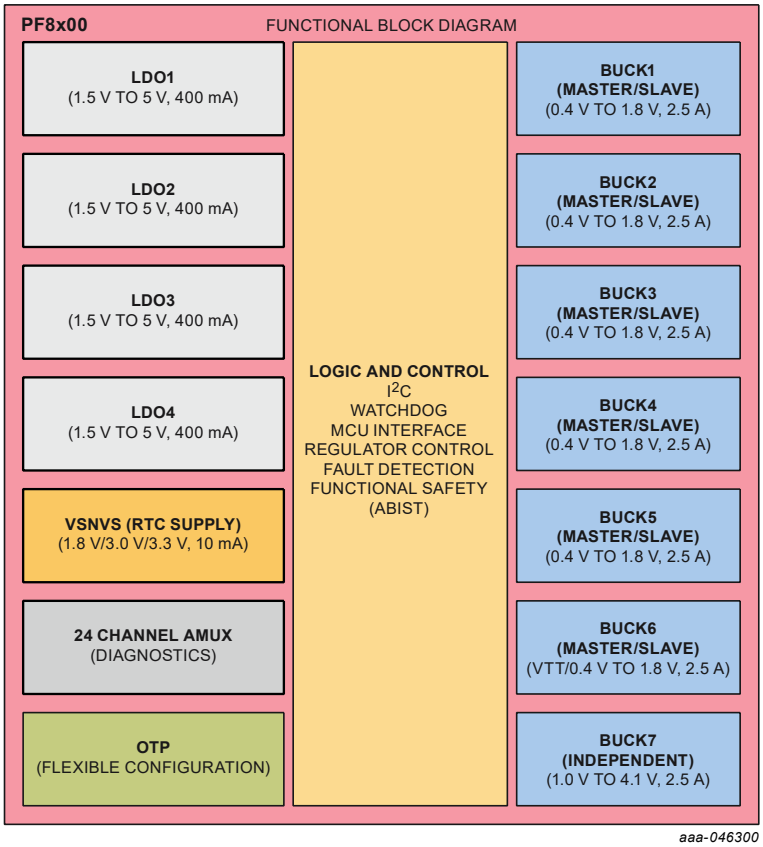

Figure 3. PF81/PF82 Device Function Block Diagram

The BYLink system power platform provided by NXP includes HV PMICs (high-voltage PMICs) and LV PMICs (low-voltage PMICs). BYLink is a simple and effective way to deliver scalable safety and power solutions as part of a platform strategy.

For Automotive applications, HV PMICs that can be powered directly by 12 or 24 V battery systems are required in many customer systems. NXP provides a complete portfolio of PMICs with embedded system features. FS56, FS86 series HV PMICs can be chosen as front power devices, optionally. These PMICs have one HV BUCK with up to 15 A output capability. This output can facilitate using one intermediate voltage, thereby replacing discrete battery connected regulators in the system, while providing value in functional safety and integration. Figure 4 and Figure 5 show the block diagrams of FS56 and FS86 family devices.

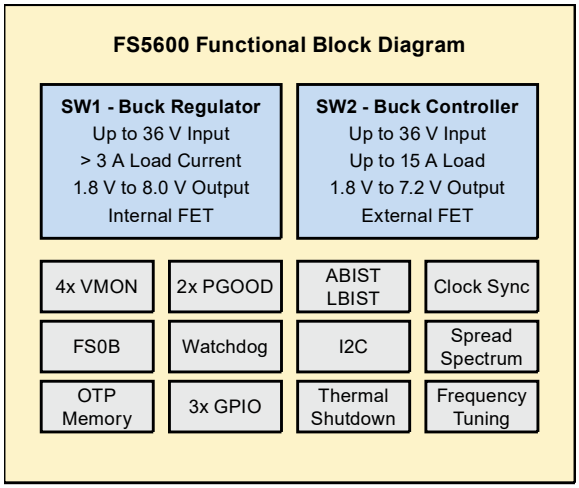

Figure 4. FS56 function block diagram

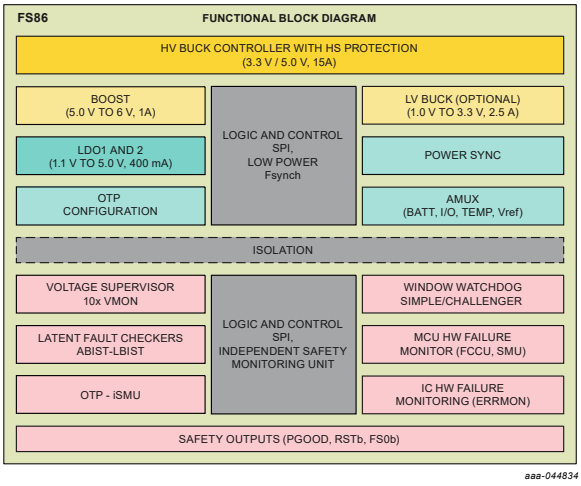

Figure 5. FS86 function block diagram

4 A1000L/A1000 power solution introduction

To implement the NXP power solution for the Black Sesame A1000L/A1000 processor, a low-voltage PMIC PF81/82 is suitable. Figure 6 shows a Black Sesame A1000L/A1000 system power solution block diagram. Table 1 lists the key signals related to the safety power solution.

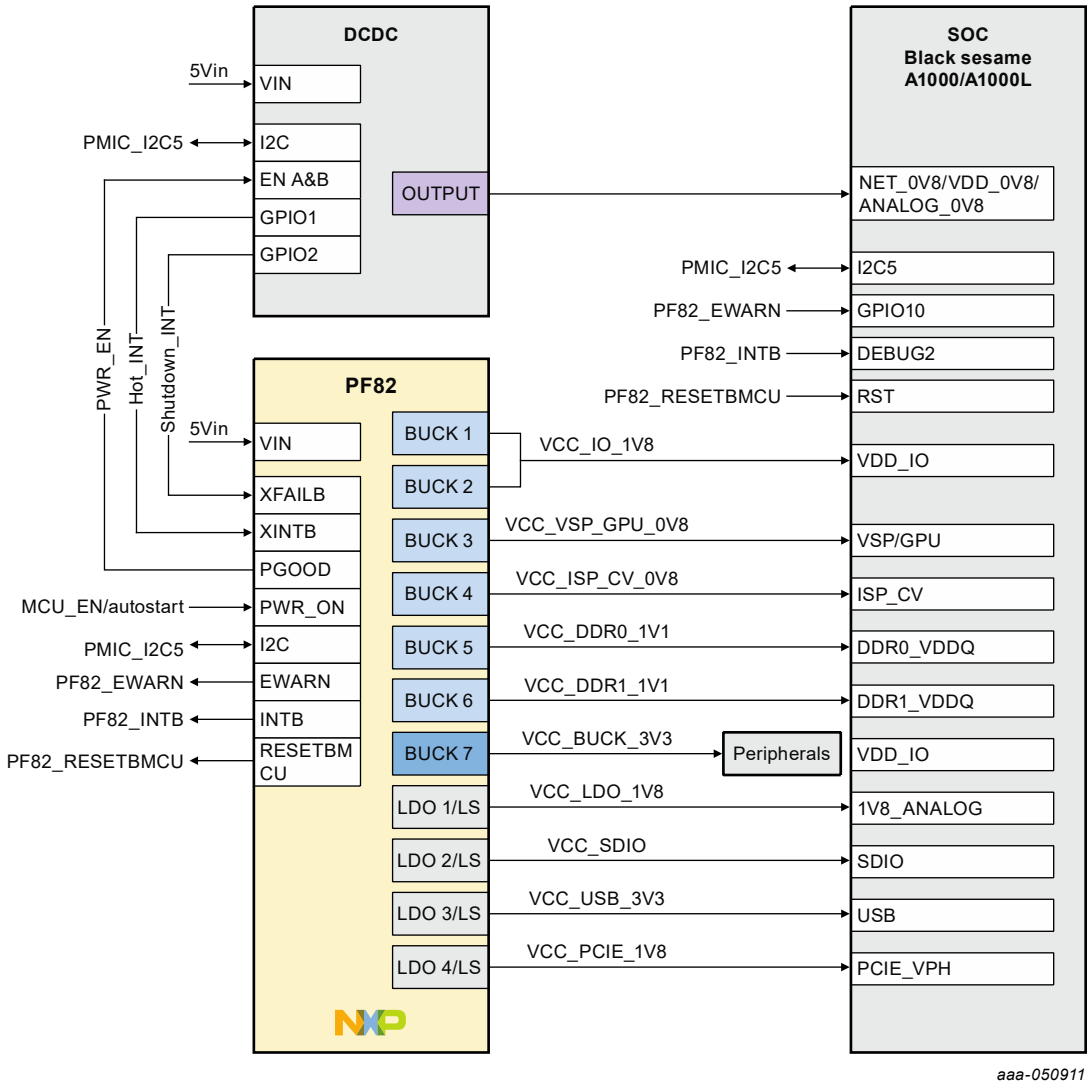

Figure 6. NXP PF8200 power solution for Black Sesame A1000L/A1000

Table 1. Key signals related to the safety power solution

Signal name	PF8200	DCDC	A1000L/ A1000	Function
MCU_EN/Autostart	PWRON	—	—	Enable PF82 power-up from MCU or pull high automatically
PMIC_I2C5	SCL and SDA	I^2C pins	I2C5	I^2C communication to each device
PF82_EWARN	EWARN	—	GPIO10	PF82 notify A1000L/A1000 that an imminent power failure is about to occur
PF82_INTB	INTB	—	DEBUG2	Interruption from PF82 that can make sense to A1000L/A1000
PF82_RESETBMCU	RESETBMCU	—	RST	PF82 active low output used to bring A1000L/A1000 to reset
PWR_EN	PGOOD	EN A&B	—	The PGOOD pin of PF82 acts as GPO to enable DCDC
Hot_INT	XINTB	GPIO1	—	An interruption from DCDC
Shutdown_INT	XFAILB	GPIO2	—	Shutdown interrupt that can let PF82 execute its power-down sequence

In this application, the recommended PF82 part number for A1000L/A1000 is SC33PF8200KCES(R2). The OTP version is defined by Black Sesame and NXP. The OTP configuration report is available to customers who will use the NXP power solution.

Notes:

1. *For tape and reel, add an R2 suffix to the part number.*
2. *SC~ is NXP customed mass production.*

In this solution, an external DCDC provides core voltage that could provide large current for a A1000L/A1000 processer. PF82 provides the voltages of DDRs, PCIE, USB, IOs, GPU and other peripherals. The PF82 power-up and power-down sequences can sync with the external DCDC with the PGOOD pin assert to high.

5 Power-up and power-down sequences

This application note shows typical NXP PMIC designs for an A1000L/A1000 device system. Table 2 shows the design parameters of PF82 attach A1000L/A1000 solution, including detailed PMIC power tree configurations, power-up sequences, and current capability of each power rail.

Table 2. Design parameters of SC33PF8200KCES attach A1000L/A1000 solution

Item	Power config	Voltage (V)	Max current capability (A)	System power rail	Power up delay
1	PF82 SW1-2	1.8	5	VDD_IO	1.08 ms–slot9
2	PF82 SW3	0.8	2.5	VSP / GPU	2.64 ms–slor22
3	PF82 SW4	0.8	2.5	ISP_CV	2.64 ms–slor22
4	PF82 SW5	1.1	2.5	DDR0_VDDQ	2.64 ms–slor22
5	PF82 SW6	1.1	2.5	DDR1_VDDQ	2.64 ms–slor22
6	PF82 SW7	3.3	2.5	Other device	1.08 ms–slot9
7	PF82 LDO1	1.8	0.4	1V8_ANALOG	3.12 ms–slot26
8	PF82 LDO2	3.0	0.4	SDIO	1.08 ms–slot9
9	PF82 LDO3	3.3	0.4	USB	1.56 ms–slo13
10	PF82 LDO4	1.8	0.4	PCIE_VPH	2.06 ms–slot17
11	PF82 RESETBMCU	—	—	RST	9.12 ms–slot76
12	PF82 PGOOD	—	—	EN_A&B	2.52 ms–slor21

If SC33PF8200KCES cannot meet a customer's requirement, PF8x can also support customized OTP configurations. NXP PMICs feature a built-in One-Time Programmable (OTP) memory that stores key startup configurations. Users define the OTP configuration based on their specific application requirements. The default sequence slot for PMICs are programmed via the OTP configuration registers. The sequence slot includes Time base and Time slot to realize a flexible power-up\power-down sequence configuration. There are 255 sequence time slots for each regulator, PGOOD, RESETMCU can be set from 0 to 254. Time base has four options: 30 µs, 120 µs, 250 µs and 500 µs. The LV PMICs feature a dedicated functional block for synchronizing power-up sequences from multiple PMICs. XFAILB is a bidirectional pin with an open drain output used to synchronize the power up and power down sequences of multiple LV PMICs.

Figure 7 and Figure 8 show the SC33PF8200KCES power-up\power-down configuration for the requirement of A1000L/A1000. In this application, the PGOOD of SC33PF8200KCES is used as a GPO, that enables the DCDC power up. Once a fault occurs in the DCDC, the GPIO2 of DCDC asserts the XFAILB to low that PF82 will execute its power-down sequence.

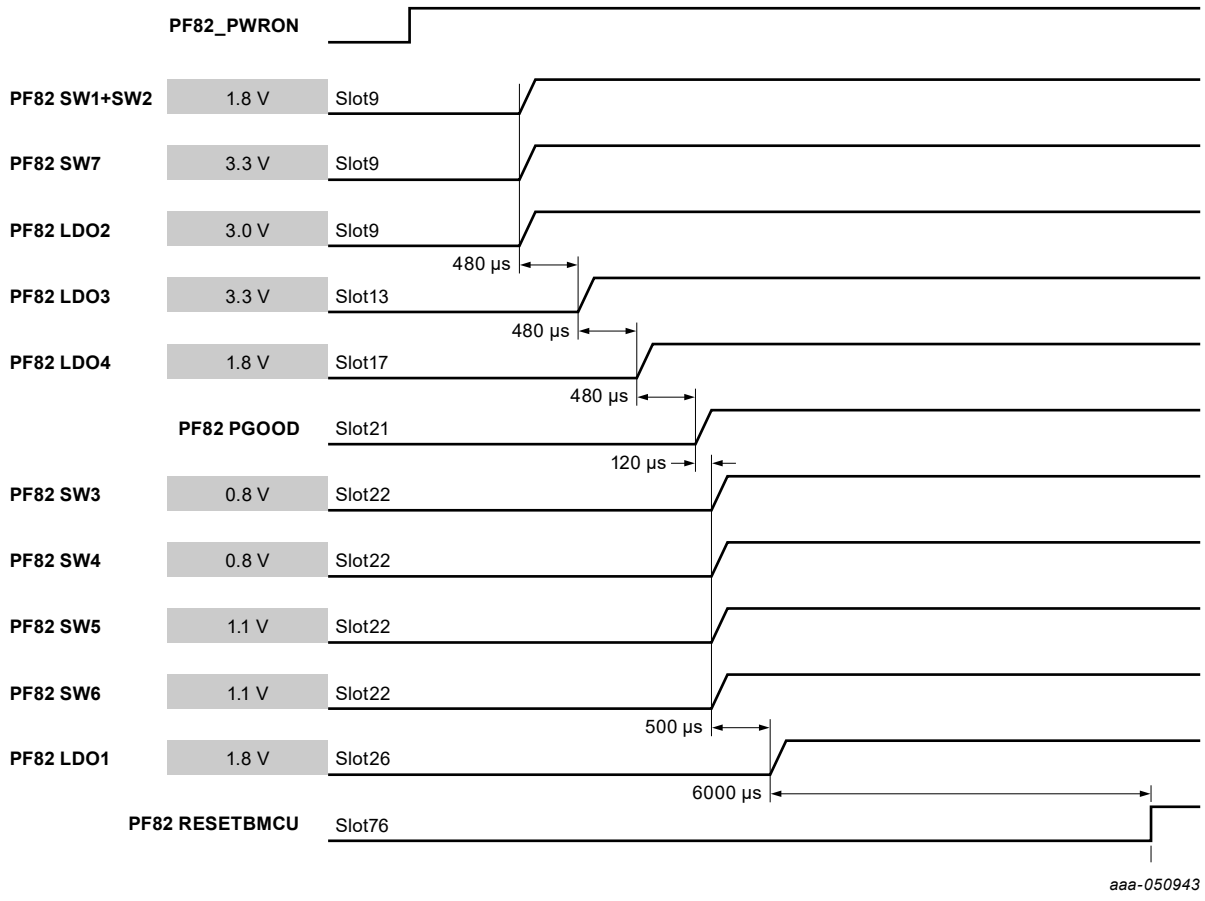

Figure 7. SC33PF8200KCES power up sequence for A1000L/A1000

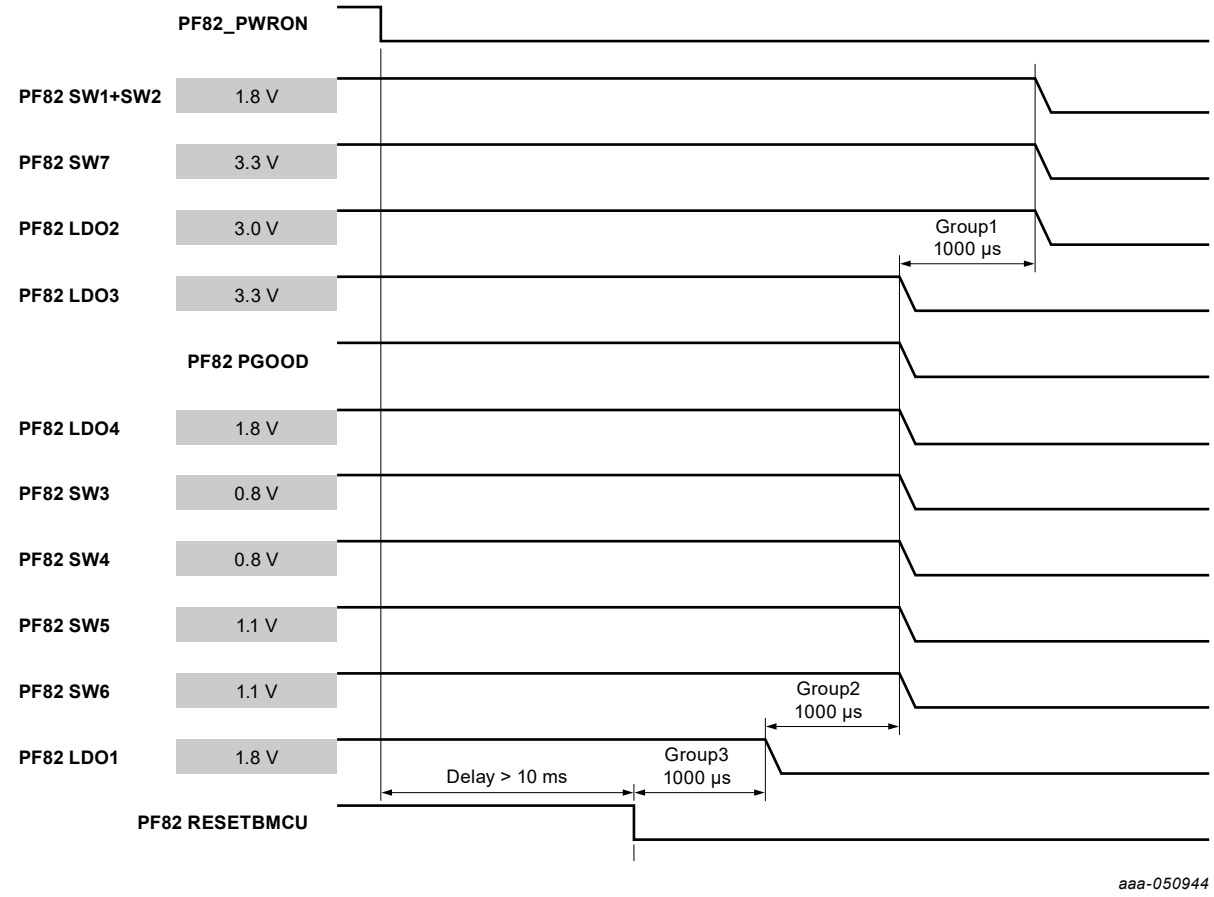

Figure 8. SC33PF8200KCES power down sequence for A1000L/A1000

6 Optional safety features

PF82 devices have embedded safety mechanisms. NXP PMICs meet ISO26262 standard and PF82 is up to the ASIL-B functional safety level. The safety mechanism includes the following functional safety features:

- **Independent voltage monitoring and fault detection:** PMICs feature independent fault monitoring function for each regulator. UV, OV, and ILIM are three types of faults monitored by the PMIC fault monitor block. These PMICs can indicate output state for each regulator through the PGOOD signal.
- **Watchdog monitoring and internal watchdog counter:** The PF81/82 features internal watchdog counters to monitor a watchdog event that happened from the processor. If the PMIC internal watchdog expiration counter reaches the maximum value, a reset event is performed by the PMIC. The watchdog can be disabled if not needed.
- **I^2C CRC and write protection:** The fuses are loaded into the functional I^2C registers of the PMIC. The fuse circuits have a CRC error check routine that reports and protects against register loading errors on the PMIC registers. If a register loading error is detected, the corresponding flag is asserted. The I^2C secure write is to protect the secure registers from a wrong operation.
- **Functional safety output:** When a fault is detected by the PMIC, such as an incorrect regulator output or WD failure, the PMIC can reset the A1000L/A1000 processor through the RESETBMCU pin. The PMIC can also trigger the FSOB pin to put the system into a safe state.
- **Fail-safe state:** This state works as a safety lock-down upon a critical device/system failure. If the fail-safe bypass is disabled, the device moves to the fail-safe state when the proper condition is met. The device can exit the fail-safe state only after a power cycle event is present.

- **Analog Built-In Self-Test (ABIST):** When the system power is turned on, the PMICs routinely implement an ABIST process of all output voltage monitors before starting the power-up sequence. ABIST checks the state of the voltage monitoring block (OV/UV) of each regulator, whether normal or not. If a failure on the OV/UV monitor is detected during the ABIST on demand request, the PMIC will assert the corresponding ABIST flags.

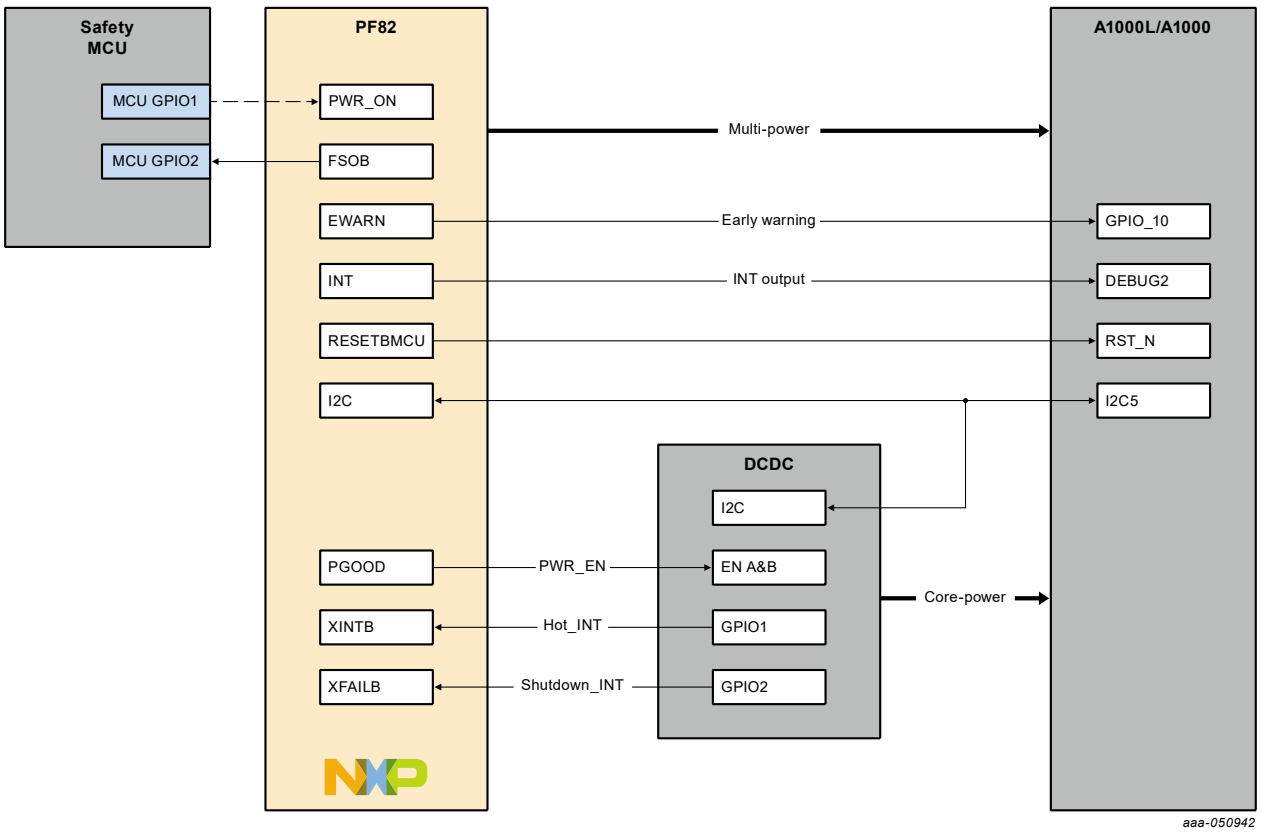

Figure 9. Functional signal connection between PF82 and Black Sesame A1000L/A1000

Figure 9 shows the recommended functional signal connections between the PF82 and Black Sesame A1000L/A1000 processor.

In this application, SC33PF8200KCES(R2) has enabled the I^2C CRC protection, Fail-safe state, FSOB output, and watchdog monitoring input. The watchdog timer and independent regulator OV/UV/OC fault monitoring features are disabled, but they can be configured by the functional register bits once the PMIC is on. If the application does not need these PMIC safety features, NXP also provides QM PMIC PF81, which is pin-to-pin compatible with the ASIL-B PMIC PF82. QM version PMICs are low-cost devices containing basic regulator OV/UV/OC fault monitoring features. Details about the functional differences between QM and ASIL-B devices can be found in the data sheet of PF81/82.

7 Schematic

Figure 10 shows an A1000L/A10000 power solution schematic based on SC33PF8200KCES.

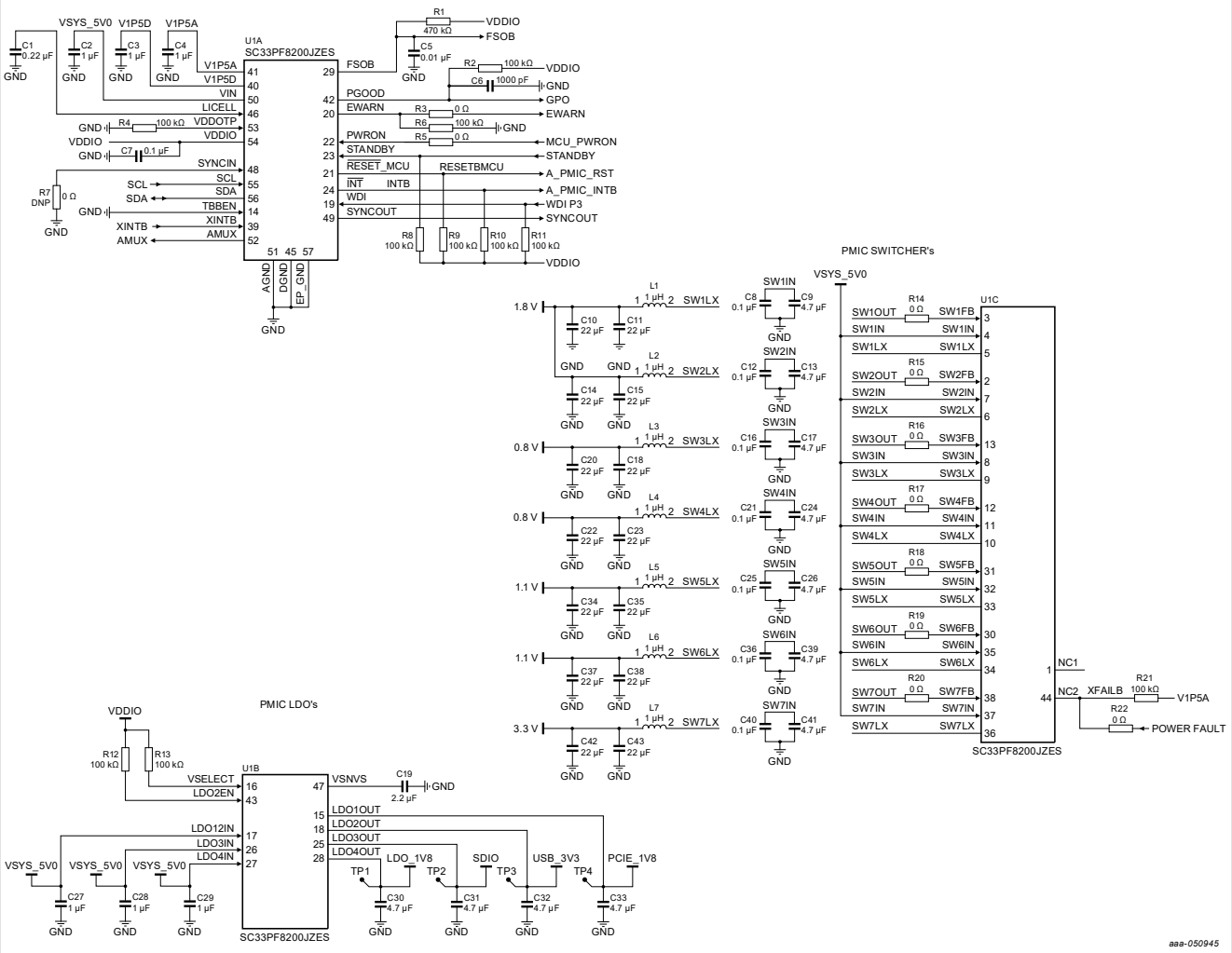

Figure 10. SC33PF8200KCES schematic for A1000L/A10000 power rails

8 Bill of materials

Table 3 is an SC33PF8200KCES bill of materials to support the Black Sesame A1000L/A10000 processor.

Table 3. The design parameters of PF8200 attach A1000L/A1000 solution

Value	Qty	Part number	Description	Vendor	Part Reference
0.22 µF	1	GRT155C81E224KE01	CAP CER 0.22 µF 25 V 10 % X6S AEC-Q200 0402	MURATA	C1
1 µF	6	GCM155C71A105KE38D	CAP CER 1 µF 10 V 10 % X7S AEC-Q200 0402	MURATA	C2, C3, C4, C27, C28, C29
0.01 µF	1	CGA3E2X7R1H103K080AA	CAP CER 0.01 µF 50 V 10 % X7R AEC-Q200 0603	TDK	C5
1000 pF	1	CGA3E2C0G1H102J080AA	CAP CER 1000 pF 50 V 5 % C0G AEC-Q200 0603	TDK	C6
0.1 µF	8	GCM155R71C104KA55D	CAP CER 0.1 µF 16 V 10 % X7R AEC-Q200 0402	MURATA	C7, C8, C12, C16, C21, C25, C36, C40
4.7 µF	11	GRT188C81E475KE13	CAP CER 4.7 µF 25 V 10 % X6S AEC-Q200 0603	MURATA	C9, C13, C17, C24, C26, C30, C31, C32, C33, C39, C41
22 µF	14	GRT21BC81A226ME13	CAP CER 22 µF 10 V 20 % X6S AEC-Q200 0805	MURATA	C10, C11, C14, C15, C18, C20, C22, C23, C34, C35, C37, C38, C42, C43
2.2 µF	1	GRT155C71A225KE13	CAP CER 2.2 µF 10 V 10 % X7S AEC-Q200 0402	MURATA	C19
1.0 µH	7	TFM252012ALMA1R0MTAA	IND PWR 1.0 µH@1 MHZ 4.7 A 20 % AEC-Q200 SMD	TDK	L1, L2, L3, L4, L5, L6, L7
470K	1	CR0603-FX-4703ELF	RES MF 470K 1/10 W 1 % 0603	BOURNS	R1
100K	10	CRCW0603100KJNEA	RES MF 100K 1/10 W 5 % AEC-Q200 0603	VISHAY	R2, R4, R6, R8, R9, R10, R11, R12, R13, R21
0	11	CRCW04020000Z0ED	RES MF ZERO Ω 1/16 W -- AEC-Q200 0402	VISHAY	R3, R5, R7, R14, R15, R16, R17, R18, R19, R20, R22
SC33PF8200 KCES	1	SC33PF8200KCES	IC POWER MANAGEMENT 2.7 to 5.5 V AEC-Q100 QFN56	NXP	U1

9 NXP BYLink system power platform for A1000L/A1000

BYLink is a simple and effective way to enable complex applications, such as ADAS and ADS. This new power supply concept simplifies the board design by:

- Providing power management building blocks and design flexibility
- Helping customers achieve a complete automotive system power solution

For more details about the BYLink System Power Platform, visit official website.

In car and truck systems, the 12 V and 24 V supplies from the battery are regulated and generated into multiple supply rails to satisfy the system power demands. NXP provides a complete portfolio of safety PMICs with embedded system features. These features are classified in two main categories:

- High voltage PMICs
- Low voltage PMICs

The PF8x00 power solutions for the A1000L/A1000 system that were mentioned earlier belong to the low voltage subset of BYLink PMICs.

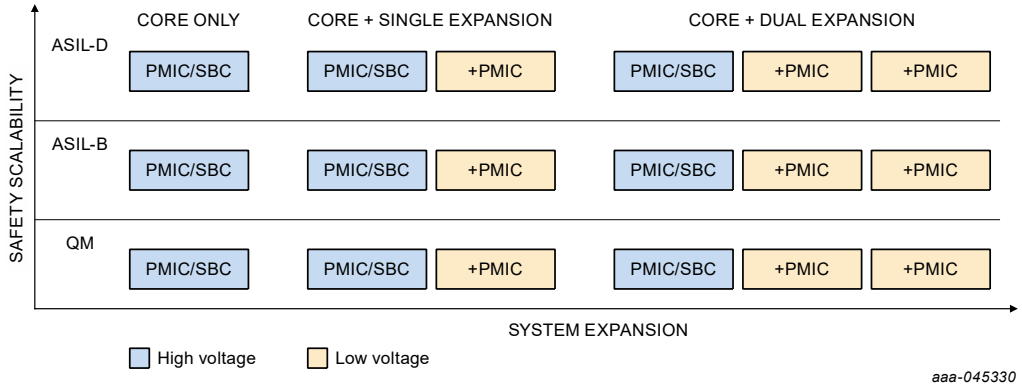

Figure 11. Safety scalability vs. system expansion

FS56 and FS86, each of which can be used to connect to a battery input as a high voltage PMIC, are suitable for using in an A1000L/A1000 system for 12 V or 24 V automotive applications. To implement the BYLink system power platform for A1000L/A1000, select an FS56 or FS86 as the front-end power device to generate voltage for low voltage PMICs.

The FS56 can provide input to DCDC and PF8x and power to other peripherals. This device's current capability at SW2 can be 15 A, with a 1.8 to 7.2 voltage range. SW1 can provide 1.8 to 8.0 V/3 A high efficiency power for an MCU and other peripherals. EN1 and EN2 of the FS56 can be connected to an ignition signal or a CAN Phy wakeup signal. Figure 12 illustrates one real use case for an A1000L/A1000 12 V system.

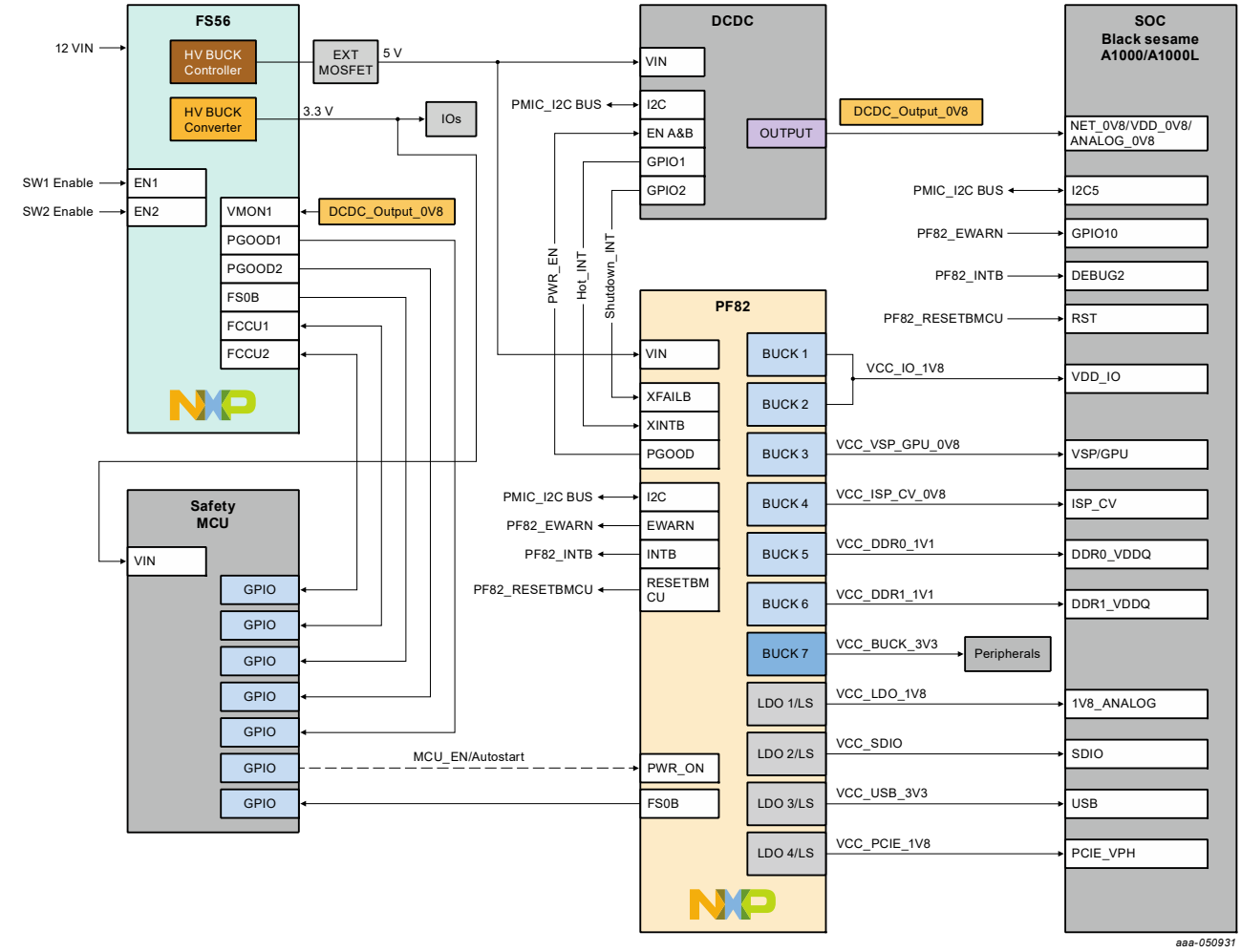

Figure 12. FS56+PF82 board solution for Black Sesame A1000L/A1000

For a 24 V and 12 V battery compatible system, FS86 family devices can be used to work with DCDC and PF8x. Also, because FS86 is suitable for ASIL-D and ASIL-B systems, it can be integrated closely with an ASIL-D MCU to achieve the ASIL-D target at the system level.

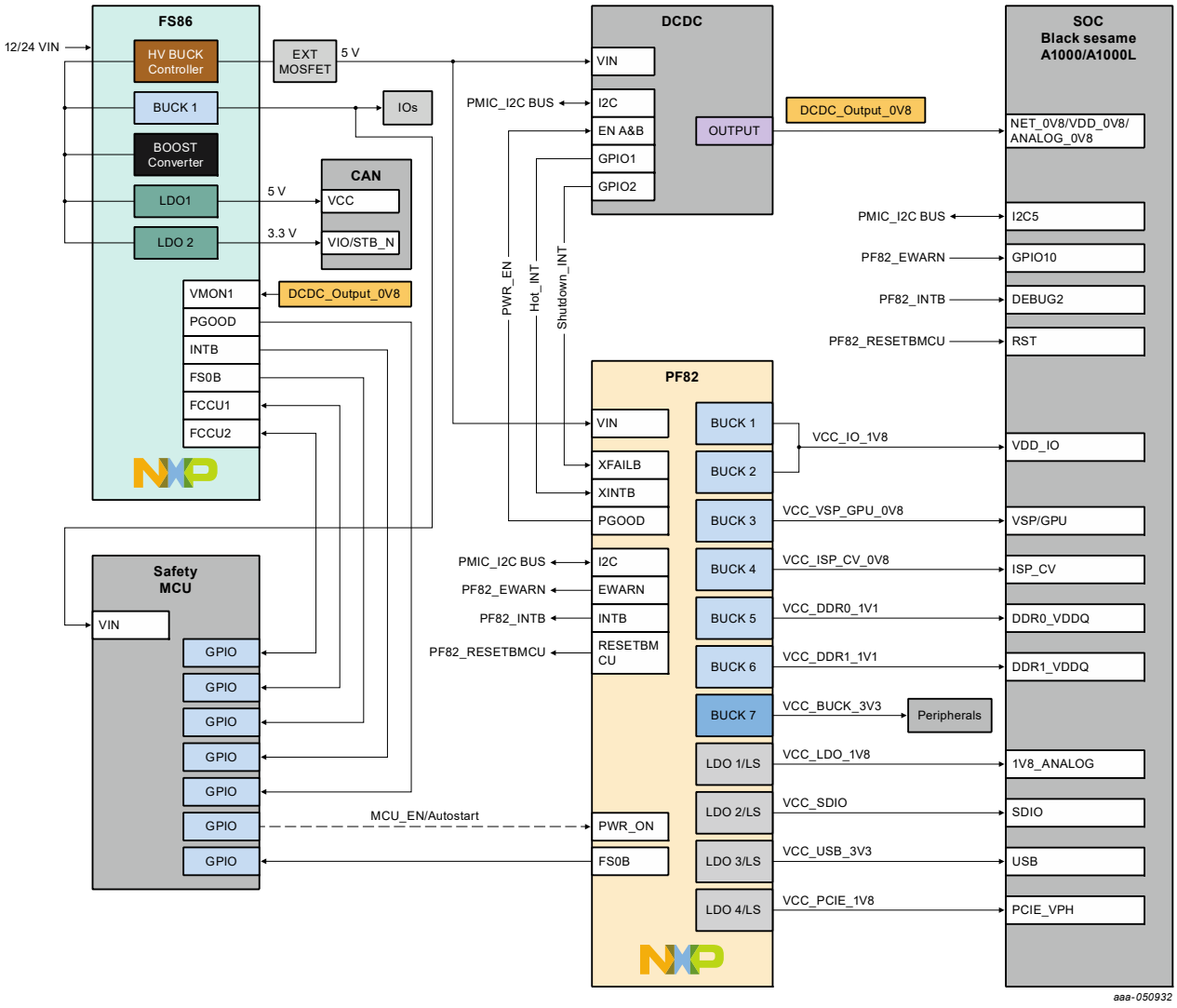

Figure 13. FS86+PF82 board solution for Black Sesame A1000L/A1000

When using an A1000L/A1000 SoC in a system, the HV-PMIC can be chosen to support the Safety MCU. High-voltage PMICs from NXP can work in synchronization with low-voltage PMICs to provide a total solution. Provide power requirements to NXP and we will help you with a customized power tree for a dedicated system.

10 References

[1] PF81/82 information and tools: https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/12-channel-power-management-integrated-circuit-pmic-for-high-performance-processing-applications:PF8100-PF8200

[2] FS5600 information and tools: https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/automotive-dual-buck-regulator-and-controller-with-voltage-monitors-and-watchdog-timer:FS5600

[3] FS86 information and tools: https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-for-domain-controller-fit-for-asil-b-and-d:FS86

Tables

Figures

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For more information, please visit: http://www.nxp.com

Date of release: 13 June 2023
Document identifier: AN13863