AN14022

i.MX 93 Migration Guide from i.MX 8M Nano

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Document Information

Information	Content
Keywords	i.MX 8M Nano, i.MX 93, Migration
Abstract	This application note introduces the i.MX 93 application processor by highlighting the differences from the i.MX 8M Nano processor.

1 Introduction

This application note introduces the i.MX 93 application processor by highlighting the differences from the i.MX 8M Nano processor. The differences cover architecture, hardware, and power. When considering how to migrate, hardware and software are both covered.

The audiences of this document are users who want to upgrade from i.MX 8M Nano to i.MX 93. This document helps them to port their project to the i.MX93 platform.

2 Definitions, acronyms, and abbreviations

Table 1. Acronyms and meanings

Acronyms	Meanings
ADC	Analog-to-Digital Converter
ASRC	Asynchronous Sample Rate Converter
ATF	Arm Trusted Firmware
BBSM	Battery Backed Secure Module
CAAM	Cryptographic Acceleration and Assurance Module
CCM	Clock Controller Module
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
CSU	Central Security Unit
DAP	Debug Access Port
DVFS	Dynamic Voltage and Frequency Scaling
ENET	Ethernet
FPU	Floating Point Unit
GPC	General Power Controller
GPIO	General-Purpose I/O
GPMI	General Purpose Media Interface
GPU	Graphics Processing Unit
HAB	High-Assurance Boot
I2C	Inter-Integrated Circuit
IOMUX	Input-Output Multiplexer
ISI	Image Sensing Interface
JTAG	Joint Test Action Group (a serial bus protocol used for test purposes)
LCDIF	Liquid Crystal Display Interface
LDO	Low Dropout Regulator
LP	Low Power
LVDS	Low Voltage Differential Signaling
MQS	Medium Quality Sound
NPU	Neural Processing Unit

Table 1. Acronyms and meanings...*continued*

Acronyms	Meanings
MU	Messaging Unit
OCOTP	On-Chip One-Time Programmable Controller
OSC	Oscillator
PDM	PDM Microphone Interface
PIT	Periodic Interrupt Timer
PLL	Phase-Locked Loops
PMIC	Power Management IC
ROM	Read Only Memory
POR	Power-On Reset
PWM	Pulse Width Modulation
PXP	Pixel Pipeline
RDC	Resource Domain Control
SAI	Synchronous Audio Interface
SDPIF	Sony Philips Digital Interface
SJC	System JTAG Controller
SPI	Serial Peripheral Interface
SRC	System Reset Controller
SNVS	Secure Non-Volatile Storage
TCM	Tightly Coupled Memory
TPM	Timer/PWM Module
TRDC	Trusted Resource Domain Control
TSTMR	Timestamp Timer
TZ	Trust Zone
WDOG	Watchdog
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
uSDHC	Ultra Secured Digital Host Controller
XCVR	Audio Transceiver

3 General comparison between i.MX 8M Nano and i.MX 93

This section describes the general SoC differences between i.MX 8M Nano and i.MX 93. Figure 1 and Figure 2 shows features of i.MX 8M Nano and i.MX 93 in the top level. For more detailed comparison, see the following subsections.

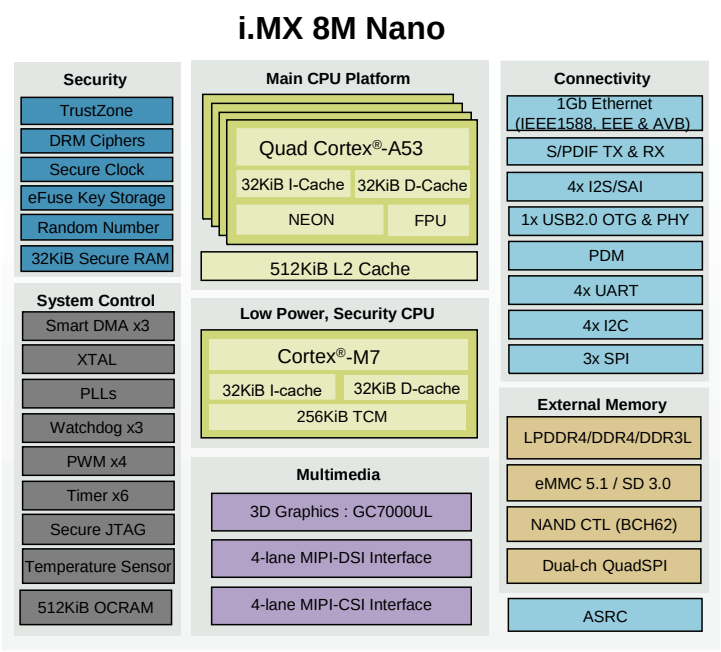

Figure 1. i.MX 8M Nano feature diagram

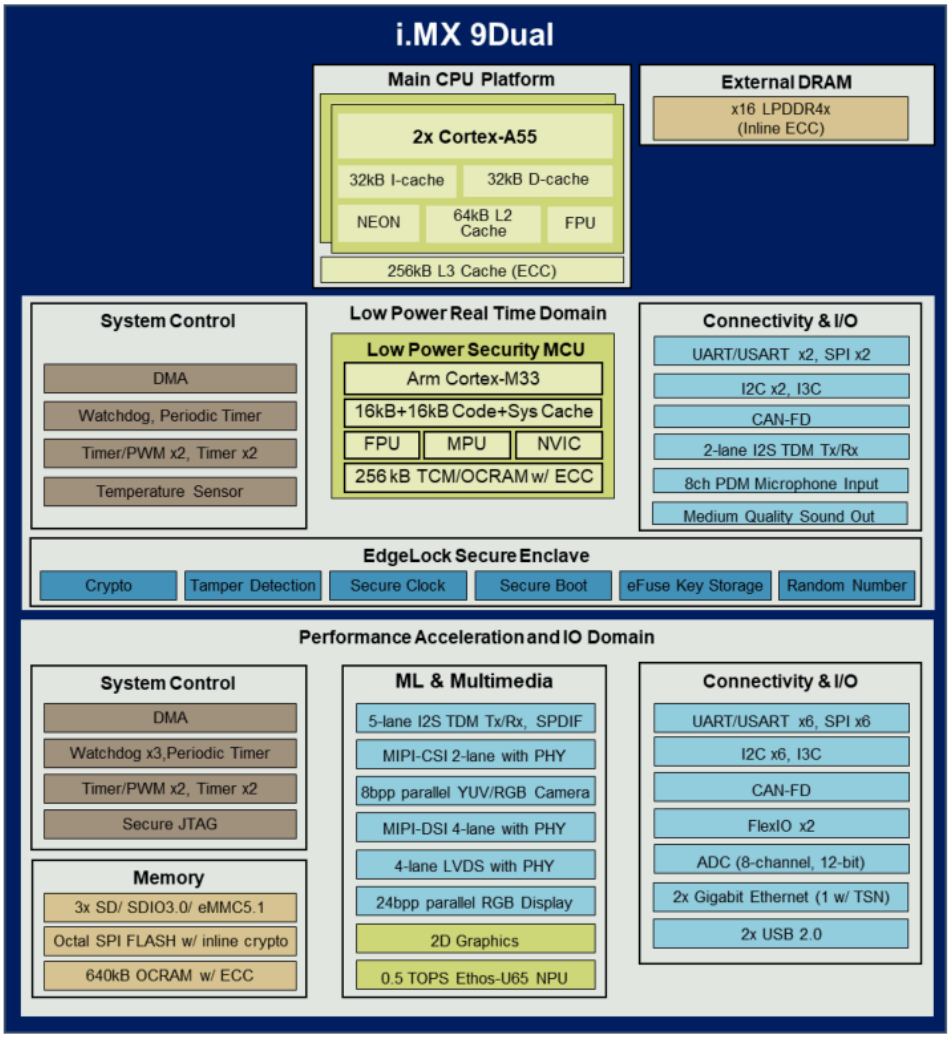

Figure 2. i.MX 93 feature diagram

3.1 Architecture differences

The architecture differences cover the CPU architecture and SoC architecture. For CPU architecture, it describes the resources and performance of CPU, including the core number, cache size, frequency, and so on.

Table 2. CPU architecture

Items		i.MX 8M Nano	i.MX 93
Cortex-A	Cores	A53 × 4	A55 × 2
	Cache	32 kB L1 Instruction Cache 32 kB L1 Data Cache 512 kB L2 Cache	32 kB L1 Instruction Cache 32 kB L1 Data Cache 64 kB L2 Cache 256 kB shared L3 Cache
	Frequency	1.5 GHz	1.7 GHz
	Others	NEON, FPU	NEON, FPU
Cortex-M	Cores	M7	M33

Table 2. CPU architecture*...continued*

Items		i.MX 8M Nano	i.MX 93
	Memory	256 kB TCM	16 kB System Cache 16 kB Code Cache 256 kB TCM
	Frequency	750 MHz	250 MHz

For SoC architecture, it describes the distribution of all modules in SoC MIXs. i.MX 8M Nano and i.MX 93 share only a few of the same MIXs. For SoC in the i.MX 8M Nano, most modules are located in SUPERMIX including M7. However, in i.MX 93, most modules locate in AONMIX and WAKEUPMIX. The two MIXs still share some same kind of modules. M33 is located in AONMIX.

Table 3. SoC Architecture

i.MX 8M Nano		i.MX 93	
CPU	A53	A55MIX	A55
SUPERMIX	M7, WDOG, UART, I2C, GPIO, PWM, Timer, Quad SPI, OCOTP, IOMUX, MU, RDC, CSU, ENET, uSDHC, GPMI, eCSPI, SPDIF, PDM, SAI, ASRC, CoreSight, DAP	AONMIX	M33, LPIT1, SAI1, MQS1, CAN-FD1, WDOG1..2, IOMUX, LPI2C1..2, LPSPI1..2, LPUART1..2, LPUART1..2, MU1, I3C1, PDM, LPTMR1, TPM1..2, TSTMR1, GPIO1
		WAKEUPMIX	uSDHC, ENET, ENET_QoS, PDM, GPIO2..4, FLEXIO1..2, MU2, WDOG3..5, FlexSPI1, TSTMR2, LPIT2, TPM3..6, LPTMR2, I3C2, LPUART3..8, LPSPI3..8, LPI2C3..8, CAN-FD2, SAI2..3, MQS2, XCVR
GPUMIX	GC7000UL	—	—
DISPLAYMIX	MIPI CSI, ISI, LCDIF, MIPI DSI	MEDIAMIX	MIPI CSI, ISI, PXP, LCDIF, MIPI DSI, LVDS
HSIOMIX	USB	HSIOMIX	USB
—	—	MLMIX	NPU
ANAMIX	XTAL OSC, PLLs, Temp Sensor	ANAMIX	ADC, XTAL OSC, PLLs, Temp Sensor
DDRMIX	DDR	DDRMIX	DDR
CCMSRC GPCMIX	GPC, SRC, CCM	CCMSRCGPCMIX	GPC, SRC, CCM, TCU_CCM
SNVSMIX		BBSMMIX	
NOC_WRAPPER		NICMIX	

3.2 Hardware differences

3.2.1 Clocking

i.MX 8M Nano shares most clock sources and PLLs as i.MX 93. However, i.MX 8M has extra clock sources (CCM_EXT_CLK[4:1]) and PLLs (SYSTEM PLL2, SYSTEM PLL3, M7 ALT PLL, GPU_PLL). The SYSTEM PLL1 dividers of the two SoCs are also different. The maximum frequencies of PLLs with the same name are a little different. The SYSTEM PLL of i.MX 8M Nano is integer PLL, while the SYSTEM PLL of i.MX 93 is fractional PLL.

Table 4. Clock sources and PLLs

i.MX 8M Nano		i.MX 93	
CCM_EXT_CLK[4:1]		—	
OSC 24 MHz		OSC 24 MHz	
OSC 32 kHz		OSC 32 kHz	
Arm PLL		Arm PLL	
SYSTEM PLL1	SYSTEM_PLL1_CLK	SYSTEM PLL	SYS_PLL_PFD0 SYS_PLL_PFD0_DIV2 SYS_PLL_PFD1 SYS_PLL_PFD1_DIV2 SYS_PLL_PFD2 SYS_PLL_PFD2_DIV2
	SYSTEM_PLL1_DVI2		
	SYSTEM_PLL1_DVI3		
	SYSTEM_PLL1_DVI4		
	SYSTEM_PLL1_DVI5		
	SYSTEM_PLL1_DVI6		
	SYSTEM_PLL1_DVI8		
	SYSTEM_PLL1_DVI10		
	SYSTEM_PLL1_DVI20		
SYSTEM PLL2	SYSTEM_PLL2_CLK	-	
	SYSTEM_PLL2_DVI2		
	SYSTEM_PLL2_DVI3		
	SYSTEM_PLL2_DVI4		
	SYSTEM_PLL2_DVI5		
	SYSTEM_PLL2_DVI6		
	SYSTEM_PLL2_DVI8		
	SYSTEM_PLL2_DVI10		
	SYSTEM_PLL2_DVI20		
SYSTEM PLL3		—	
AUDIO PLL1		AUDIO PLL	
AUDIO PLL 2		—	
DRAM PLL		DRAM PLL	
VIDEO PLL		VIDEO PLL	
M7 ALT PLL		—	
GPU_PLL		—	

Table 5. PLL output frequency of i.MX 8M Nano

PLL	Type	VCO frequency (MHz)	Post divider	Max.frequency	Use case
SYSTEM PLL1	integer	3200	4	800	Set to fixed frequency after boot by ROM code.
SYSTEM PLL2	integer	2000	2	1000	

Table 5. PLL output frequency of i.MX 8M Nano*...continued*

PLL	Type	VCO frequency (MHz)	Post divider	Max.frequency	Use case
SYSTEM PLL3	integer	1600~3200	2^s 0 ≤ s ≤ 6	1000	Fully configurable by software to support clock requirement for various IP modules.
Arm PLL	integer	1600~3200		2000	
GPU PLL	integer	1600~3200		1000	
VPU PLL	integer	1600~3200		800	
DRAM PLL	fractional	1600~3200		800	
Audio PLL1	fractional	1600~3200		650	
Audio PLL2	fractional	1600~3200		650	
Video PLL1	fractional	1600~3200		650	

Table 6. PLL output frequency of i.MX 93

PLL	Type	VCO frequency (MHz)	PFD/DFS MFI	PFD/DFS MFN	Max.frequen	Use case
SYSTEM PLL1	Fractional with PFD/DFS	4000	4	0	1000	Set to fixed frequency after boot by ROM code.
			5	0	800	
			6	2	625	
Arm PLL	integer	2500~5000	N/A	N/A	2000	Fully configurable by software to support clock requirement for various IP modules.
DRAM PLL	fractional	2500~5000			1000	
Audio PLL1	fractional	2500~5000			650	
Video PLL1	fractional	2500~5000			594	

3.2.2 Power management

The main difference is that i.MX 93 supports low-power run mode. In this mode, modules in AONMIX of i.MX 93 can run when other domains can be powered down. For more detailed information, see Section 4.2.4.

SNVS, IDLE, and suspend are referred as low-power mode for the chip. Suspend and Idle are the two typical low-power modes defined based on the use case of Linux kernel.

Table 7. Power Modes

i.MX 8M Nano	i.MX 93	
Run mode	Run mode	No change
	Low-power run mode	New: This mode is defined as a low-power run mode with all external power rails are ON. In this mode, all the unnecessary power domain (MIX) can be off, except AONMIX and the internal modules required, such as OSC24M/PLL. Cortex-M33 CPU in AONMIX handles all the computing and data processing. Cortex-A55 is powered down and DRAM can be in self-refresh/retention mode. All the modules in the AONMIX, such as, SAI/CAN/LPUART, can be used directly. To use modules in other power domains, such as, WAKEUPMIX, the user can turn on other peripherals and related power by Cortex-M33 as needed.

Table 7. Power Modes*...continued*

i.MX 8M Nano	i.MX 93	
Idle mode	Idle mode	Updated: • For the i.MX 8M Nano, L2 data is retained. • For i.MX 93, L3 data is retained.
Suspend mode	Suspend mode	No change
SNVS mode	BBSM mode	Updated: • Replace SNVS with BBSM
OFF mode	OFF mode	No change

For different power modes, the power rails are different as below.

Table 8. Power supply states of i.MX 8M Nano

Power rail	OFF	SNVS	Suspend	Idle	Run
VDD_ARM	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON
VDDA_1P8	OFF	OFF	ON	ON	ON
VDDA_0P8	OFF	OFF	ON	ON	ON
VDD_DRAM	OFF	OFF	ON	ON	ON
VDD_SNVS	OFF	ON	ON	ON	ON
NVCC_SNVS	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	ON	ON	ON
DRAM_VREF	OFF	OFF	OFF	ON	ON

Table 9. Power Supply States of i.MX 93

Power rail	OFF	BBSM	Low-power SUSPEND (1.8 V analog OFF)	Suspend (Analog ON)	Idle	Run/Low-pPower Run
NVCC_BBSM_1P8	OFF	ON	ON	ON	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON	ON
VDD2_DDR VDDQ_DDR	OFF	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON	ON
VDD_ANAx_0P8 VDD_MIPI_0P8 VDD_USB_0P8	OFF	OFF	ON	ON	ON	ON
VDD_ANAx_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_USB_1P8 VDD_USB_3P3	OFF	OFF	OFF	ON	ON	ON

3.2.3 Reset and boot

As shown in Table 10, i.MX 93 has richer and more accurate reset sources than i.MX 8M Nano.

Table 10. Reset sources

i.MX 8M Nano	i.MX 93
POR	POR
CSU reset	CSU reset
SRC_ONOFF	SRC_ONOFF
WDOG reset	WDOG1 M33 reset WDOG2 M33 reset WDOG3 wake-up mix reset WDOG4 A55 reset WDOG5 A55 reset
—	Temper sensor reset
—	M33 lockup reset
—	M33 system reset
SJC software reset	JTAG software reset
SJC_TRST_B	—

i.MX 93 supports single boot and low-power boot with two boot ROMs. In single boot, the Cortex-A55 ROM loads all containers and images, and then jumps to the A55 firmware. In low-power boot, only the Cortex-M33 ROM is running after Power-On Reset.

i.MX 8M Nano only supports boot from A53 with only one boot ROM. Table 11 shows the supported boot modes.

Table 11. Boot modes

i.MX 8M Nano	i.MX 93 (Single boot with A55 ROM)	i.MX 93 (Low-power boot with M33 ROM)
From internal fuses	From internal fuses	From internal fuses
Serial download	Serial download	Serial download
uSDHC (eMMC)	uSDHC (eMMC)	uSDHC (eMMC)
uSDHC (SD)	uSDHC (SD)	uSDHC (SD)
FlexSPI 3B read	FlexSPI serial NOR	FlexSPI serial NOR
FlexSPI HyperFlash 3.3 V		
FlexSPI serial NAND 2K	FlexSPI serial NAND 2K	FlexSPI serial NAND 2K
FlexSPI serial NAND 4K	—	—
eCSPI boot	—	—

3.2.4 Security

Compared to i.MX 8M nano processors, i.MX93 processors enhanced the security in the following parts.

i.MX93 introduces EdgeLock Enclave (ELE), which i.MX 8M nano does not have. It is an independent security domain that provides security services, which include key management and execution of cryptographic services. The ELE provides a secure environment, which enables applications to execute secure cryptographic services.

Advanced High Assurance Boot (AHAB) is used in i.MX 93. It replaces the High Assurance Boot (HAB) which is used in the i.MX 8M nano. AHAB is responsible for authenticating the ELE firmware, which supplies the services for authenticating boot images of the application core signed by the user.

Trusted Resource Domain Controller (TRDC) replace the Resource Domain Controller (RDC) and Central Security Unit (CSU) which is used in i.MX 8M nano. It is responsible for the memory/peripheral resource sharing and isolation between the Cortex-A55 platform, Cortex-M33 core, and other bus masters. For more information, see Section 4.2.3.

i.MX 93 extends the secure debug features. It still supports the password-based authentication, and introduced a new asymmetric authentication function.

i.MX 93 supports tamper detection features, which i.MX 8M Nano does not support.

There are still some other differences in the security aspect, as described in Table 12.

Table 12. Security modules

Item	i.MX 8M Nano	i.MX 93
RDC	RDC	TRDC
TrustZone	TrustZone support Trustzone-A	TrustZone support both Trustzone-A and Trustzone-M
OCRAM secure region	OCRAM secure region	Removed: There are 32 kB of `OCRAM_s` in i.MX 8M Nano and it is controlled by `IOMUXC_GPR_GPR11` and `CSU_CSL_59`, while there are no `OCRAM_s` in i.MX 93. But there are 640 kB of OCRAM in i.MX 93 and it is managed by `TRDC_N`.
HAB	HAB	AHAB
CAAM	CAAM	ELE HSM
SNVS/BBSM	SNVS	BBSM/BBNSM. Updated with tamper functions
Debug	Password based secure debug	Password and asymmetric authentication

3.2.5 Other module differences

The section describes the modules resources changes. It shows the changes of IP updates and instance numbers. It covers memory, multimedia, connectivity, timer, and system debug.

Table 13. Other modules

	i.MX 8M Nano	i.MX 93
NPU	N/A	NPU × 1
MU	MU × 1	MU × 2
OCRAM	544 kB	640 kB
DDRC	DDRC × 1 Support DDR4/DDR3L/LPDDR4	DDRC × 1 Support LPDDR4/LPDDR4x
SPI	ECSPI × 3	LPSPI × 8
GPMI/NAND	GPMI/NAND	N/A
uSDHC	uSDHC × 3	uSDHC × 3
FlexSPI	FlexSPI × 1	FlexSPI × 1
ISI	ISI × 1	ISI × 1
GPU/PXP	GPU	PXP

Table 13. Other modules*...continued*

	i.MX 8M Nano	i.MX 93
LCDIF	eLCDIF × 1	LCDIF × 1 i.MX 93 also support parallel display
MIPI CSI	MIPI CSI × 1	MIPI CSI-2 × 1 Different IP
MIPI DSI	MIPI DSI × 1	MIPI DSI × 1 Different IP
LVDS	N/A	LVDS Display × 1
CSI	N/A	Parallel Camera × 1
SAI	SAI × 5	SAI × 3 Fewer instances and different supported lanes
SPDIF	SPDIF × 1	SPDIF XCVR × 1 Different IP
PDM	PDM × 1	PDM × 1
ASRC	ASRC	N/A
MQS	N/A	MQS × 1
GPIO	GPIO × 5	GPIO × 4 Different IP
USB	USB 2.0 × 1	USB 2.0 × 2
FlexCAN	N/A	FlexCAN × 2
I3C	N/A	I3C × 2
FlexIO	N/A	FlexIO × 2
Ethernet	Ethernet × 1	Ethernet × 1 Ethernet_QoS × 1
I2C	I2C × 4	LPI2C × 8
UART	UART × 4	LPUART × 8
LPTMR	N/A	LPTMR × 2
LPIT	N/A	LPIT × 2
TPM	N/A	TPM × 6
TSTMR	N/A	TSTMR × 2
GPT	GPT × 6	N/A
PWM	PWM × 4	N/A
WDO	WDOG × 3	WDOG × 5
TMU	TMU × 1	TMU × 1
ADC	N/A	SAR_ADC × 1

3.3 Power difference

3.3.1 Power architecture

There are a few differences of power architecture between i.MX 8M Nano and i.MX 93. The main difference is that i.MX 93 removes the VDD_ARM and the cores are supplied with VDD_SOC. For other differences, see Table 14.

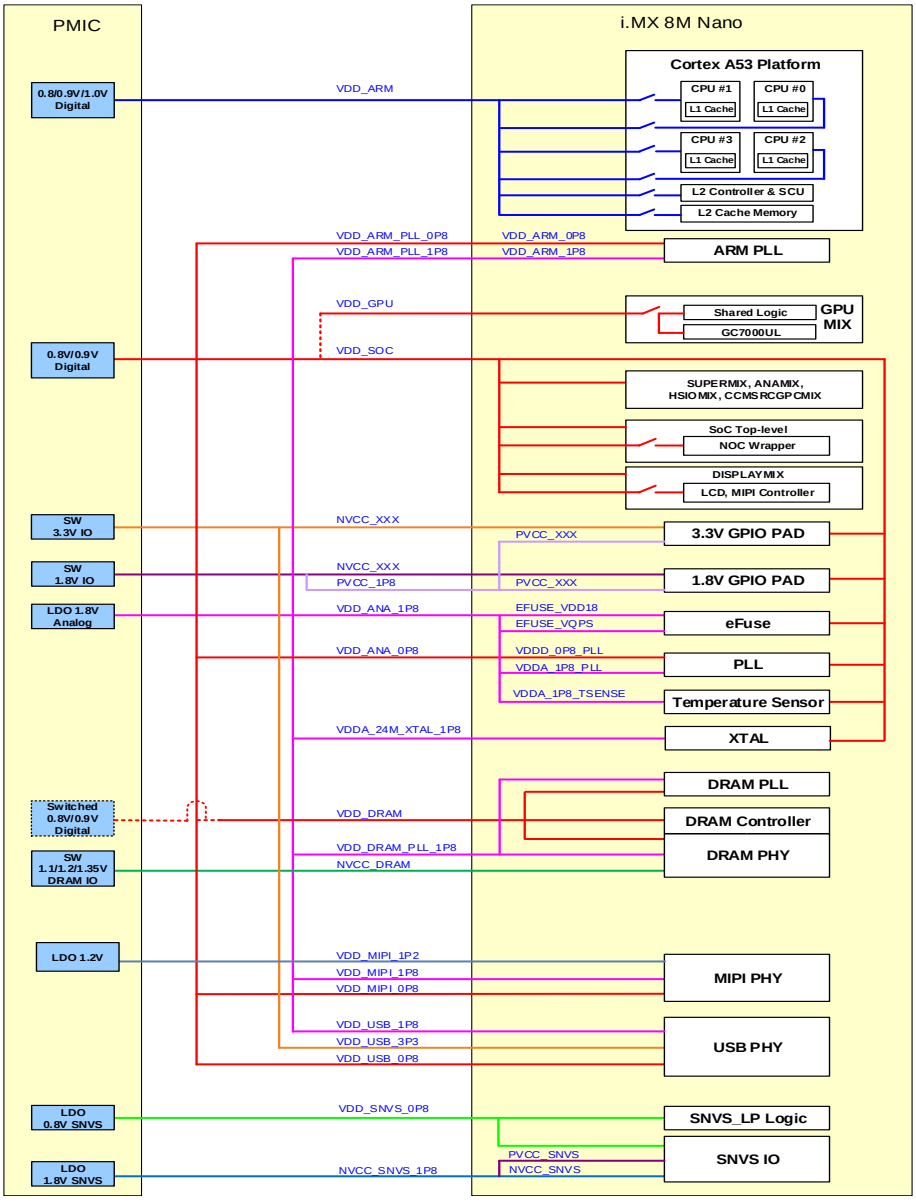

Figure 3. Power architecture of i.MX 8M Nano

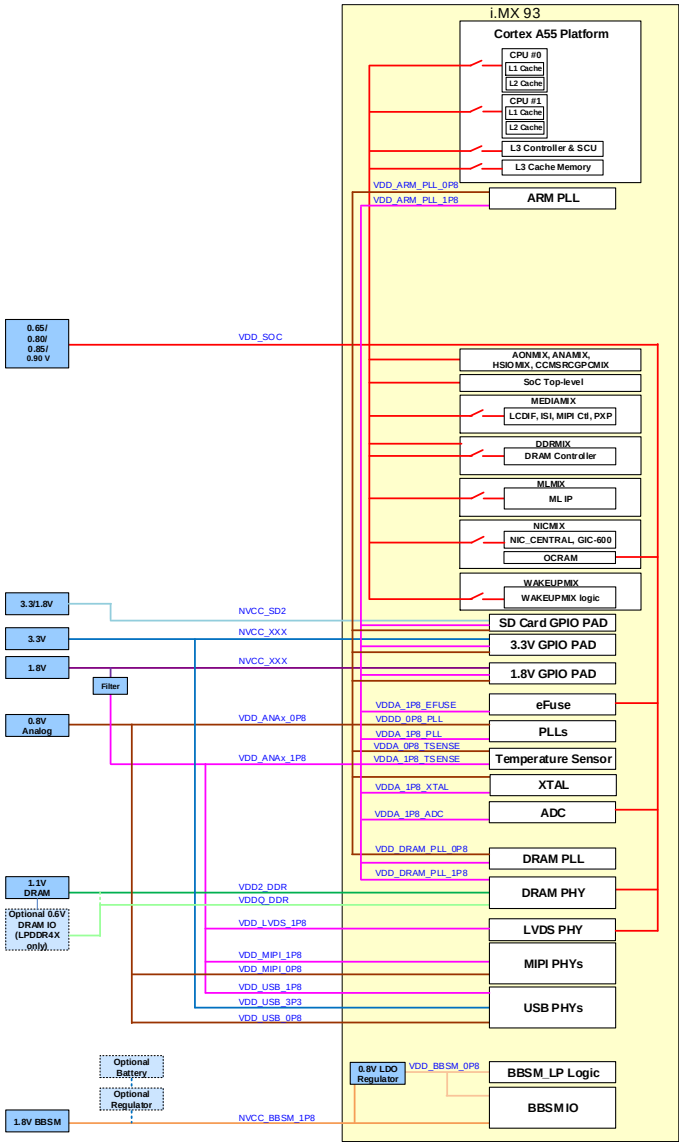

Figure 4. Power architecture of i.MX 93

Table 14. Power architecture differences

Item	i.MX 8M Nano	i.MX 93
VDD_ARM/VDD_SOC	The digital logic inside the chip is supplied with two supplies: VDD_ARM and VDD_SOC. The VDD_SOC can be nominal or overdrive voltage.	The digital logic inside the chip is supplied with only one supply: VDD_SOC. The VDD_SOC can be nominal or overdrive or a low drive voltage.
DRAM controller and PHY	The DRAM controller and PHY have three external power supplies: • VDD_SOC supplies controller and PHY digital logic • VDDA_DRAM for PHY analog circuit • NVCC_DRAM for IO	• VDD_ANAx_0P8/VDD_DDR_PLL_0P8 for PLL and PHY digital logic • VDD_ANAx_1P8/VDD_DDR_PLL_1P8 for DRAM PLL and PHY analog circuitry • VDD2_DDR for 1.1V DRAM PHY supply • VDDQ_DDR for DRAM PHY IO supply (1.1V for LPDDR4 and 0.6V for LPDDR4X)

Table 14. Power architecture differences*...continued*

Item	i.MX 8M Nano	i.MX 93
SNVS/BBSM	The 0.8 V core logic supply, 1.8 V IO pre-driver supply, and 1.8 V IO pad supply are supplied externally. If the PMIC does not have 0.8 V output, external LDOs can be used to generate the 0.8 V supply from 1.8 V. The SVNS core logic can also be 0.9 V to support the existing PMIC.	The 1.8 V IO pre-driver supply and 1.8 V IO pad supply are supplied externally. The `BBSM_LP` core digital domain logic is supplied by an internal LDO.

3.3.2 Power optimization

The overall system power consumption depends on the software optimization and the system hardware implementation. The following list of suggestions can help reduce system power consumption. i.MX 8M Nano and i.MX 93 shared power optimization plans.

Table 15. Power optimization

Optimization strategy	i.MX 8M Nano	i.MX 93
Run fast and idle	Y	Y
Clock gating	Y	Y
PLL number reduction	Y	Y
Core DVFS and system bus scaling	DVFS	VFS, not dynamic because core and SoC share same power rail `VDD_SOC`
Lower DDR frequencies	Y	Y
DDR interface optimization	Y	Y
Power gating of PHYs	Y	Y
Distribution of workloads	Y	Y
Use OCRAM to minimize DDR accesses	Y	Y
Thermal management to reduce leakage	Y	Y
Nominal or low drive mode	Y	Y

4 How to migrate

4.1 Hardware

4.1.1 Board changes

The layers of the boards and the power up sequences are different.

Table 16. PCB Layers comparison of different packages

Item	i.MX 8M Nano		i.MX 93		
Packages	FCBGA 14 × 14 mm, 0.5 mm pitch	FCBGA 11 × 11 mm, 0.5 mm pitch	FCBGA 14 × 14 mm, 0.65 mm pitch	FCBGA 11 × 11 mm, 0.5 mm pitch	FCBGA 9 × 9 mm, 0.5 mm pitch
Minimum Layers	6	6	6	6	4

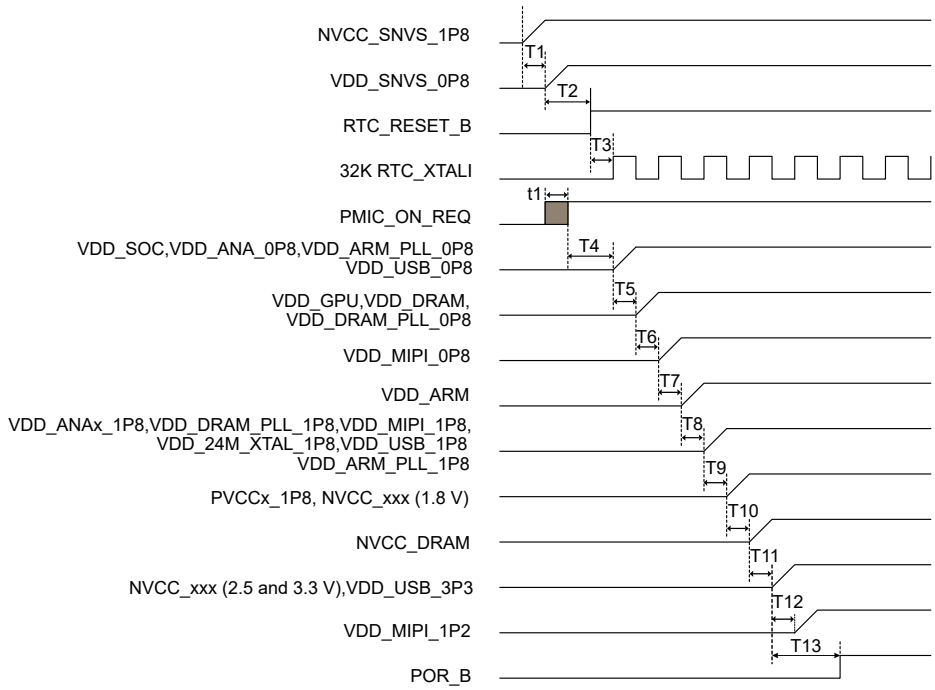

Figure 5. Power-up sequence for i.MX 8M Nano 14 × 14 mm package

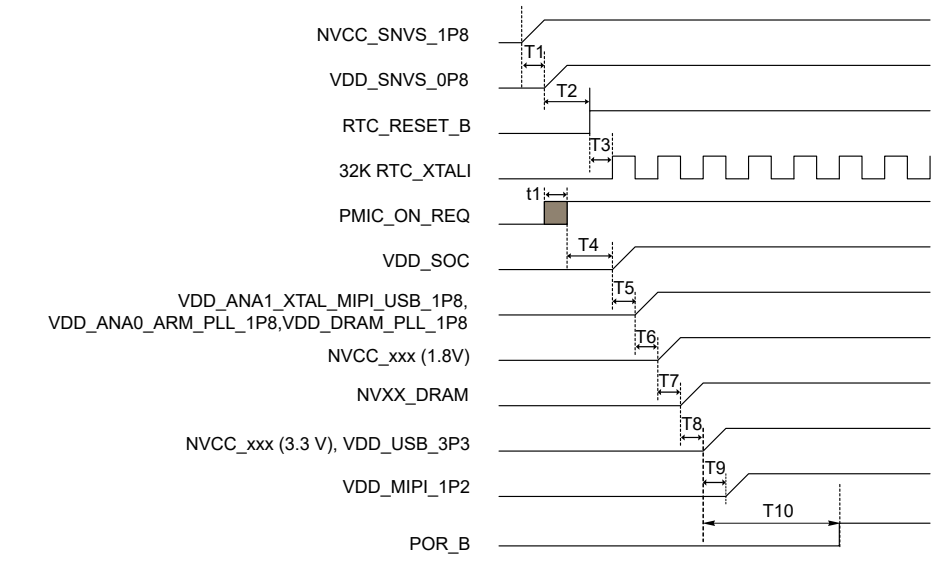

Figure 6. Power-up sequence for i.MX 8M Nano 11 × 11 mm package

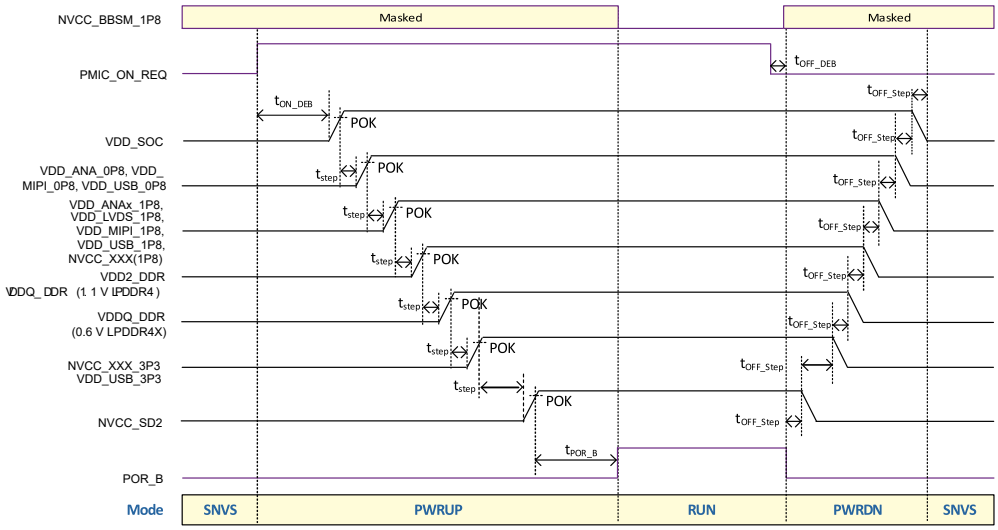

Figure 7. Power-up sequence for i.MX 93

Table 17. Maximum current design requirement

i.MX 8M Nano		i.MX 93	
Supply input	Max. current (mA)	Supply input	Max. current (mA)
VDD_ARM	2200	VDD_SOC	1500
VDD_SOC, DRAM and GPU	2000	VDD2_DDR	500
NVCC_DRAM	1000	VDDQ_DDR	260

4.1.2 Board design considerations

i.MX 8M Nano and i.MX 93 contain different SoCs with different boards. For more details, see the Reference chapter in the hardware design guide of specific SoC.

4.2 Software

4.2.1 U-Boot and kernel changes

From the view point of application, there are no special differences between i.MX 8M Nano and i.MX 93 in U-Boot and kernel. The references of the power domain in `dts` are also similar.

Table 18. U-Boot changes

Item	i.MX 8M Nano	i.MX 93
`config`	`imx8mn*defconfig`	`imx93*defconfig`
`dtb`	`imx8mn*.dts`	`imx93*.dts`

`Build` command	For `imx8mn_evk_defconfig`, the default value is `imx8mn_evk.dtb`.
	`make imx8mn_evk_defconfig`
	`make`
		For `imx93_11x11_evk_defconfig`, the default value is `imx93-11x11-evk.dtb`.
		`make imx93_11x11_evk_defconfig`
		`make`

Table 19. Kernel changes

Item	i.MX 8M Nano	i.MX 93
config	imx_v8_defconfig	imx_v8_defconfig
dtb	imx8mn*.dts imx8mn-evk.dts imx8mn-ddr3l-evk.dts imx8mn-ddr4-evk.dts	imx93*.dts imx93-11x11-evk.dts imx93-9x9-qsb.dts imx93-14x14-evk.dts .....
Build command	make imx_v8_defconfig make	make imx_v8_defconfig make

Table 20. Power domain changes in kernel dts

i.MX 8M Nano	i.MX 93
pgc_hsiomix	—
pgc_otg1	—
pgc_gpumix	—
pgc_dispmix -> disp_blk_ctrl	mediamix -> media_blk_ctrl
pgc_mipi	—
—	mlmix

4.2.2 SDK changes

Table 21. SDK changes

i.MX 8M Nano	i.MX 93	
BOARD_InitMemory()		For i.MX 8M Nano, M7 has its local cache and is enabled by default. Set smart subsystems (0x28000000 ~ 0x3FFFFFFF) noncacheable before accessing this address region. No requirements for i.MX 93.
BOARD_RdcInit()		For i.MX 8M Nano, move the M7 core to specific RDC domain 1, then enable the clock gate of the IP/BUS/ PLL in domain 1 in the CCM. In this way, the clock of the peripherals used by M core is not affected by A core which is running at domain 0. No requirements for i.MX 93 SDK. Most of RDC configurations are done in Arm trusted firmware.
BOARD_InitBootPins()	BOARD_InitBootPins()	Common operation
BOARD_BootClockRUN()	BOARD_BootClockRUN()	Clocks are already configured by ROM or U-Boot. For i.MX 8M Nano, enable some other root clocks.
BOARD_InitDebug Console()	BOARD_InitDebug Console()	Common operation

4.2.3 RDC changes

In i.MX 8M Nano, the name of the resource domain management module is RDC. Some simple configurations are done in ATF. Sometimes, extra configurations are required in BOARD_RdcInit () of SDK.

In i.MX 93, the name of the resource domain management module is TRDC. ELE assigns different maters to a specific domain and no extra configurations are required in common cases.

Table 22. RDC vs TRDC

<table>
<tr><th></th><th>i.MX 8M Nano</th><th>i.MX 93</th></tr>
<tr><td>hardware</td><td>This device has only one RDC module. It manages all the connected modules. The RDC supports up to four domains.</td><td>This device has six instances of the TRDC module in different MIX:
• TRDC AONMIX
• TRDC WAKEUPMIX
• TRDC MEGAMIX
• TRDC NICMIX
• TRDC MEDIAMIX
• TRDC HSIOMIX
Each TRDC supports up to 16 domains.</td></tr>
<tr><td>software</td><td>ATF: imx8mn_bl31_setup.c
<pre>static const struct imx_rdc_cfg rdc[] = {
 /* Master domain assignment */
 RDC_MDAn(RDC_MDA_M7, DID1),

 /* peripherals domain permission */
 RDC_PDAPn(RDC_PDAP_UART4, D1R | D1W),
 RDC_PDAPn(RDC_PDAP_UART2, D0R | D0W),
 RDC_PDAPn(RDC_PDAP_RDC, D0R | D0W | D1R),

 /* memory region */
 RDC_MEM_REGIONn(16, 0x0, 0x0, 0xff),
 RDC_MEM_REGIONn(17, 0x0, 0x0, 0xff),
 RDC_MEM_REGIONn(18, 0x0, 0x0, 0xff),

 /* Sentinel */
 {0},
};</pre>SDK: board.c
BOARD_RdcInit ()</td><td>ATF: trdc.c
trdc_config.h
Below is the default domain ID of different masters.
<table><tr><th>Master</th><th>DEFAULT_DID</th></tr><tr><td>MTR_MSTR</td><td>1</td></tr><tr><td>M33</td><td>2</td></tr><tr><td>A55</td><td>3</td></tr><tr><td>Reserved</td><td>4</td></tr><tr><td>uSDHC1</td><td>5</td></tr><tr><td>uSDHC2</td><td>6</td></tr><tr><td>eDMA1/eDMA2</td><td>7</td></tr><tr><td>CoreSight ETR/ TESTPORT</td><td>8</td></tr><tr><td>DAP AHB_AP_SYS</td><td>9</td></tr><tr><td>uSDHC3
ENET
ENET QOS
NPU
USB 2
ISI
PXP
LCDIF</td><td>10</td></tr><tr><td>USB 1</td><td>11</td></tr></table></td></tr>
</table>

4.2.4 M core running when A core suspended

Both i.MX 8M Nano and i.MX 93 can make M core run when A cores enter suspend mode. But the required operations are slightly different to enable the feature.

For i.MX 8M Nano, if the Linux OS kernel runs together with M7, make sure that the correct *dtb* file is used. This *dtb* file reserves resources used by M7 and avoids the Linux kernel from configuring them. For both i.MX 8M

Nano and i.MX 93, if DDR memory is not required, add *clk-imx93.mcore_booted* to *bootargs(mmcargs)* through `uboot` command as below.

Table 23. How to make sure root clocks not gated

	i.MX 8M Nano	i.MX 93

Change `dtb`	• For the DDR4 board:
	`setenv fdtfile fsl-imx8mn-ddr4-evk-rpmsg.dtb`
	• For the LPDDR4 board:
	`setenv fdtfile fsl-imx8mn-evk-rpmsg.dtb`
		No requirements.

Set `mcore_booted`	`setenv mmcargs $mmcargs clk-imx8mn.mcore_booted`	`setenv mmcargs $mmcargs clk-imx93.mcore_booted`

If DDR memory is required in the M core application, below codes are necessary. ATF would read the value of `ServiceFlagAddr` to decide whether to disable all PLLs or not.

Table 24. Request ATF to let DDR active when A53 is suspended in i.MX 8M Nano

ATF

```
#define M4_LPA_ACTIVE 0x5555
#define DSP_LPA_ACTIVE 0xD
#define DSP_LPA_DRAM_ACTIVE 0x1D
#define M4_LPA_IDLE 0x0
bool imx_m4_lpa_active(void)
{
      uint32_t lpa_status;
      lpa_status = mmio_read_32(IMX_SRC_BASE + LPA_STATUS);
      return (lpa_status == M4_LPA_ACTIVE ||
          lpa_status == DSP_LPA_ACTIVE ||
          lpa_status == DSP_LPA_DRAM_ACTIVE);
}
```

The M core application

```
#define ServiceFlagAddr SRC- >GPR9
#define ServiceBusy (0xDU)
#define ServiceIdle (0x0U)

ServiceFlagAddr = ServiceBusy;
```

For i.MX 93, it is similar as i.MX 8M Nano to request ATF to let DDR active when A55 is suspended. ATF would read the value of `M33_ACTIVE_FLAG` to decide whether to disable all PLLs or not.

Table 25. Request ATF to let DDR active when A55 is suspended in i.MX93

ATF

```
#define M33_ACTIVE_FLAG         (IMX_SRC_BASE + 0x54)
#define M33_ACTIVE              U(0x5555)
/*
 * M33 side need to raise this flag it DDR is used when
 * A55 side enter low power mode.
 */
static inline bool is_m33_active(void)
{
    return mmio_read_32(M33_ACTIVE_FLAG) == M33_ACTIVE;
```

Table 25. Request ATF to let DDR active when A55 is suspended in i.MX93*...continued*

	`}`

The M core application	`#define IMX_SRC_BASE 0x44460000`
	`#define M33_ACTIVE_FLAG (IMX_SRC_BASE + 0x54)`
	`#define M33_ACTIVE (0x5555)`
	`#define M33_DisACTIVE (0x0)`
	
	`/* Request ATF to let DDR active when Cortex-A is suspended */`
	`*((uint32_t *)M33_ACTIVE_FLAG) = M33_ACTIVE;`

4.2.5 Enable DVFS or VFS

i.MX 8M Nano can support dynamic VFS because `VDD_SOC` and `VDD_ARM` are supplied separated. i.MX 93 can only support NOT dynamic VFS. The setup flows are different, as shown in Table 26 and Table 27. The section only covers the method in kernel.

Table 26. How to enable or disable VFS in i.MX 8M Nano

Target	i.MX 8M Nano
Enable DVFS	`cpufreq-set -g powersave`
Disable DVFS	`cpufreq-set -g performance`

Unlike i.MX 8M family, there is no separate VDD_ARM power rail for Cortex-A platform. A single VDD_SOC power rail is used for the whole digital logic in the SoC. The VDD_SOC can be nominal (ND) or overdrive (OD) or a Low Drive (LD) voltage. For LD mode, use imx93-11x11-evk-ld.dtb.

Table 27. How to enable or disable VFS in i.MX 93

Target	i.MX 93
Nominal drive mode, `ddr` to half speed	*echo 1 > /sys/devices/platform/imx93-lpm/mode*
Overdrive mode, `ddr` to full speed	*echo 0 > /sys/devices/platform/imx93-lpm/mode*
Low drive mode, `ddr` to half speed	*imx93-11x11-evk-ld.dtb* *echo 2 > /sys/devices/platform/imx93-lpm/mode*
Low drive mode with SWFFC, `ddr` to lowest speed	*imx93-11x11-evk-ld.dtb* *echo 3 > /sys/devices/platform/imx93-lpm/mode*

5 Reference

- *i.MX 8M Nano Applications Processor Datasheet for Consumer Products* (document IMX8MNCEC)
- *i.MX 8M Nano Applications Processor Reference Manual* (document IMX8MNRM)
- *i.MX 8M Nano Hardware Developer's Guide* (document IMX8MNHDG)
- *i.MX 8M Nano Power Consumption Measurement* (document AN12778)
- *i.MX 8M Low Power Design By M Core Running In System Suspend* (document AN13400)
- *i.MX 93 Consumer Application Processors Data Sheet* (document IMX93CEC)
- *i.MX 93 Applications Processor Reference Manual* (document IMX93RM)
- *i.MX 93 Hardware Design Guide* (document IMX93HDG)
- *i.MX 93 Power Consumption Measurement* (document AN13917)

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7 Revision history

Table 28 summarizes the revisions to this document.

Table 28. Revision history

Revision number	Release date	Description
1	07 August 2023	Initial public release

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