Freescale Semiconductor
Application Note

MPC8260 SDRAM Support

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This application note supplements the "SDRAM Machine" section of the *MPC8260 PowerQUICC™ II User's Manual*. In particular, it addresses the common misconception that the MPC8260 supports a maximum of only 128 MBytes of synchronous dynamic random access memory (SDRAM). Limitations of an SDRAM machine are not on the total memory it can support, but rather on the type and size of the SDRAM device.

1   Basic SDRAM Capabilities of the MPC8260

The MPC8260 provides one SDRAM machine for the 60x bus and one for the local bus. Although each bus has only one machine, multiple chip selects ($\overline{\text{CS}}$) can be programmed to support multiple SDRAM devices. Note that no limitation exists on the number of chip selects that can be programmed for SDRAM. This means that $\overline{\text{CS}}$[1:11] can be programmed to support SDRAM, assuming $\overline{\text{CS0}}$ is reserved for the general-purpose chip-select machine (GPCM) to connect to Flash memory. See the figure entitled "128-Mbyte SDRAM," in the user's manual for an example of a multiple chip select SDRAM configuration.

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If multiple chip selects are configured to support SDRAM on a single bus, each SDRAM device should have the same port size and timing parameters. This means that all option registers (OR*n*) for the SDRAM chip selects should be programmed exactly the same. All the chip selects on the 60x bus share the same 60x SDRAM mode register (PSDMR) for initialization and the 60x bus-assigned SDRAM refresh timer register (PSRT) and the memory refresh timer prescaler register (MPTPR) for refresh. All chip selects on the local bus share the local bus SDRAM mode register (LSDMR), the local bus-assigned SDRAM refresh timer register (LSRT), and MPTPR. Note that MPTPR is shared by both buses.

For refresh, the memory controller supplies auto refresh (CBR) to SDRAM according to the time interval specified in PSRT or LSRT and MPTPR as follows:

$$\text{Refresh Period} \ = \ \frac{(\text{PSRT or LSRT} + 1) \ \text{x} \ (\text{MPTPR[PTP]} + 1)}{\text{Bus Frequency}}$$

Equation 1.

This represents the time period required between refreshes. When the refresh timer expires, the memory controller requests the bus. If the request is granted, it issues a CBR to each chip select. Each CBR is separated by one clock. A refresh timing diagram for multiple chip selects is shown in the user's manual Table 10-39, "SDRAM Bank-Staggered CBR Refresh Timing."

During a memory transaction on the bus, the memory controller compares the memory address with the address information of each chip select (programmed with BR*n* and OR*n*). If the comparison matches a chip select that is controlled by SDRAM, the memory controller requests service to the 60x or local bus SDRAM machine, depending on the bus information in BR*n*. Although multiple chip selects may be programmed for SDRAM, only one chip select is active at any given time; thus, multiple chip selects can share the same SDRAM machine.

2 Maximum Amount of SDRAM Supported

Table 1 is based on the SDRAM data sheet supplied by Micron.

Table 1. Micron SDRAM Devices

SDRAM Device	64 Mbit			128 Mbit			256 Mbit		
I/O Port	x4	x8	x16	x4	x8	x16	x4	x8	x16
Bank	4	4	4	4	4	4	4	4	4
Row	12	12	12	12	12	12	13	13	13
Column	10	9	8	11	10	9	11	10	9

The data port size is programmable, but the following examples use all 64 bits of the 60x bus. The 64-bit port size requires eight SDRAM devices (with 8-bit I/O ports) connected in parallel to a single chip select. If 128-Mbit devices are used, one chip select provides 128-Mbit/device x 8 devices = 128 MBytes. If 8 chip selects are programmed for SDRAM use, the result is 128 MBytes x 8 = 1 Gbyte. If 256-Mbit SDRAM devices are used (page-based interleaving), the total available memory is 2 Gbyte.

Although there is no technical difficulty in supporting multiple chip select configurations, in practice the user may want to maximize the amount of SDRAM assigned to each chip select to minimize cost.

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3 MPC8260 SDRAM Machine Limitations

This section describes limitations of the MPC8260 SDRAM machine. The maximum size for one chip select is 128 MBytes in bank-based interleaving mode. The following is true for both the MPC8260 60x and local bus SDRAM controller: in page-based interleaving mode during the address bus partition, the address lines used for bank selects cannot be less than A[21] (in relation to big endianess). For example, in Table 10-21 of the *MPC8260 PowerQUICC II User's Manual*, the address lines A[22], A[23], A[24]... cannot be used for the bank select signal.

3.1 Column Number Limitation for MPC8260 Rev. A and B

Revisions A and B of the MPC8260 do not support more than 10 columns when in single-MPC8260 mode. An SDRAM device that has 11 columns uses A11+A[9:0] as the column address. (A10 is reserved for auto-precharge.) Notice that during READ/WRITE, the logical address A10 has to be multiplexed to the physical address pin A11, but this multiplexing is not supported on revisions A and B of the MPC8260. Beginning with revision C of the MPC8260 and beginning with revision A of the MPC8260A (HiP4), the SDAMUX signal is enabled in single-MPC8260 mode and can be used with an external mux to overcome the column-number limitation in earlier revisions. See the 1-Gbyte example in Section 4.3, "1-Gbyte SDRAM Memory Module." In 60x-compatible mode, the user is responsible for row/column address multiplexing with the SDAMUX signal. Logic column address A10 can be easily multiplexed to physical column address A11. In other words, the column number limitation is not an issue.

3.2 Analysis of Maximum Row Number Due to Bank Select Mux

PSDMR[BSMA] is used to multiplex the bank select address. What follows is the BSMA field and corresponding multiplexed address.

```
000 A12–A14

001 A13–A15

…

111 A19–A21
```

3.2.1 60x Bus

The highest address pins that the bank selects can be multiplexed with are A[12:14], which limits the pins for the row address to A[15:31]. In the case of a 64-bit port, A[29:31] are not connected. The maximum row is A[15:28] (14 rows). For smaller port sizes, the row number can be greater. For example, in a 32-bit port, only A[30:31] are not connected; A[15:29] can be used for the row address (15 rows). The Micron 256-Mbit device has only 13 rows.

3.2.2 Local Bus

The local bus has only the lower 18 address bits (L_A[14:31]). If L_A14 and L_A15 are used for bank select, L_A[16:31] can be used for the row address. For a 32-bit port, the maximum width of the local bus, L_A[30:31] are not connected, and the maximum row number is 14. In short, the MPC8260 supports 14 or more rows that are sufficient for all devices.

3.3 Inflexibility of Multiplexing Bank Select Signals to Higher Address Pins in Bank-Based Interleaving

Normally, bank selects are multiplexed to the address pins immediately above the row address. Refer to the example in the section on "SDRAM Configuration Example (Page-Based Interleaving)," and the section on "DRAM Configuration Example (Bank-Based Interleaving)" in the user's manual. For both of these interleaving examples, bank-select signals are multiplexed to A[15:16]. Page-based interleaving, however, allows bank signals to be multiplexed to the higher-order address pins to leave room for future upgrades. For example, a user could multiplex the bank select signals to A[14:15], leaving A16 to connect to the address pin for a larger memory size.

Bank-based interleaving has no such flexibility. If you attempt to multiplex the bank select signals to A[14:15], an incorrect value is multiplexed. Namely, the logical address A[5:6] is multiplexed instead of the correct value A[6:7].

You can also use dedicated BNKSEL pins instead of multiplexing bank select signals to the higher order address pins. For page-based interleaving, the value of SDMR[BSMA] has no effect. The correct bank select signals are always output to the BNKSEL*n*. But for bank-based interleaving, BNKSEL*n* are correct only if BSMA is programmed so that the bank select signals are multiplexed to the address pins immediately above the row address.

3.4 Analysis of Row Address Multiplexing

The SDMR[SDAM] field multiplexes the row address during an ACTIVATE command. It applies to both page- and bank-based interleaving. For two banks, one address pin is assigned for bank select, two address pins are assigned for four banks, and three address pins are assigned for eight banks. The following analysis is based on four banks (because all Micron SDRAMs have four) and a 60x bus. The analysis uses SDAM = 101 (example from the table entitled "SDRAM Address Multiplexing" in the user's manual). See Table 2.

Table 2. SDRAM Address Multiplexing when SDAM = 101

Physical Address	A12	A13	A14	A15	…	A28	A29	A30	A31
Logical Address	—	A0	A1	A2	…	A15	A16	A17	A18

For both page-based and bank-based interleaving modes, the row address is determined as follows. For a port size of 64 bits, A[29:31] are not connected. If the bank-select signals are multiplexed to the highest possible physical address A[12:14] (to maximize the row number), the physical row address is A[15:28], which corresponds to logical address A[2:15]. Thus, the maximum row number is 14. The column number is determined as follows: for page-based interleaving, because the logical row address is determined to be A[2:15], the logical address can only be partitioned as in Table 3. The logical address A[16–17] are for bank selects. The logical address partition for the column address is A[18:31]. Because the port size is 64 bits, A[29:31] are not connected. Thus, only A18-A28 are used for logical column address.

Table 3. Logical Address Partition for Page-based Interleaving

Address Partition	Row			Bank		Column		
Logical Address	A2	…	A15	A16	A17	A18	…	A31

For bank-based interleaving, the bank selects are of higher order than the row address and are partitioned as in Table 4. The logical address partition for the column address is A16-A31, but because the port size is 64-bit, only A16-A28 are used for the logical column address. (A29-A31 are not connected.)

Table 4. Logical Address Partition for Bank-based Interleaving

Address Partition	Bank		Row			Column		
Logical Address	A0	A1	A2	…	A15	A16	…	A31

Table 5 summarizes the port size and column and row number for each SDAM configuration. The row number is the maximum allowed for that configuration. The column number is exact for that SDAM configuration. Note that Table 5 and Table 6 refer to 4-bank SDRAM devices only.

Table 5. Page-based Interleaving (60x bus, 4-bank)

SDAM	Port Size			
	64	32	16	8
000	6 col x 14 row	6 col x 15 row	6 col x 16 row	6 col x 17 row
001	7 col x 14 row	7 col x 15 row	7 col x 16 row	7 col x 17 row
010	8 col x 14 row	8 col x 15 row	8 col x 16 row	8 col x 17 row
011	9 col x 14 row	9 col x 15 row	9 col x 16 row	9 col x 17 row
100	10 col x 14 row	10 col x 15 row	10 col x 16 row	10 col x 17 row
101	11 col x 14 row	11 col x 15 row	11 col x 16 row	11 col x 17 row

Table 6. Bank-based Interleaving (60x bus, 4-bank)

SDAM	Port Size			
	64	32	16	8
000	8 col x 14 row	8 col x 15 row	8 col x 16 row	8 col x 17 row
001	9 col x 14 row	9 col x 15 row	9 col x 16 row	9 col x 17 row
010	10 col x 14 row	10 col x 15 row	10 col x 16 row	10 col x 17 row
011	11 col x 14 row	11 col x 15 row	11 col x 16 row	11 col x 17 row
100	12 col x 14 row	12 col x 15 row	12 col x 16 row	12 col x 17 row
101	13 col x 14 row	13 col x 15 row	13 col x 16 row	13 col x 17 row

NOTE

When SDAM = 101 for page-based interleaving and when SDAM = 011, 100, 101 for bank-based interleaving, the column number is more than 10. In single-MPC8260 mode, revisions A and B cannot use these SDAM values. However, the MPC8260A (HiP4) and revision C of the MPC8260 can use these values but require an external multiplexer.

4 Examples

This section shows examples of specific modules.

4.1 SDRAM of 256 MBytes
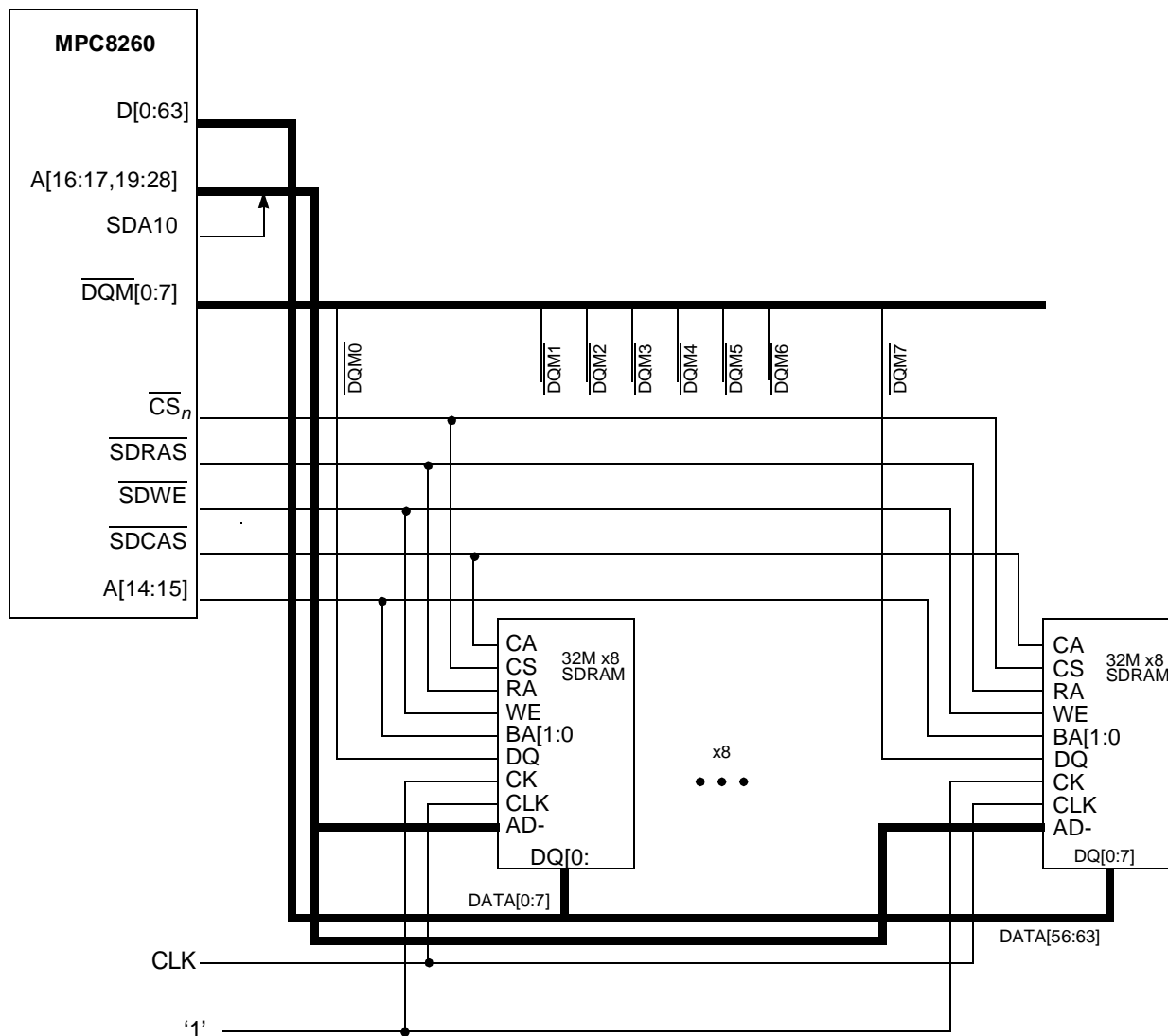
Figure 1shows an SDRAM of 256 Mbytes.

Figure 1. 256-Mbyte SDRAM Diagram

Consider the following SDRAM organization:

- The 64-bit port size is organized as 8 x 8 x 32 Mbit.
- Each device has four internal banks, 13 row address lines, and 10 column address lines.

The address bus is partitioned as shown in Table 7.

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Table 7. 60x Address Bus Partition

A[0:3]	A[4:16]	A[17:18]	A[19:28]	A[29:31]
msb of start address	Row	Bank select	Column	lsb

The following parameters are extracted:

- PSDMR[PBI] = 1, page-based interleaving
- BPD = 01, four internal banks
- ROWST = 100, row starts at A[4]
- NUMR = 100, 13 row lines

During an ACTIVATE command, the SDRAM address port is set as in Table 8.

Table 8. SDRAM Device Address Port During ACTIVATE Command

A[0:13]	A[14:15]	A[16:28]	A[29:31]
—	Internal bank-select A[17:18]	Row A[4:16]	no-connect

To multiplex A[4:16] over A[16:28], set PSDMR[SDAM] to 100 and, because the internal bank selects are multiplexed over A[14:15], PSDMR[BSMA] must be set to 001. Only the lower two bank select lines are used. Refer to Table 10-19, "SDRAM Address Multiplexing," in the user's manual.

Table 9 shows the address port configuration during a READ/WRITE command.

Table 9. SDRAM Device Address Port During READ/WRITE Command

A[0:13]	A[14:15]	A[16, 17]	A[18]	A[19:28]	A[29:31]
—	Internal bank select	Don't care	AP	Column	no-connect

Because AP alternates with row line A6, set PSDMR[SDA10] to 100. This outputs A6 on the SDA10 line during the ACTIVATE command and AP during READ/WRITE and CBR commands. SDA10 is connected to the appropriate SDRAM address bit, A10. Table 10 shows the register configuration. Not shown are PSRT and MPTPR, which should be programmed according to the refresh requirements of the device.

Table 10. Register Setting for 256 Mbyte SDRAMs

Register	Field	Value
BRx	BA	Base address
	PS	00 = 64-bit port size
	MS	010 = SDRAM-60x bus
	V	1

Table 10. Register Setting for 256 Mbyte SDRAMs (continued)

Register	Field	Value
OR*x*	USDAM	11110
	SDAM	0000000
	LSDAM	00000
	BPD	01
	ROWST	0100
	NUMR	100
PSDMR	PBI	1
	RFEN	1
	OP	000
	SDAM	100
	BSMA	001
	SDA10	100
	RFRC	From device data sheet
	PRETOACT	From device data sheet
	ACTTOROW	From device data sheet
	BL	0
	LDOTOPRE	From device data sheet
	WRC	From device data sheet
	CL	From device data sheet

4.2   512 MByte SDRAM Module

Figure 2, MT16LSDT6464A with 512 Mbytes, is from Micron. This matches the former example but uses two chip selects.
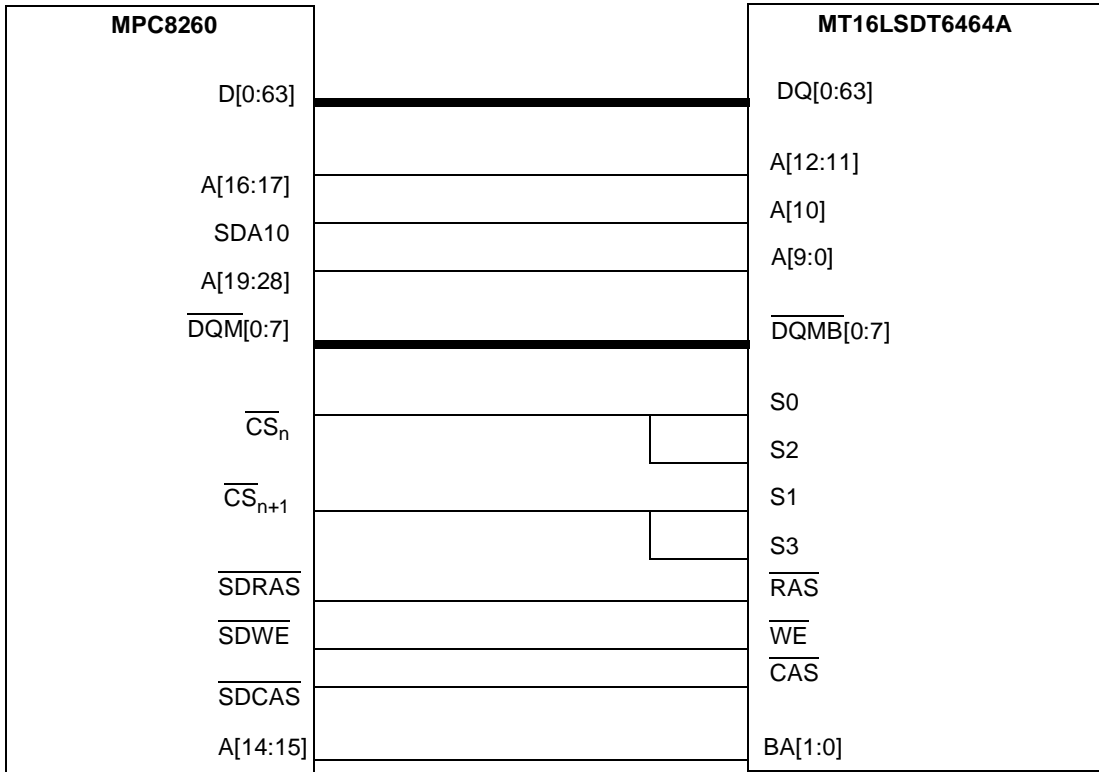
Figure 2. Example of a 512-Mbyte SDRAM Configuration Using an MT16LSDT6464A

4.3   1-Gbyte SDRAM Memory Module

This example uses an MT36LSDF12872G from Micron.
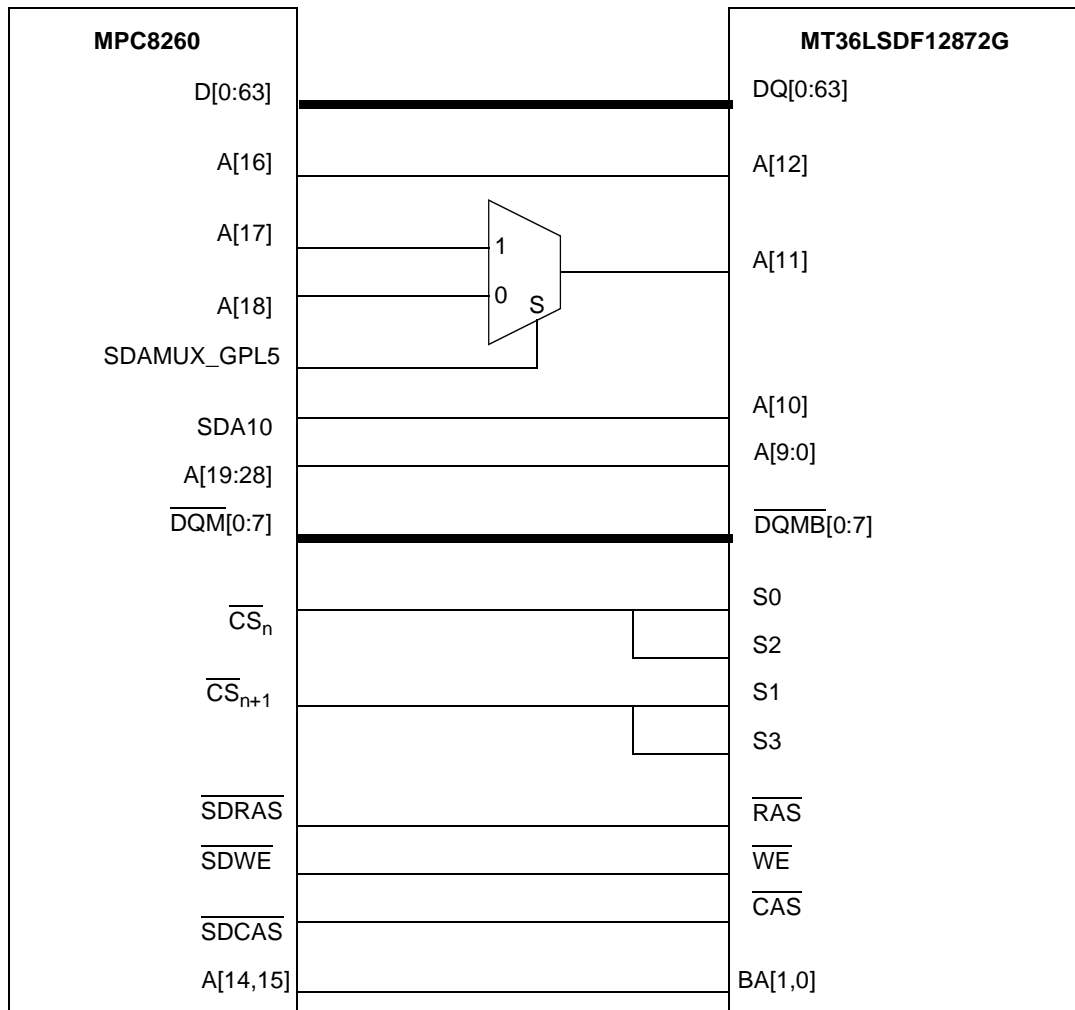
Figure 3. MT36LSDF12872G Example

In this SDRAM organization:

- The 64-bit port size is 16 x 4 x 64 Mbit x 2 chip select lines.
- Each device has 4 internal banks, 13 row address lines, and 11 column address lines.

The address bus is partitioned as shown in Table 11.

Table 11. 60x Address Bus Partition

A[0:2]	A[3:15]	A[16:17]	A[18:28]	A[29:31]
msb of start address	Row	Bank select	Column	lsb

The following parameters can be extracted:

- PSDMR[PBI] = 1, page-based interleaving
- BPD = 01, four internal banks
- ROWST = 011, row starts at A[3]
- NUMR = 100, 13 row lines

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During an ACTIVATE command, the SDRAM address port is set as in Table 12.

Table 12. SDRAM Device Address Port During ACTIVATE Command

A[0:13]	A[14:15]	A[16:28]	A[29:31]
—	Internal bank select (A[16:17])	Row (A[3:15])	no-connect

To multiplex A[3:15] over A[16:28], set PSDMR[SDAM] to 101 and, because the internal bank selects are multiplexed over A[14:15], PSDMR[BSMA] must be set to 001. Only the lower two bank select lines are used. Refer to Table 10-19, "SDRAM Address Multiplexing," in the *MPC8260 PowerQUICC II User's Manual.*

Table 13 shows the address port settings during a READ/WRITE command.

Table 13. SDRAM Device Address Port During READ/WRITE Command

A[0:13]	A[14:15]	A[16]	A[17]	A[18]	A[19:28]	A[29:31]
—	Internal bank select	Don't care	Column	AP	Column	no-connect

Because AP alternates with the msb of the row line A5, set PSDMR[SDA10] to 101. This outputs A5 on the SDA10 line during the ACTIVATE command and AP during READ/WRITE and CBR commands. SDA10 is connected to the appropriate SDRAM address bit, A10. An external multiplex is needed for proper generation of A11. Table 14 shows the register configuration. Not shown are PSRT and MPTPR, which should be programmed according to the refresh requirements of the specific device.

Table 14. Register Settings for1-Gbyte SRAMs

Register	Field	Value
BRx	BA	Base address
	PS	00 = 64-bit port size
	MS	010 = SDRAM-60x bus
	V	1
ORx	USDAM	11100
	SDAM	0000000
	LSDAM	00000
	BPD	01
	ROWST	0011
	NUMR	100

Table 14. Register Settings for 1-Gbyte SRAMs (continued)

Register	Field	Value
PSDMR	PBI	1
	RFEN	1
	OP	000
	SDAM	101
	BSMA	001
	SDA10	101
	RFRC	From device data sheet
	PRETOACT	From device data sheet
	ACTTOROW	From device data sheet
	BL	0
	LDOTOPRE	From device data sheet
	WRC	From device data sheet
	CL	From device data sheet

Table 15. Document Revision History

Revision Number (Rev.)	Changes
0	—
0.1	Addition of section on limitations of Page-Based Interleaving mode
2	Nontechnical formatting; rebranding for Freescale

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