Freescale Semiconductor
Application Note

Document Number: AN2584
Rev. 1, 1/2007

Migrating from the MPC852T to the MPC875

by *Ned Reinhold*
NCSD Applications
Freescale Semiconductor, Inc.
Austin, TX

This document presents information that is useful when migrating from the MPC852T to the MPC875. For more detailed information, refer to the *MPC885 PowerQUICC™ Family Reference Manual* and *MPC875/MPC870 Hardware Specifications (*for MPC875*)*, and the *MPC866 PowerQUICC™ Family Users Manual* and *MPC852T Hardware Specifications (*for MPC852T*).*

The need for embedded security and an additional fast Ethernet channel makes the transition from an MPC852T to an MPC875 a logical progression. Both processors contain the same embedded PowerPC^{TM} architecture-based core and system integration unit (SIU) to ease software migration.

The MPC875 has twice the internal L1 cache as the MPC852T for a total of 8 Kbytes for data and 8 Kbytes for instructions. The MPC875 has a faster core and faster bus speed than the MPC852T. The MPC875 incorporates four 16-bit timers that can be cascaded into two 32-bit timers.

The MPC875 incorporates two fast Ethernet channels instead of one and has a similar CPM. However, the variety of serial channels has changed. The MPC875 supports an I^2C controller and an internal security processor that can perform encryption on the serial channels and TDM interface.

Contents

freescale™ semiconductor

1 Feature Comparison

Figure 1 and Figure 2 show block diagrams for MPC875 and MPC852T, respectively. The MPC852T and MPC875 communications microprocessors incorporate many types of communications engines to accommodate different system requirements. The following sections compare the hardware and protocol features of these microprocessors.

1.1 Hardware Features

Table 1 compares MPC852T and the MPC875 hardware features.

Table 1. Hardware Features Comparison

Feature	852T	875
Core frequency (max)	100 MHz	120 MHz
Bus frequency (max)	66 MHz	80 MHz
I and D cache	4K	8K
FEC	1	2
Security	No	Yes
USB1.1	No	Yes
Time slot assigner (TSA)	No	Yes
SPI	1	1
SMC	1	1
SCC	2	1
PCMCIA	Yes	Yes

1.2 Protocol Features

Table 2 compares MPC852T and the MPC875 protocol features.

Table 2. Protocol Feature Comparison

Protocol	MPC852T	MPC875
10/100 Fast Ethernet	1	2
10BT Ethernet	Yes	Yes
HDLC/SDLC	Yes	Yes
UART	Yes	Yes
Transparent	Yes	Yes

2 MPC875

The MPC875 PowerQUICC™ processor is a 0.18-micron version of the MPC860 PowerQUICC family of communications microprocessors. Like the MPC852T, the MPC875 has a core voltage of 1.8 V and an

I/O voltage of 3.3 V, with 5 V input compatibility. The MPC875 supports a maximum core speed of 120 MHz and a maximum external bus speed of 80 MHz (in 1:1 mode). It incorporates the same embedded MPC8*nn* processor core and similar CPM and SIU. The MPC875 also supports an on-chip security engine and two 10/100 fast Ethernet controller modules. The CPM supports USB 1.1, one SCC (SCC4), SMC1, and the SPI. The SCC can support 802.3 Ethernet, HDLC/SDLC, UART, and transparent protocols. Figure 1 shows the MPC875 block diagram.

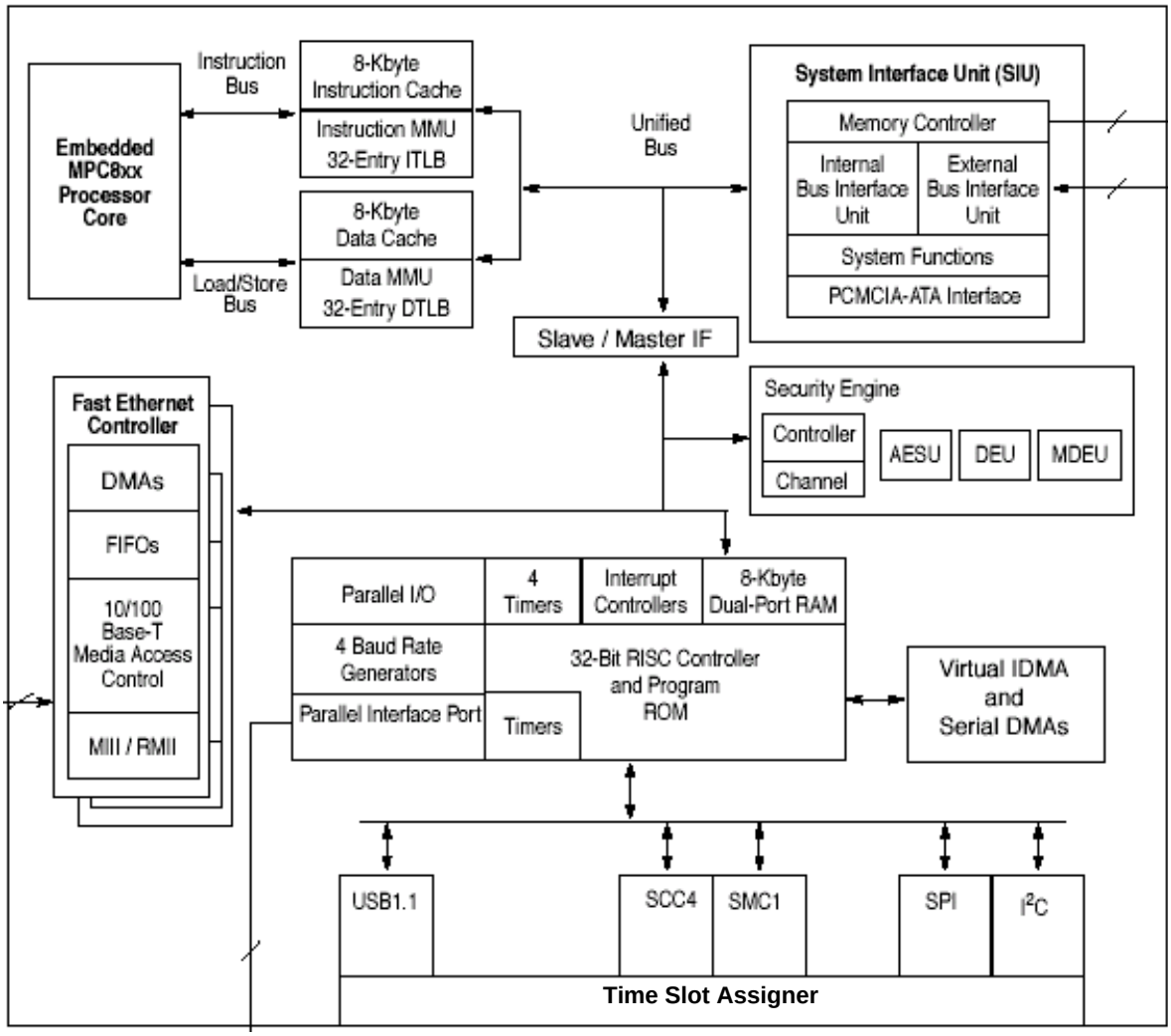

Figure 1. MPC875 Block Diagram

3 MPC852T

The MPC852T PowerQUICC is a 0.18-micron version of the MPC8*nn* PowerQUICC family of communications microprocessors. Like the MPC875, the MPC852T has a core voltage of 1.8 V and an I/O voltage of 3.3 V, with 5V-compatibility. The MPC852T supports a maximum core speed of 100 MHz and a maximum external bus speed of 66 MHz. The MPC852T incorporates the same embedded MPC8*nn* processor core and similar CPM and SIU as the MPC8*nn* family. The MPC852T features one 10/100 fast Ethernet controller module. The CPM supports two SCCs (SCCs 3 and 4), SMC1, and the SPI. The SCCs can support JTAG® 802.3™ Ethernet, HDLC/SDLC, UART, and transparent protocols.

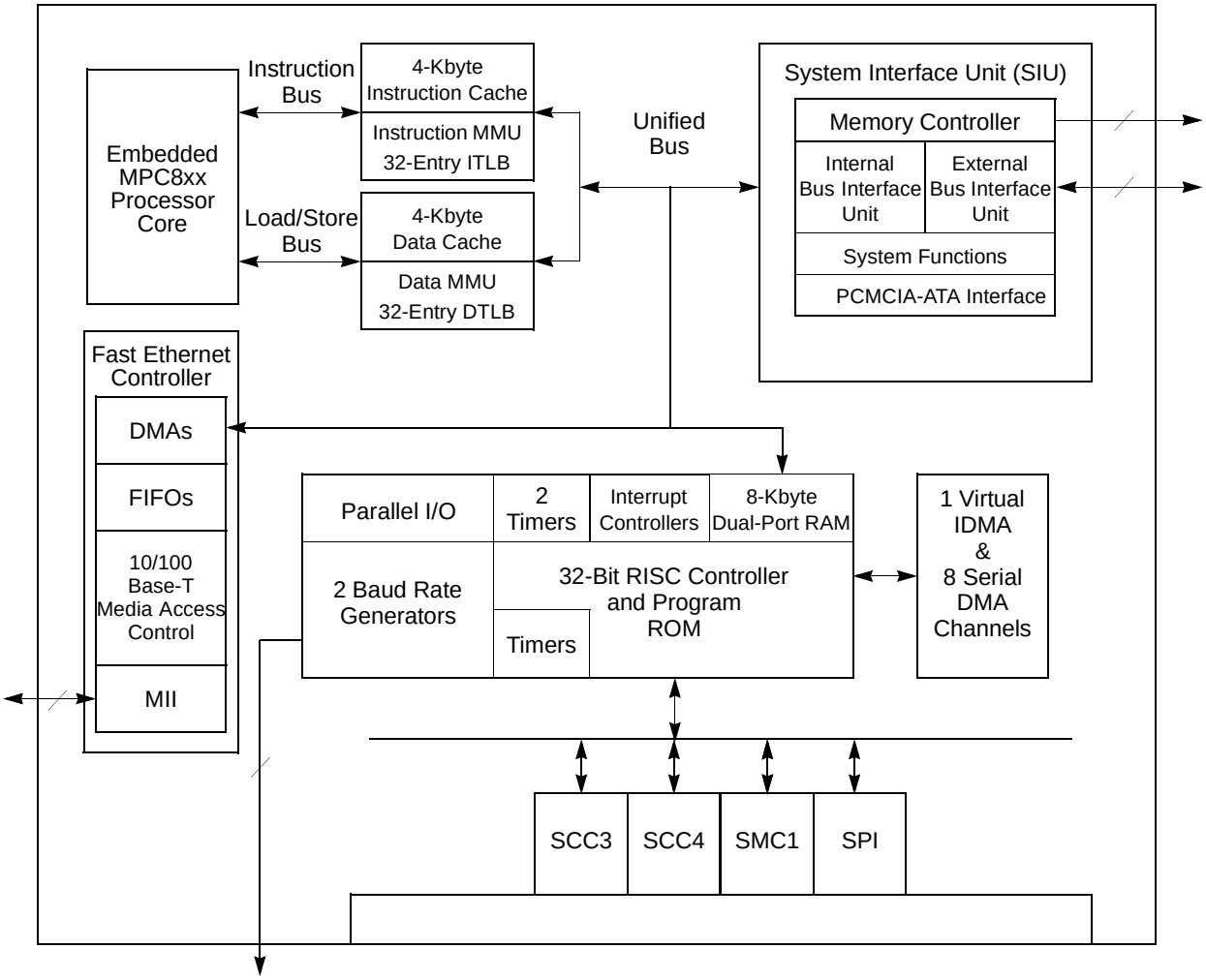

Figure 2. MPC852T Block Diagram

4 Similarities and Differences Of MPC852T and MPC875

The following sections discuss MPC852T and MPC875 differences for pinout and memory mapping.

4.1 Pinout

Both the MPC852T and the MPC875 use the 256 plastic ball grid array (PBGA) package. Buses and other functions are grouped in a logical order, but reuse of layout is not available. Parallel ports changed from four (Port A, B, C, and D) on the MPC852T to five (Port A, B, C, D, and E) on the MPC875. Each signal in the I/O ports can be configured as a general-purpose I/O signal or as a signal dedicated to communications peripherals, such as Ethernet or USB. For details, see the *MPC885 PowerQUICC™ Family User's Manual*.

Figure 3 shows the MPC875 pinout.

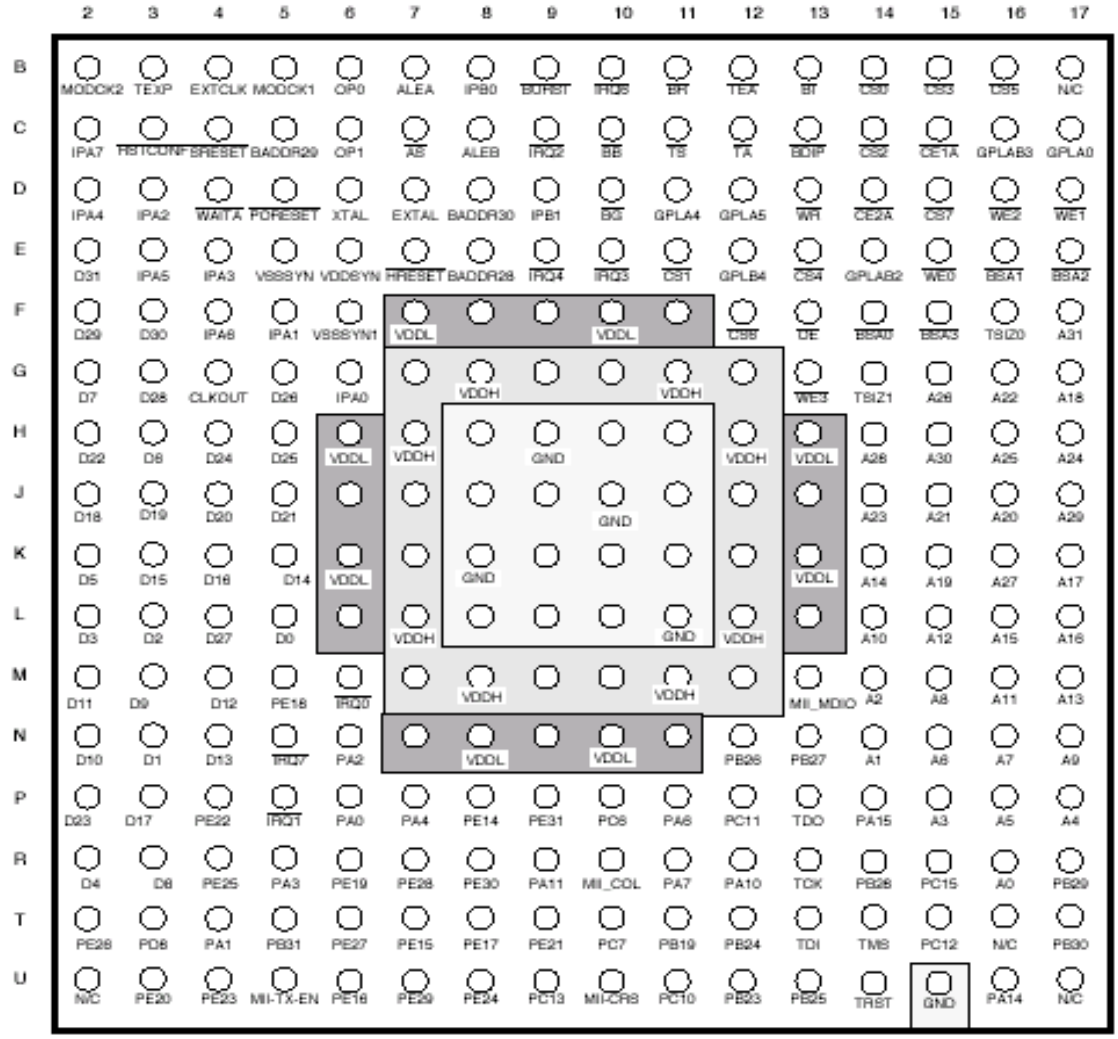

Figure 3. MPC875 Pinout

Figure 4 shows the MPC852T pinout.

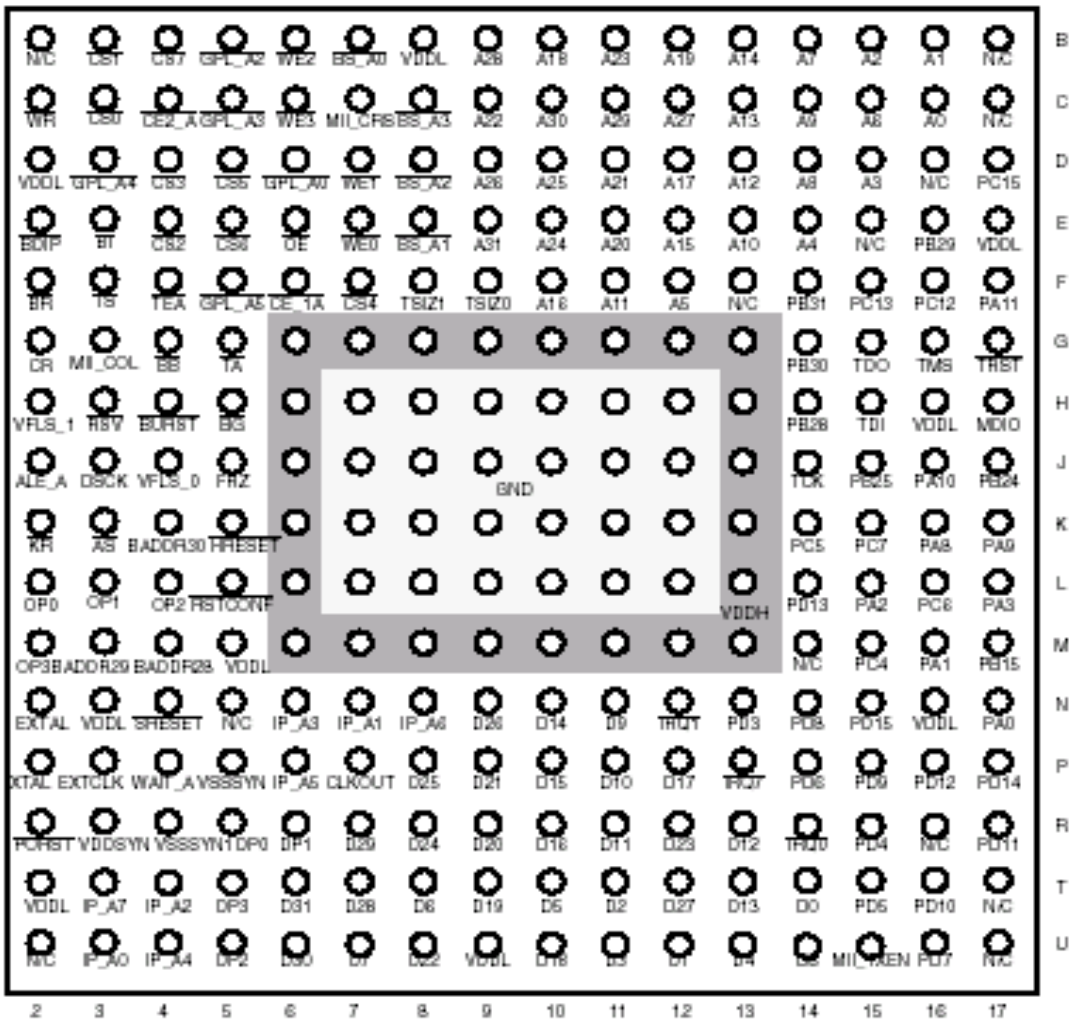

Figure 4. MPC852T Pinout

4.2 Memory Map

The memory maps for both the MPC852T and the MPC875 are very similar except that on the MPC875 SCC1 is replaced with a USB 1.1 controller and port E registers reside in a previously reserved area of the port B registers.

On the MPC852T, the registers mapped for the FEC are now mapped for FEC1, with direct compatibility.

On the MPC875, the registers for FEC2 are located in a formerly reserved area of the internal memory map, and begin at address 1E00. For ease of porting, FEC2 registers are located in the same order as FEC1, with offset for FEC2 equal to FEC1 plus 0x1000.

Dual-port RAM for both processors is from IMMR + 0x2000–0x2FFF, with expanded dual-port RAM from 0x3000–0x3BFF.

5 New Features of MPC875

The following sections discuss new features of MPC875.

5.1 IMMR[ISB] Bits 14–15

The IMMR[ISB] bits have new meaning with the MPC875. When these bits are cleared, the internal memory map is the same as in previous iterations of PowerQUICC. When ISB = 10, the registers for the security engine become available.

5.2 Security Engine

The block diagram of the internal architecture of the security engine is shown in Figure 5. The MPC8*nn* bus interface module transfers 32-bit words between the MPC8*nn* bus and any register inside the security engine core.

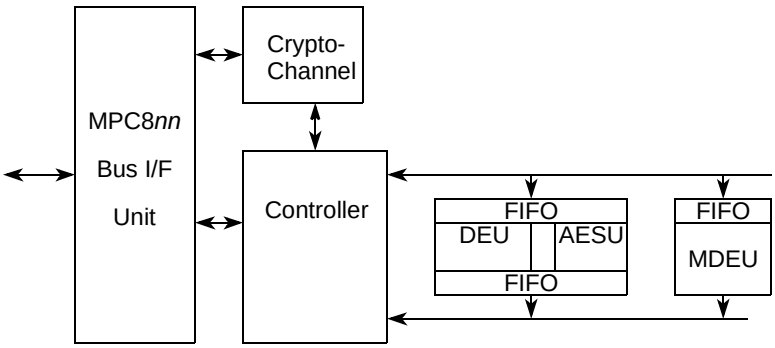

Figure 5. Security Engine Functional Blocks

An operation begins with a write of a pointer to the crypto-channel fetch register, which points to a data packet descriptor. The channel requests the descriptor and decodes the operation to be performed. The channel then asks the controller to assign crypto execution units and fetch the keys, IVs, and data needed to perform the specific operation. The controller assigns execution units to the channel and makes requests to the master interface to satisfy the requests. As data is processed, it is written to the individual executions unit's output buffer and then back to system memory by means of the MPC8*nn* bus interface module.

The internal registers for the security engine can be accessed when IMMR[ISB] = 10. The *MPC885 PowerQUICC Family Reference Manual* lists details of the registers and their locations in the internal memory map.

6 Summary

Although the migration from the MPC852T to the MPC875 requires layout and software changes, the benefits of an additional fast Ethernet controller, USB1.1, and an internal security engine may warrant the migration, depending on system requirements.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: AN2584
Rev. 1
1/2007