**Freescale Semiconductor**
Application Note

Document Number: AN3276
Rev. 0.3, 01/2010

# Interfacing the MC13783 Power Management IC with i.MX31 Applications Processors

**by: Power Management and i.MX31 Application Teams**

## 1 Introduction

The purpose of this application note is to provide information for the development of the power management section of a product that incorporates an i.MX31 processor or similar processor and a power management IC (PMIC) such as the MC13783.

The i.MX31 applications processors incorporate numerous features to enhance use time and battery life by reducing power consumption.

These features include:

- Power gating
- Variety of low power modes
- Smart techniques for short wake-up time from low power modes
- Dynamic Process Temperature Compensation (DPTC)
- Automatic Dynamic Voltage and Frequency Scaling (DVFS, sometimes shortened to DVS for Dynamic Voltage Scaling)
- Low-power clocking scheme
- Active Well Bias (AWB)

### Contents

Some of these features are implemented entirely within the i.MX31; others such as dynamic voltage scaling, dynamic process temperature compensation of voltage and power gating require the use of a power management device designed with i.MX31 in mind.

Freescale's MC13783 power management IC is designed with all of the power management, logic and audio features needed for an advanced 3G cell phone or other portable devices using the i.MX31 as an applications processor.

At the heart of the MC13783 is a bank of programmable buck (step-down) switching regulators. These switching regulators are designed to accommodate the dynamic voltage changes needed for DVS and DPTC.

# 2 Power Management Basics

This section forms an introduction to the basics of power management in order to design an advanced portable product such as a media player or a 3G cell phone.

## 2.1 Power

The i.MX31 processor typically requires 3 or 4 separate power rails, while the various peripheral devices, memory, interface, lighting, wireless module, display, etc. also require power. In all, 10 to 20 independent power rails are often required.

This power is sourced either from a battery, the battery charge supply or an external supply. Multiple power rails are generated to operate the processor and the various peripherals or modules in the product.

Battery life of a portable product is a key metric and very visible to an end user, so efficient power management using the MC13783 helps to optimize system design and performance.

## 2.2 Additional PMIC Functions

In addition to simply providing power rails, the following functions are often required by the i.MX31 of the PMIC:

1. Ability to operate from a single battery (typically 3.6 V) and external DC
2. Battery charging from multiple sources (wall charger, USB, etc.)
3. ON/OFF, system reset, battery monitoring and shut-down mechanism
4. Power sequencing and a selection of pre-programmed default power modes
5. Ability to perform load-switching
6. Ability to perform voltage and frequency scaling depending on CPU load and ambient temperature conditions to reduce dynamic power loss
7. Ability to reduce static power loss
8. Ability to operate in different power modes for efficiency

Additional functions that may or may not be needed depending on the product being designed, but are often included in Freescale's PMICs such as the MC13783 are:

1. Digital audio (voice CODEC, stereo DAC, etc.)
2. Analog audio (amplifiers, switches, microphone inputs, mono and stereo headset and speaker amplifiers, etc.)
3. Lighting drivers
4. RTC and back up battery
5. USB OTG full speed interface
6. Housekeeping ADC and analog multiplexer

## 2.3 Battery Input and Regulator Output Voltages

The regulators on the PMIC are normally powered by the system battery and in special cases, one regulator will be powered from another. For instance, a low voltage linear regulator might be powered by the output of a buck switching regulator.

Therefore, the input power to the PMIC is nominally 3.6 V, but will vary from 4.2 V when the battery is fully charged to approximately 2.8 V when it is discharged to the end of its useful range. The PMIC may also need to operate from a 5 V external supply, often the charger supply.

Any supply rail that is required must always be above the battery range, such as 5 V for backlights or the USB-OTG VBUS must be generated by a "boost" switching regulator. Any supply rail that is always below 2.8 V can be generated either by a linear LDO regulator or a "buck" switching regulator.

A linear LDO regulator can be used to drop a voltage from the input voltage to its output voltage. This uses typically only one off-chip component, a capacitor. From a simplicity and cost point of view, it is very desirable. However, the input and output current are about same, so the efficiency of the part is equal to the ratio of output to input voltage, and power dissipation is directly related to the voltage drop from input to output. For low voltage outputs, an efficiency improvement may be realized by powering the LDO from a buck switcher, for instance, a 1.5 V LDO can be powered by a 1.8 V buck. If such a regulator were sourcing 100 mA, it would be 36% efficient and dissipate 270 mW if powered by the fully charged battery. Whereas, if powered by the 1.8 V buck (85%), the net efficiency would be 71% and net dissipation 60 mW.

# 3 MC13783 Overview

The MC13783 power management IC was designed to power all of the functional modules on an advanced 3G cell phone. The power processing and distribution features of the IC include power rails for cell phone-specific items such as the RF modules, baseband processor, audio, SIM card, vibrator, etc. Since a modern high-end cell phone incorporates a complete hand-held computer, the MC13783 also includes all of the specialized power rails needed for the applications processor, peripherals and memory that make up that computer.

However, the MC13783 is protocol independent, and many of the core functions and peripheral supplies are equally well suited to non-phone applications built with the MC13783 and i.MX (MCIMX31) application processor lineup.

## 3.1 MC13783 Power Tree

Figure 1 shows the power source of the MC13783 (yellow) and the various loads they would supply in a typical advanced portable device application (green).

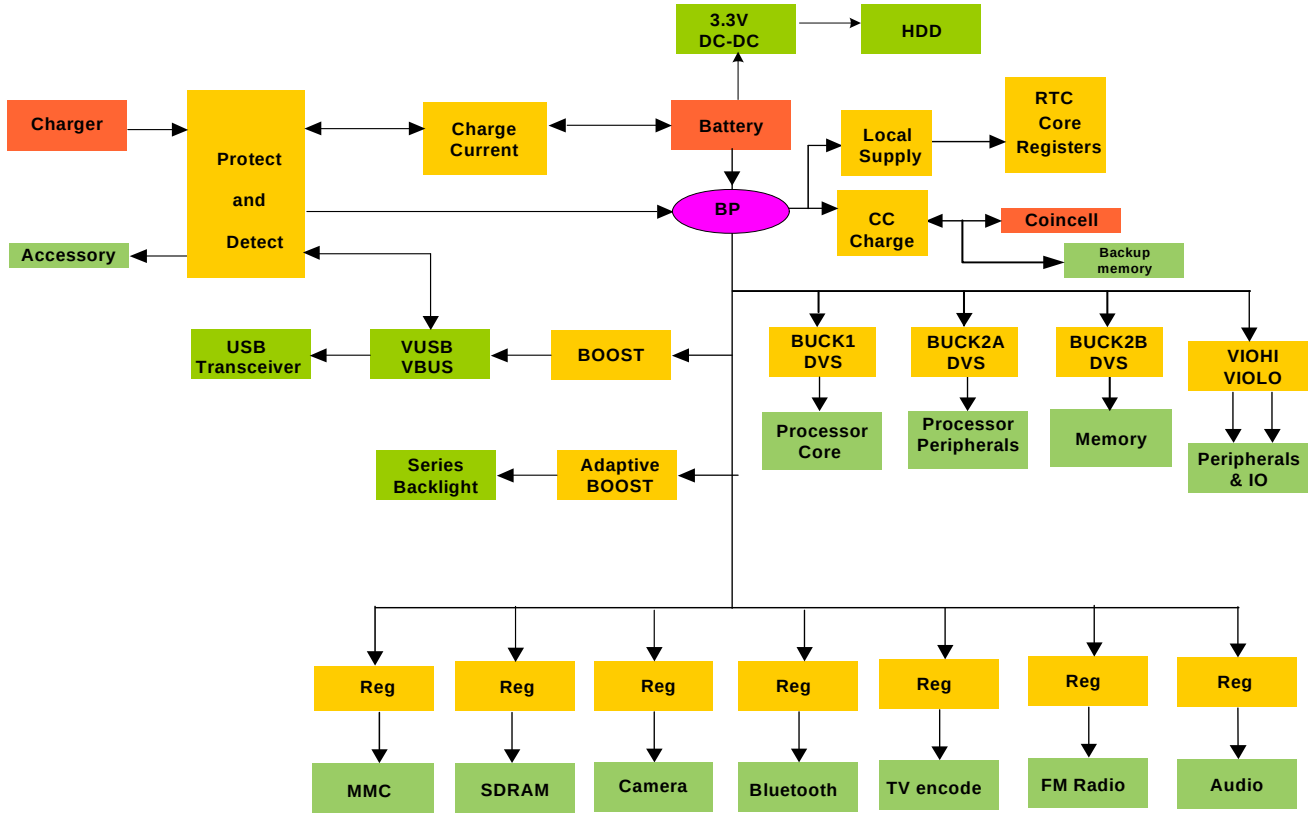



**Figure 1. MC13783 Power Source**

## 3.2 MC13783 Voltage Rails

The MC13783 is capable of supplying the voltages at the listed current as shown in Table 1. Additional supply rails not listed are available for powering system peripherals; see the *MC13783 Power Management and Audio Circuit Data Sheet* (MC13783/D) or the *MC13783 User's Guide* for details.

**Table 1. MC13783 Voltage Rails**

| Name | Voltage(s) (V) | Current mA | Notes |
|---|---|---|---|
| Buck 1A | 0.9–2.2 | 500 | These two can be combined |
| Buck 1B | 0.9–2.2 | 500 | – |
| Buck 2A | 0.9–2.2 | 500 | These two can be combined |
| Buck 2B | 0.9–2.2 | 500 | – |
| Boost | 5.0, 5.5 | 300–350 | – |
| VAUDIO | 2.775 | 200 | – |

**Table 1. MC13783 Voltage Rails (continued)**

| Name | Voltage(s) (V) | Current mA | Notes |
|---|---|---|---|
| VIOHI | 2.775 | 200 | – |
| VDIG | 1.2, 1.3, 1.5, 1.8 | 150–200 | – |

Many of these are named for the typical circuit modules they power in a 3G cell phone application, but they are generically applicable for allocation to any system need with the capability for each respective supply. Refer to Section 6.2, "Hardwired Default Settings," for the default voltage and turn-on sequence.

## 3.3 MC13783 Block Diagram

The full IC block diagram is shown in Figure 2 for reference.

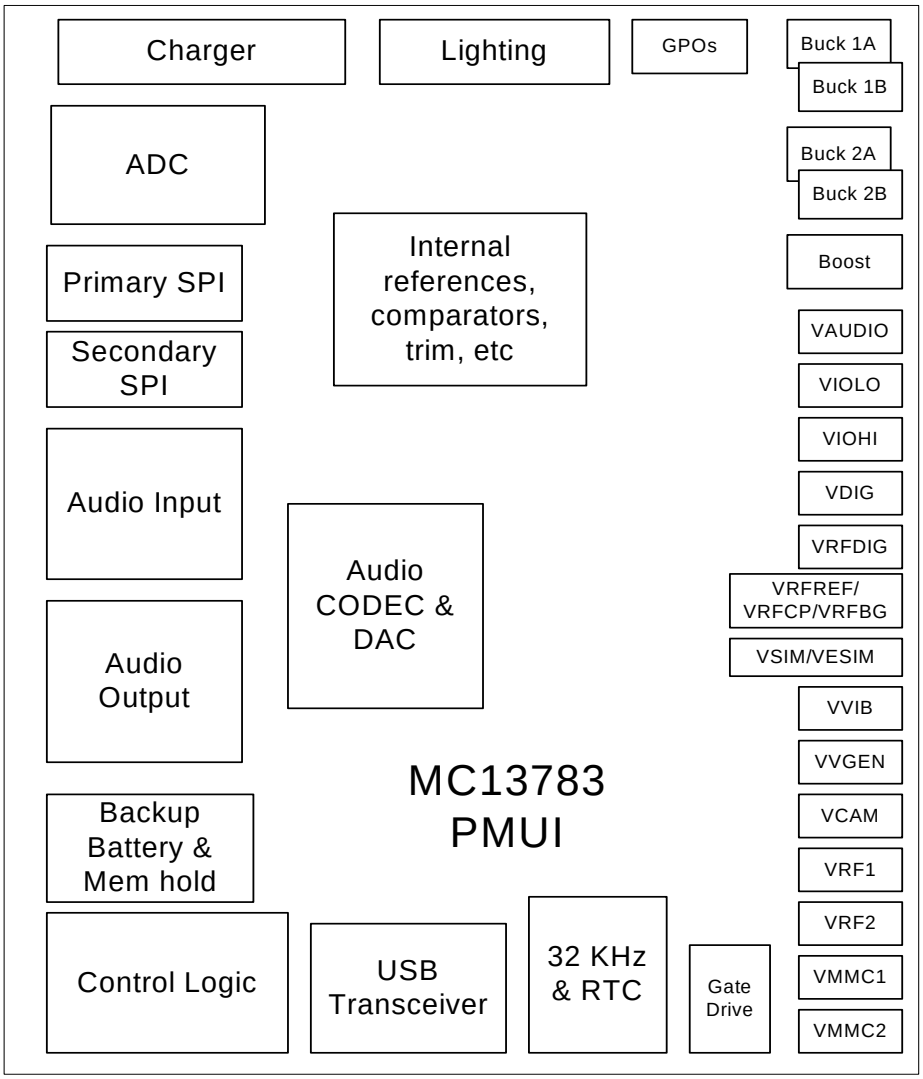



**Figure 2. MC13783 Block Diagram**

# 4 i.MX31 Overview

The following information is presented to better understand the requirements and power management features of the i.MX31.

## 4.1 Introduction to the i.MX31 Processor

The i.MX31 (MCIMX31) is a multimedia applications processor that represents the next step in low-power, high-performance application processors. Based on an ARM11™ microprocessor core, the i.MX31 provides the performance with low power consumption required by modern digital devices.

The i.MX31 incorporates a number of power savings features, among these are:

- DPTC—Dynamic Process Temperature Compensation
- DVFS—Dynamic Voltage and Frequency Scaling
- Power Gating

The following sections detail these power saving features.

## 4.2 Dynamic Process Temperature Compensation

Dynamic process temperature compensation (DPTC) is a routine that is running continuously on i.MX31 and the flow chart is shown in Figure 3.

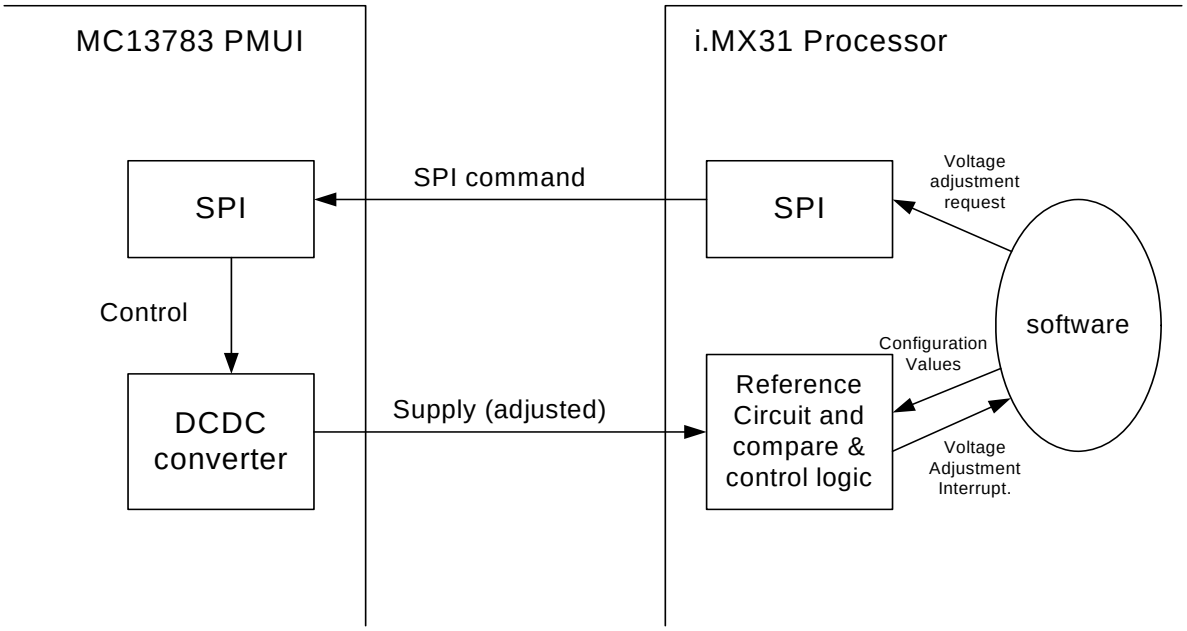



**Figure 3. Dynamic Process Temperature Compensation Flow Chart**

A small hardware routine runs and compares its own performance at the transistor level. It then commands the PMIC to increase or decrease the voltage to change or hold the IC's power supply in order to keep the transistor level performance as required. From part to part and over temperature, the voltage needed for optimum performance may vary.

Production variations in ICs exhibit different characteristics causing each part to need different values of voltage from one temperature extreme to the other. The DPTC adjusts the voltage feed to the IC using the lowest voltage to obtain the specific performance, This action assures lower overall system power consumption than if the voltage were set to a higher fixed predetermined level that is calculated to assure the worst case performance doesn't exceed specified values.

The DPTC control system establishes the high operate voltage for full performance. The MC13783 has the finely programmable voltage steps needed to support this feature.

## 4.3 Dynamic Voltage Scaling

Full processor and software system performance is obtained at the maximum run speed when operating at the highest voltage needed for that particular part and temperature.

During less demanding periods of nominal run speed, the required performance can be obtained at a slightly lower voltage, resulting in a significant power savings. During times when the software is idle, the processor can be stopped and the voltage can be lowered further since speed performance is not needed and only enough voltage to hold the state of registers is required. Some typical examples are: 0.9 V STOP, 1.2 V RUN nominal speed, 1.6 V RUN maximum speed.

The transition between two set points must be smooth and controlled. This is achieved on the MC13783 by having a DVS Range 0.9 V–1.70 V, which transitions in mini steps of 25 mV each in configurable time steps. This appears as a ramp from one voltage to the next. Figure 4 shows the ramp up and down of the voltage domain as a result of DVS.

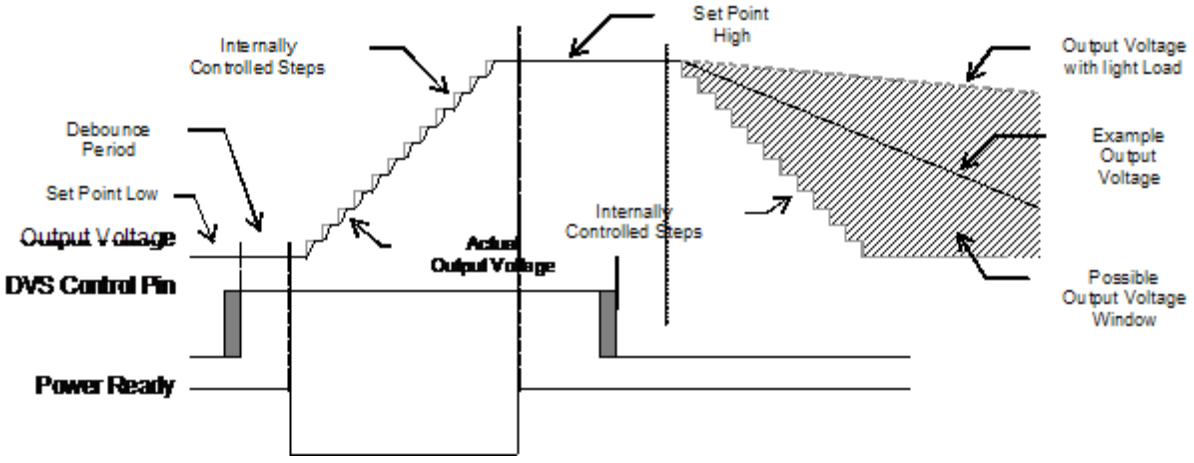



**Figure 4. Ramp Up and Down of the Voltage Domain as a Result of DVS**

The hardware inputs driven from the processor's General Purpose Output (GPO) or standby pins drive the PMIC to slew from one set point to the next. A “power ready” signal indicates a higher set point is established.

## 4.4 Power Gating

Power gating is a very aggressive technique to reduce the leakage current of disabled modules effectively to zero. The i.MX31 is divided into several power domains to provide maximum flexibility to apply power gating. The MC13783 has 4 DVS switching regulator power domains, and can supply as many as 15 other domains for specific needs, most of which are for powering peripheral devices and can be enabled or disabled independently. There are also 2 power gate drivers available to further split a given regulator to supply 2 domains at that same voltage that can be independently enabled or disabled. Figure 5 shows an example of power gating.

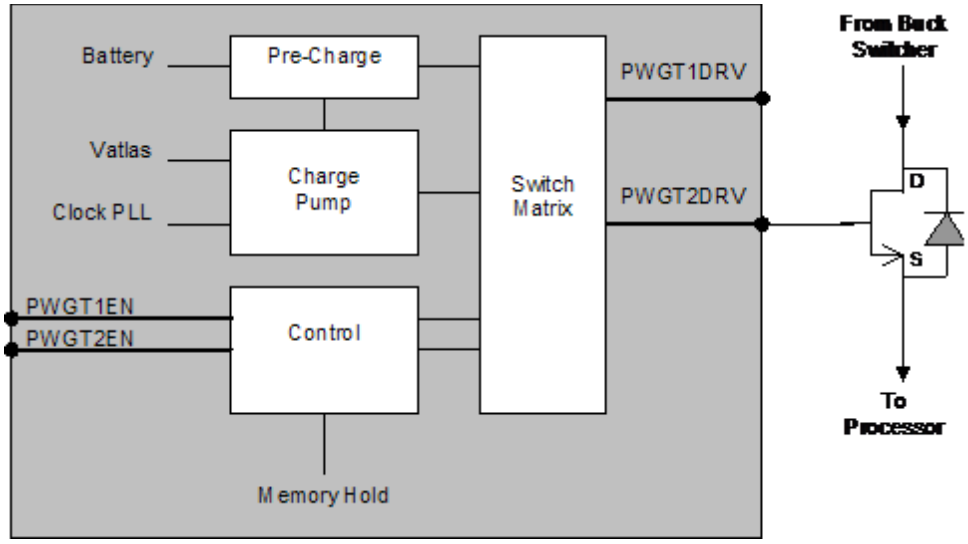



**Figure 5. Power Gating Example**

## 4.5 Analysis of Power Loss

The power loss in CMOS circuits consist of two main components:

- Pstatic = Gate oxide tunneling current, source drain sub-threshold conduction, P-N junction leakage. Features in the processor design, such as well biasing, as well as power gating by the PMIC reduce this loss.
- Pdynamic = Proportional to clock frequency, load capacitance and the square of the voltage. Features that involve both the processor and PMIC such as DVFS and DPTC reduce this loss.

Conclusions of power loss are:

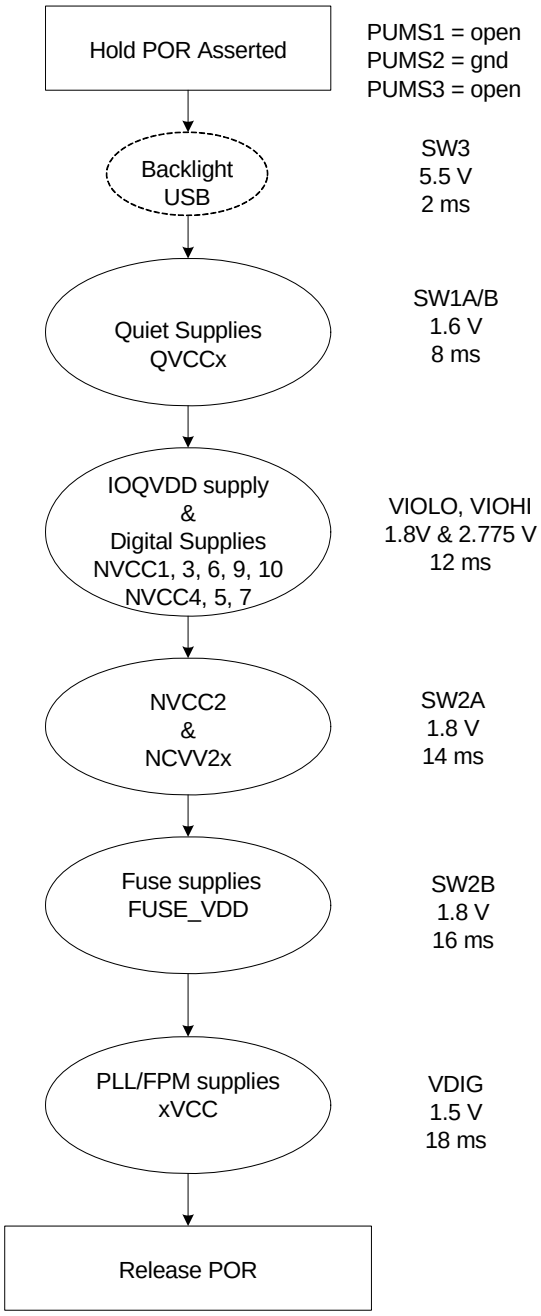
The relationship states that lowering any of the three values will reduce dynamic power. Load capacitance ($C_L$) is fixed for a given circuit and cannot be changed. Controlling the voltage and frequency dynamically will result in power saving.

## 4.6 Voltage Needs and Sequencing

The i.MX31 uses numerous power domains:

- 1.8 V or 2.775 V for interface (most of the NVCC domains).
- 0.9 V to 1.6 V for the core QVCC0-10 must always be powered. QVCC4x and QVCC1_x shall be powered at the same voltage, but can be gated on and off for power savings.
- 1.3 V to 1.6 V for the PLL domains (FVCC, MVCC, UVCC, SVCC).
- 1.8 V/3.15V for FUSE_VDD (normal/programming mode for i.MX31 versions 1.15 and 1.2 only, an additional off-chip adjustable supply can be provided or one of the existing MC13783 rails can be used at 1.8V); for rev 2.0 and higher, FUSE_VDD will not be powered for normal mode.

The NVCC domains can be powered by 1.8 V or 2.8 V depending on what they are connected to, so exact configuration will vary from product to product. In general, NVCC 1, 3, 6, 9 and 10 are tied to 1.8 V and NVCC4, 5, 7 are tied to 2.775 V. Figure 6 shows how the domains should be powered up by using this sequence.




**Note:** Applies to i.MX31 versions 1.15 and 1.2 only. For rev 2.0 and higher, FUSE_VDD will not be powered and that block on the flow chart can be disregarded. Alternately, FUSE_VDD can be powered from an off-chip 1.8/3.15V supply, freeing up SW2B for other uses.

**Figure 6. Voltage Sequencing**

Table 2 shows the power settings that need to be used.

**Table 2. Power Settings**

| Pins | Setting |
|---|---|
| PUMS1 | open |
| PUMS2 | gnd |
| PUMS3 | open |

Wiring information in Section 5.1, "Connecting the Power Domains", on page 12 describes how to achieve these power needs.

# 5 Interconnection

At its most basic level, a system block diagram is shown in Figure 7 presenting the interconnection of the i.MX31 and MC13783.

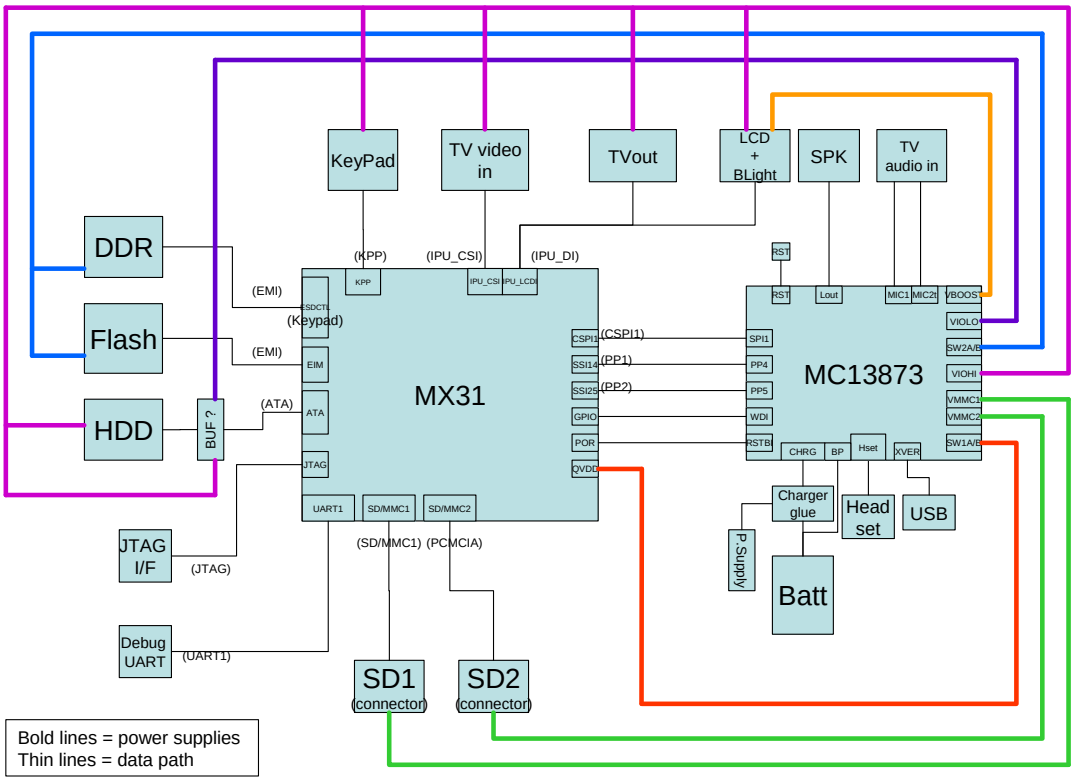



**Figure 7. Interconnection Block Diagram**

## 5.1 Connecting the Power Domains

### 5.1.1 Wiring the Power Lines

The i.MX31 actually has 66 power pins for the 18 voltage domains, many of these domains will be powered by the same source, some together and some isolated with a power gating FET switch.

Selection of power for these domains must be done in product design. For instance, if a particular domain powers a module with i.MX31 that interfaces with an off-chip circuit, that domain must be run on the same supply as the off-chip circuit (memory, sensor, interface IC, etc.). Some of these will run at 2.775 V, some at 1.8 V, and some at other voltages. The product designer must select the appropriate regulator on the MC13783 for that circuit and domain.

It is recommended that a 0.1 µF capacitor be tied to each supply domain as close to the i.MX31 as possible. Multiple capacitors may be needed for multiple pins for best filtering.

Table 3 shows one possible recommendation for interconnections between the MC13783 and i.MX31. In this case, the A and B of the first buck switcher, SW1, are tied together, SW1 (A and B combined) is used for the processor core and SW2 (A only) for memory. VDIG is used to power the PLLs on the i.MX31, VIOHI is used for 2.775 V domains and VIOLO for 1.8 V domains. There may be other configurations which mandate wiring differently, for instance to run a power domain from 1.8 V instead of 2.775 V, etc.

**Table 3. Interconnections Between the MC13783 and i.MX31**

| MC13783 Signal | i.MX31 Signal | Voltage Default | Turn on Time (ms) |
|---|---|---|---|
| SW1A&B (SW1AFB pin) | QVCC0 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC1 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC10 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC2 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC3 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC4 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC5 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC6 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC7 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC8 | 1.6 V | 8 |
| SW1A&B (SW1AFB pin) | QVCC9 | 1.6 V | 8 |
| VIOHI | NVCC40 | 2.775 V | 12 |
| VIOHI | NVCC41 | 2.775 V | 12 |
| VIOHI | NVCC50 | 2.775 V | 12 |
| VIOHI | NVCC51 | 2.775 V | 12 |
| VIOHI | NVCC52 | 2.775 V | 12 |

**Table 3. Interconnections Between the MC13783 and i.MX31 (continued)**

| MC13783 Signal | i.MX31 Signal | Voltage Default | Turn on Time (ms) |
|---|---|---|---|
| VIOHI | NVCC70 | 2.775 V | 12 |
| VIOHI | NVCC71 | 2.775 V | 12 |
| VIOHI | NVCC72 | 2.775 V | 12 |
| VIOHI | NVCC73 | 2.775 V | 12 |
| VIOLO | IOQVDD | 1.8 V | 12 |
| VIOLO | NVCC10 | 1.8 V | 12 |
| VIOLO | NVCC100 | 1.8 V | 12 |
| VIOLO | NVCC101 | 1.8 V | 12 |
| VIOLO | NVCC102 | 1.8 V | 12 |
| VIOLO | NVCC103 | 1.8 V | 12 |
| VIOLO | NVCC11 | 1.8 V | 12 |
| VIOLO | NVCC12 | 1.8 V | 12 |
| VIOLO | NVCC30 | 1.8 V | 12 |
| VIOLO | NVCC31 | 1.8 V | 12 |
| VIOLO | NVCC32 | 1.8 V | 12 |
| VIOLO | NVCC60 | 1.8 V | 12 |
| VIOLO | NVCC61 | 1.8 V | 12 |
| VIOLO | NVCC62 | 1.8 V | 12 |
| VIOLO | NVCC80 | 1.8 V | 12 |
| VIOLO | NVCC81 | 1.8 V | 12 |
| VIOLO | NVCC9 | 1.8 V | 12 |
| SW2A (SW2AFB pin) | NVCC20 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC21 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC210 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC211 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC212 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC22 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC220 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC221 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC222 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC223 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC224 | 1.8 V | 14 |

**Table 3. Interconnections Between the MC13783 and i.MX31 (continued)**

| MC13783 Signal | i.MX31 Signal | Voltage Default | Turn on Time (ms) |
|---|---|---|---|
| SW2A (SW2AFB pin) | NVCC225 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC226 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC227 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC228 | 1.8 V | 14 |
| SW2A (SW2AFB pin) | NVCC23 | 1.8 V | 14 |
| SW2B (SW2BFB pin) | FUSE_VDD [1] | 1.8 V | 16 |
| VDIG | FVCC | 1.5 V | 18 |
| VDIG | MVCC | 1.5 V | 18 |
| VDIG | SVCC | 1.5 V | 18 |
| VDIG | UVCC | 1.5 V | 18 |
| SW1A through FET1 | QVCC40 | 1.6 V | Command |
| SW1A through FET1 | QVCC41 | 1.6 V | Command |
| SW1A through FET1 | QVCC42 | 1.6 V | Command |
| SW1A through FET1 | QVCC43 | 1.6 V | Command |
| SW1A through FET2 | QVCC1_0 | 1.6 V | Command |
| SW1A through FET2 | QVCC1_1 | 1.6 V | Command |
| SW1A through FET2 | QVCC1_2 | 1.6 V | Command |
| SW1A through FET2 | QVCC1_3 | 1.6 V | Command |

[1] 1.8 V/3.15V for FUSE_VDD (normal/programming mode for i.MX31 versions 1.15 and 1.2 only, an additional off-chip adjustable supply can be provided or one of the existing MC13783 rails (SW2B shown in the table) can be used at 1.8V); for rev 2.0 and higher, FUSE_VDD will not be powered for normal mode.

To achieve these voltages and sequences, use the following settings: PUMS1 = open, PUMS2 = gnd, PUMS3 = open.

### 5.1.2 Wiring the Control Lines

Table 4 shows the control lines that are typically used. The use of these signals is discussed in more detail in Section 6, “Control and Other Considerations,” on page 17.

**Table 4. Control Lines**

| MC13783 Signal | i.MX31 Signal | Description |
|---|---|---|
| DVSSW1A | DVFS1 | DVS control |
| DVSSW1B | DVFS0 | On combined switchers, provides another step |
| DVSSW2A | Not used | Typically not needed on fixed voltage memory |

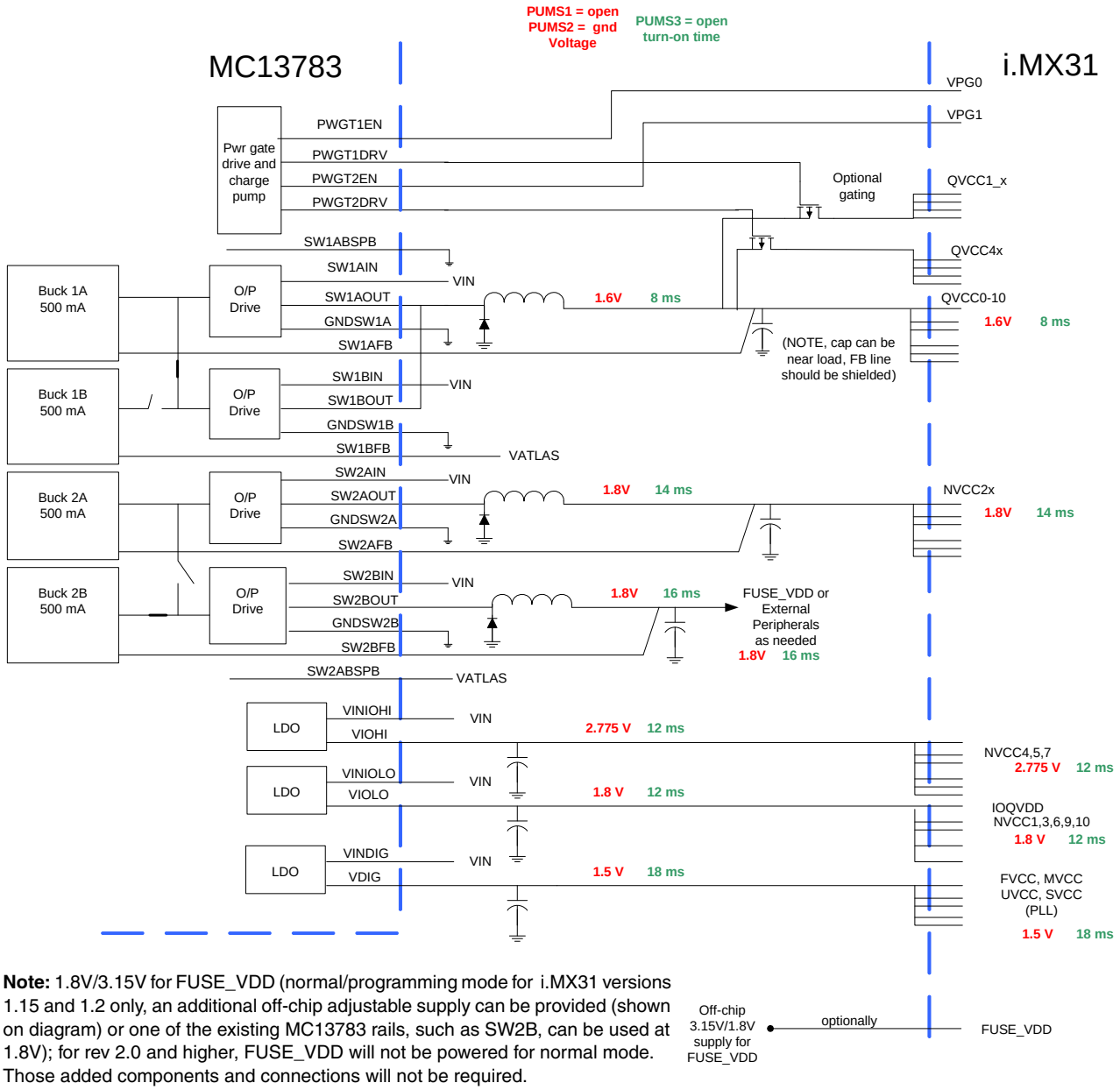
**Table 4. Control Lines (continued)**

| MC13783 Signal | i.MX31 Signal | Description |
|---|---|---|
| DVSSW2B | Not used | Not used on combined switchers |
| SW1BFB | N/A | Tie to VATLAS for combined switchers |
| SW1ABSPB | N/A | Tie to ground for combined switchers |
| SW2ABSPB | N/A | Tie to VATLAS for separated switchers |
| PRIVCC | N/A | Primary SPI - supply VIOHI |
| PRICS | CSP12_SS0 | Primary SPI |
| PRICLK | CSP12_SCLK | Primary SPI |
| PRIMOSI | CSP12_MOSI | Primary SPI |
| PRIMISO | CSP12_MISO | Primary SPI |
| SECVCC | Not used | Secondary SPI - supply |
| SECCS | Not used | Secondary SPI |
| SECCLK | Not used | Secondary SPI |
| SECMOSI | Not used | Secondary SPI |
| SECMISO | Not used | Secondary SPI |
| GNDSPI | gnd | gnd |
| SIMEN | GPIO if used | Regulator enable for SIM |
| ESIMEN | GPIO if used | Regulator enable for VESIM, VMMC1 and/or VMMC2 |
| VIBEN | GPIO if used | Regulator enable for VIB |
| REGEN | GPIO1_6 | Regulator enable for all, polarity selectable, might need level shift |
| STANDBYPRI | VSTBY | Standby (a low power state retention mode) |
| BATTDETB | GPIO | Battery/charger detect |
| PWRGT1EN | VPG0 | Enable for FET driver |
| PWRGT2EN | VPG1 | Enable for FET driver |
| CLK32K | Peripherals, if needed | 32 kHz peripheral clock |
| CLK32KMCU | CKIL | 32 kHz MCU clock |
| PWRREADY | GPIO1_5 | Power ready handshaking |
| RESETB | RESET_IN_B | Reset |
| RESETBMCU | POR_B | Reset |
| WDI | WD_RST | Watch dog, from proc to PMIC |
| SECINT | Not used | Secondary interrupt |
| ADTRIG | GPIO if used | ADC trigger |
| PWRFAIL | PWR_FAIL | Battery/power signal |
| LOBATB | GPIO if used | Battery/power signal |

Depending on the application, some control signals may not be used. Other application-specific signals are not shown as they are outside the scope of this application note, such as the USB interface and the audio interface.

### 5.1.3 Wiring Block Diagram

Figure 8 shows the partial wiring block diagram.




**Note:** 1.8V/3.15V for FUSE_VDD (normal/programming mode for i.MX31 versions 1.15 and 1.2 only, an additional off-chip adjustable supply can be provided (shown on diagram) or one of the existing MC13783 rails, such as SW2B, can be used at 1.8V); for rev 2.0 and higher, FUSE_VDD will not be powered for normal mode. Those added components and connections will not be required.

**Figure 8. Wiring Block Diagram**

# 6 Control and Other Considerations

## 6.1 Handshaking and Interactions

### 6.1.1 Turn-on Handshaking

When a turn-on event occurs (such as the “On” button being pressed), the MC13783 will begin to turn on, following the turn-on sequence set by the PUMS pins. When power is ready, the RESETB lines to the processor will go high during the watchdog state of 500 ms. During this time the processor must boot up and assert a high on the WDI pin. If it does not, the MC13783 will turn off again. With WDI high, at the end of the watchdog timer interval, the MC13783 will be turned on.

The sequence is as follows:

- Power on event occurs
- Power comes on in the sequence shown in Figure 6
- RESETB (MC13783 output) goes high
- Processor boots up
- Processor asserts a high on WDI (MC13783 input)
- WDI is high at 500 ms and the MC13783 stays on.

For more details and other modes, see the *MC13783 User Guide*.

### 6.1.2 DVS Handshaking

Each buck regulator, SW1A, SW1B, SW2A, and SW2B on the MC13783, can be configured for three different voltage settings. A specific voltage and mode in normal operation, in standby operation (STANDBY pin high) and DVS operation (DVSSWxy pin high), are all programmed via SPI. When the appropriate hardware pin is asserted, the output voltage will slew up (or droop down) to the new voltage at a speed set by the bits SWxyDVSSPEED[1:0].

- When the i.MX31 changes from slow speed (Frequency Scaling in DVFS) operation to high speed, it will drive the DVS pin (an input to the MC13783).
- PWRRDY will go low and the switcher on the MC13783 will slew from the programmed normal voltage to the programmed DVS voltage . Refer to Figure 9.
- When voltage reaches its final state, PWRRDY (an output pin from the MC13783) will go high.
- Upon PWRRDY going high, the i.MX31 core will speed up to full speed.
- (This example assumes the programmed DVS voltage to be higher than the nominal voltage.)

**NOTE**

The i.MX31 processor uses an internal counter (VSCNT)—not the PWRRDY signal—to wait until the MC13783 reaches the final state. The i.MX31 processor uses the PWRRDY signal during DPTC operations and when exiting from State Retention mode.

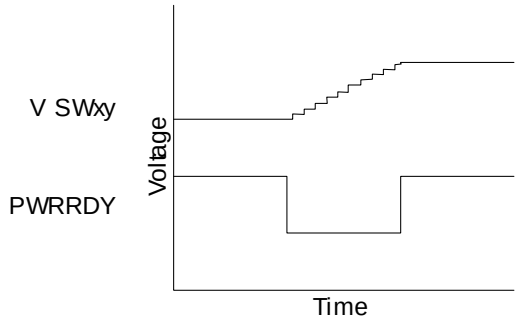



**Figure 9. Relationship of Switcher Voltage to PWRRDY Signal**

## 6.2 Hardwired Default Settings

The MC13783 provides a variety of pre-programmed turn-on sequence and voltage settings for the various regulators. In reviewing Table 5 and Table 6, a setting or sequence that is better suited to specific system needs may be used. Table 5 lists the default voltages selected by the pins PUMS1 and PUMS2 set to open and ground, respectively. (See the *MC13783 User Guide* for other options.)

**Table 5. Default Voltages for PUMS1 and PUMS2 Sample Setting**

| Pins | Default Voltages |
|---|---|
| PUMS2 | gnd |
| PUMS1 | open |
| SW1A (5) | 1.6 |
| SW1B (5) | 1.6 |
| SW2A (5) | 1.8 |
| SW2B (5) | 1.8 |
| VIOHI | 2.775 |
| VIOLO | 1.8 |
| VDIG | 1.5 |

Table 6 shows the default turn on sequence (the table lists millisecond delay after initialization of power up for each regulator) of the various regulators selected by PUMS3 set to open. (See the *MC13783 User's Guide* for other options.)

**Table 6. Default Turn On Sequence**

| PUMS3 | Open |
|---|---|
| SW1A (5) | 8 |
| SW1B (5) | 10 |
| SW2A (5) | 14 |
| SW2B (5) | 16 |
| VIOHI | 12 |
| VIOLO | 12 |
| VDIG | 18 |

For the wiring suggested in Section 5.1.1, “Wiring the Power Lines”, on page 12, use the following settings:

- PUMS1 = open
- PUMS2 = gnd
- PUMS3 = open

### 6.2.1 Combining the Buck Switching Regulators

If the switching regulators SW1A and SW1B are to be combined for added current sourcing capability (or likewise SW2A and SW2B), then the SW1ABSPB (or SW2ABSPB) pin is tied to ground and the unused feedback pin(s) SW1BFB (SW2BFB) should be tied to VATLAS. The SW1AIN and SW1BIN should be tied together as should SW1AOUT and SW1BOUT and GNDSW1A and GNDSW1B (same for the “SW2y” equivalent lines if that switcher is to also be paralleled). All commands will be made to SW1A (SW2A); any commands to either “B” switcher will be ignored.

When SW1 is used in single mode, the SW1ABSPB (P11) pin should be tied to VATLAS. When SW2 is used in single mode, the SW2ABSPB (R12) pin should be tied to VATLAS. In this case, both feedback pins are used.

## 6.3 SPI Programming

Refer to the *MC13783 User's Guide* for details on the SPI programming protocol and timing and levels for the SPI registers. Registers 24 through 33 apply to the power functions of the MC13783.

When turned on, some of the regulators will be enabled by default as set by the selected pre-programmed turn-on sequence and voltage setting of the various regulators.

**NOTE**

Do not use SPI to disable the regulator that powers the SPI, typically VIOHI tied to PRIVCC, otherwise the IC will lose SPI communication and that regulator cannot be re-enabled.

Programming of voltages for the various regulators should be performed when needed. During the turn-on sequence, the DVS and (if used) the standby voltages for the buck switching supplies should be programmed so that they are available when needed. Programming of the operate voltage during dynamic process temperature compensation will be performed on an as needed basis.

**WARNING**

Never disable the regulator that powers SPI (PRIVCC), to do so will prevent further SPI writes to the PMIC. This regulator can be controlled via a non-SPI means, such as standby or REGEN so long as the system implementation ensures a robust recovery.

## 6.4 Dealing with Unused Features

The MC13783 has numerous regulators and other functions, not all of which may be required for any given application.

### 6.4.1 Recommendations for Terminations Related to Unused Functions

Follow the guidelines below for dealing with unused functions.

- All ground pins, even those related to an unused block, should be grounded.
- VIOLO and VIOHI must have their inputs tied to B+ (battery or voltage supply), and the outputs must have a bypass capacitor to ground. VINVIB and VINCAM should also be tied to B+, but disabled. All other regulator inputs and outputs can be left “n/c” and should be disabled in the SPI. VATLAS and REFATLAS must have their bypass caps. VRF1, VRF2, VMMC1 and VMMC2 use an off-chip pass device. If that regulator is not required, do not install the pass device or the capacitor. For regulators that share an input pin, if one such regulator is used and another is not, ensure the unused regulator is disabled or has the bypass cap.
- For SW1A, SW1B, SW2A, and SW2B, SWxyIN should be tied to B+, SWxyFB to ground, and DVSSWxy can be “n/c”. The unused switching regulator should be disabled. SW3IN can be “n/c”, the other SW3 pins to ground.
- All PWRGTx and GPOx pins can be left “n/c” if not used.
- SPARE and RSRVD pins are left open (n/c).
- Except for SECMISO and SECINT which are left open, all secondary SPI pins should be tied to ground. PRI SPI must be operational.
- PUMS must be set as needed, and ICTEST and ICSCAN grounded, 32 kHz CLK pins left “n/c” if not used.
- WDI must be used; LICELL needs 100 nF cap. Other logic pins can be left open: ONxB, RESETx, STANDBYx, LOBATB, PWRRDY, MEMHLDDRV, CSOUT, and VBKUPx. PWRFAIL, USEROFF and CLK32KMCU are referenced to VBKUP1. Either VBKUP1 is enabled or another regulator should be tied to that pin to power those nodes.
- All USB/RS232 pins can be “n/c” except UMOD0 and 1 which should be tied as needed.
- All analog audio pins should be left open except for MC1RIN, MC1LIN, MC2IN and TXIN, which should be tied through a capacitor to ground.
- Audio bus pins TX1 and TX2 left “n/c”. The others: BCL1 and BCL2, FS1 and FS2, RX1 and RX2, CLIA and CLIB tied to ground.
- All ADC pins can be left “n/c”.
- All LEDx pins can be left “n/c”.
- The charger should be wired as described in the charger section of the *MC13783 User’s Guide*. If the charger is not to be used, CHRGRAW, CHRGCTRL, BPFET, BATTFET, CHRGSE1B, CHRGLED are all left open. CHRGISNSP, CHRGISNSN, BP, BATTISNS and BATT are all tied to the input power source (3.3 to 4.2V). CHRGMOD0 to ground, CHRGMOD1 to VATLAS. Put a 10uF cap on BP. Like all ground, GNDCHRG is grounded.

## 6.5 Power Dissipation and Maximum Ratings

The maximum ratings must not be exceeded and power dissipation, over temperature and input voltage, of the MC13783 IC must not be high enough to cause a junction temperature rise greater than 125°C. For every linear regulator in operation, the power dissipation should be calculated. The voltage drop, (the

maximum input voltage minus the output voltage) should be multiplied by the current drawn (average current can be used. Note, peak power lasting longer than a few tens of milliseconds can cause localized heating to occur). The power dissipated in all the regulators should be summed together. Additionally, the power dissipation of the on-chip devices of the switchers should be estimated (assume half the power lost in switcher inefficiencies to be dissipated on-chip). Power in the LED sinks and dissipated on-chip by the audio circuitry and should also be added to the power dissipation calculation.

The thermal resistance from junction to ambient when using a typical cell phone board is approximately 30 °C/W. This can be used to calculate expected temperature rise. There are built in temperature sensors that create two levels of warning interrupts before shutting down.

Absolute maximum ratings are:

- Charger input voltage: 20 V
- Battery voltage: 4.65 V
- Ambient operating temperature range: -30°C to 85°C
- ESD protection: 2.0 KV

Exceeding these ratings could damage the circuit.

Thermal protection typical values are:

- Warning lower threshold (TWL): 100°C
- Warning higher threshold (TWH): 120°C
- Protection threshold: 140°C

A voltage corresponding to the temperature sensor can be read via ADC.

# 7 Revision History

Table 7 summarizes revisions to this document since the release of the previous version (Rev. 0.1).

**Table 7. Revision History**

| Location | Revision |
|---|---|
| Section 4.6, “Voltage Needs and Sequencing” on page 9 | “FUSE_VDD needs 3.15V for programming” |
| Figure 6, Voltage Sequencing, on page 10 | Revised Note. |
| Table 3, Interconnections between the MC13783 and I.MX31, on page 14 | Revised Footnote |
| Table 4, Control Lines | Revised Descriptions for SW1BFB and SW2ABSPB |
| Figure 8, “Wiring Block Diagram,” on page 16 | Updated |
| Section 6.2.1, “Combining the Buck Switching Regulators” on page 19 | Revised text from ‘ground’ to ‘VATLAS’ (unused feedback pin(s)... should be tied to ‘VATLAS’). |
| Section 6.4.1, “Recommendations for Terminations Related to Unused Functions” on page 20 | Revised bullet item: ‘Except for SECMISO and SECINT...’ |
| Figure 8, “Wiring Block Diagram,” on page 16 | Updated |
| Throughout | Wording updated for clarity throughout |

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Document Number: AN3276
Rev. 0.3
01/2010