

Clock Options on the HC9S08 Family

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1 Introduction

This application note explains the various clock modules present on Freescale's S08 devices. Within the S08 family, it is possible to utilize an internal clock source (ICS), internal clock generator (ICG), and a multi-purpose clock generator (MCG). These modules can all have a clock source generated internally or externally (crystal oscillator) and fed through a frequency locked-loop (FLL) or phase locked loop (PLL) (MCG only) to boost the clock frequency. This application note also gives an analysis of the modules, details the various operating modes and describes the differences that exist between them. [Table 1](#) lists a few of Freescale's 8-bit products together with the clock source that they use.

Table 1. S08 Devices

Device	Clock Module
MC9S08DZxx	MCG
MC9S08AWxx	ICG
MC9S08QExx	ICS

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The three modules exist to serve the wide range of applications that Freescale devices are used within. The ICS can be thought of as a subset of the ICG and the MCG can be considered as an amalgamation of the ICS and ICG. The MCG clock module has been designed with high-end applications in mind whereas the opposite is true for the ICS that accommodates smaller, lower power, and cost sensitive HCS08 devices.

The clock operating modes are described in [Section 3, “Available Clock Modes”](#). The majority of these operating modes are common to all three of the clock modules, however, there are some operating modes unique to certain clock modules. [Table 2](#) outlines the operating modes and the corresponding modules.

Table 2. Summary of Available Clock Modes against Module

	MCG	ICG	ICS
FEI (FLL Engaged Internal)	•	•	•
FEE (FLL Engaged External)	•	•	•
FBI (FLL Bypassed Internal)	•	X	•
FBE (FLL Bypassed External)	•	•	•
BLPI (Bypassed Low Power Internal)	•	X	•
BLPE (Bypassed Low Power External)	•	X	•
PBE (PLL Bypassed External)	•	X	X
PEE (PLL Engaged External)	•	X	X
SCM (Self Clock Mode)	X	•	X

2 Eight-Bit Clock Modules

The following section provides technical descriptions on each of the three clock modules. Each module has been broken down into its sub-components for ease followed by a walk-through of the main registers programmed to operate each module.

2.1 Internal Clock Source (ICS)

The internal clock source (ICS) is a cost-effective module generally found on the smaller, lower cost range of MCUs in the HCS08 family. This application note describes V3 of the ICS module, which varies from earlier versions. The four main sub-modules that form the ICS are:

- FLL
- Clock select logic
- Internal reference clock
- External oscillator

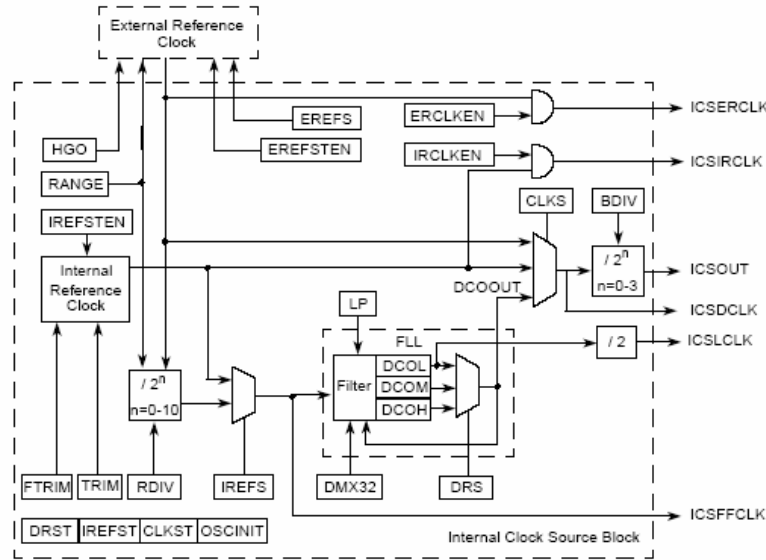


Figure 1. Internal Clock Source (ICS) Block Diagram (S08ICSV3)

The ICS outputs several different clock sources as shown in [Figure 1](#), which can be utilized as an alternative clock source by the integrated S08 modules and peripherals. [Table 3](#) lists the various functions the signals are used for. The main clock output signal, used for the CPU clock, is ICSOUT. The bus frequency is derived from ICSOUT divided by two. For further information on these clocks and the modules they serve, consult the specific S08 family data sheet.

Table 3. Available Clock Signals

Clock Signal	Function
ICSECLK	Optional ADC Clock
ICSIKCLK	RTI
ICSOUT	Main source/bus clock when divided by two
ICSDCLK	DCO Clock source
ICSLCLK	BDC
ICSFFCLK	timers

2.1.1 ICS FLL

The main purpose of the FLL is to provide a greater range of frequencies for the MCU to operate at. The FLL can take an input from an external or internal reference source, selected by the internal reference select (IREFS) as shown in [Figure 1](#). If an external reference clock is used, the signal must be divided into the range of 31.25 kHz – 39.0625 kHz by the reference divider bits (RDIV). This is explained in further detail in [Section 2.1.4, “ICS External Reference Clock”](#). The RDIV bits have no bearing if the internal reference clock is used.

The FLL contains multiplier values by way of the digital controlled oscillator (DCO) and is capable of providing low, middle, and high factors as listed in [Table 4](#). These values multiply the input signal resulting in an increased ICSOUT frequency.

It is also possible to utilize the DCO maximum frequency bit (DMX32) to narrow the reference range and maximize the FLL factor that has the effect of providing a single DCO output frequency. [Table 4](#) summarizes.

Table 4. DCO Frequency Range

Range Status	DRS bits	DMX32	Reference Range (kHz)	FLL Factor	DCO Range (MHz)
Low	00	0	31.25 – 39.0625	512	16 – 20
		1	32.768	608	19.92
Mid	01	0	31.25 – 39.0625	1024	32 – 40
		1	32.768	1216	39.85
High	10	0	31.25 – 39.0625	1536	48 – 60
		1	32.768	1824	59.77
Reserved	11	Reserved			

2.1.2 ICS Clock Select Logic

The clock select logic chooses whether an external, internal, or FLL generated clock source is used to generate ICSOUT via the clock select bits (CLKS). The chosen signal can then be divided by a factor of 1, 2, 4 or 8 via the clock divider circuit (BDIV), giving the user greater flexibility with bus speeds and crystal choice. As [Table 3](#) shows, the bus clock, used throughout the MCU, is derived by dividing ICSOUT by two.

2.1.3 ICS Internal Reference Clock

The internal reference clock (IRC) ranges from 25 kHz to 41.66 kHz (untrimmed) and can be trimmed by writing to the trim register (ICSTRM). By trimming the internal clock, you can target specific bus frequencies and provide a clock signal with higher accuracy. Writing a high value to this register provides a slower frequency, whereas writing a lower value has the opposite effect. For an even finer adjustment of the clock frequency, the ICSSC register contains a fine trim bit (FTRIM) that can be written to. The TRIM and FTRIM are not affected by resets.

As [Figure 1](#) illustrates, the internal reference clock can be used in conjunction with the FLL or it can be used directly as selected by the CLKS bits. The main advantages to using it through the FLL are the higher frequencies gained from the DCO factors. If the internal reference is used directly, it does not have the use of the DCO multiplier factors (see [Figure 1](#)). The internal reference is also responsible for the ICSIRCLK clock signal, which is produced via activating the internal reference clock enable bit (IRCLKEN). As the IRC is an independent clock source, it is possible to have ICSOUT running off the external clock while the IRC continues to generate ICSIRCLK.

2.1.4 ICS External Reference Clock

The external reference clock can be one of three external clock sources. It can be a low-frequency oscillator for use with a 32 kHz to 38.4 kHz crystal, a high frequency oscillator for use with

1 MHz to 16 MHz crystals or resonators, or a square wave input clock approximately between 0 – 50 MHz. If the square wave input clock is used, it should be connected to the EXTAL pin only, leaving XTAL free for use as a GPIO pin. Moreover, the external reference can be fed through the FLL by clearing the IREFS bit in ICSC1 register providing an alternative clock source. If the latter method is used, the frequency should be divided into the range specified in [Section 2.1.1, “ICS FLL”](#).

[Figure 1](#) shows that the HGO and RANGE bits from register ICSC2 have an impact upon the external reference clock. The high gain select (HGO) bit controls the external oscillator by allowing you to define whether the device should run with high gain or low power. Applications in noisy environments would benefit from the high gain facility because the higher amplitude clock signals provide greater noise immunity. The RANGE bit is similar because it allows crystals or resonators of low range (32 kHz – 38.4 kHz) or high range (1 MHz – 16 MHz) to be used as the external oscillator.

The capability to choose whether to operate with a brick oscillator or with an external crystal is undertaken by writing to the external reference select bit (EREFS). Similar to the internal clock, the ICSECLK is activated as a clock source by setting the ERCLKEN bit.

2.1.5 ICS Operation

This section provides a practical walkthrough guide on configuring the ICS. [Appendix A, “ICS Example Code,”](#) contains a coded example.

NOTE

These registers refer to V3 (S08ICSV3) of the ICS module. Differences exist with registers of other module versions.

2.1.5.1 ICS Control Register 2 (ICSC2)

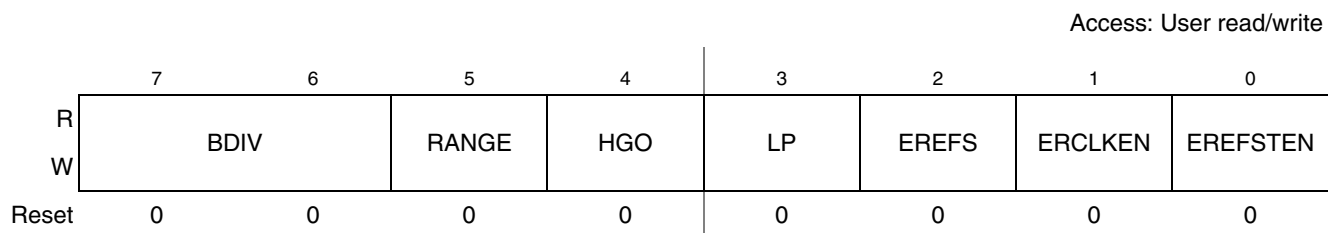


Figure 2. ICS Control Register 2

ICSC2 should be written before ICSC1 because it contains an option for choosing an oscillator or external crystal by setting/clearing the EREFS bit respectively. When the reference clock has been selected, run a check to make sure the reference clock has been initiated. This is carried out by the OSCINIT bit in the status and control register (ICSSC).

The HGO bit can provide high or low gain (low power); however, this is only relevant when using an external reference source. To minimize power consumption, the low-gain mode limits the voltage swing on the oscillator pins, whereas high-gain operation drives rail-to-rail voltage swing on the oscillator pins. The following frequency ranges are realizable from the combinations of HGO and RANGE:

Table 5. RANGE and HGO Settings with Resultant Frequency Range

RANGE	HGO	External Frequency Reference Range
0	—	32 – 38.4 kHz
1	0	1 – 8 MHz
1	1	1 – 16 MHz

Figure 1 shows the main output clock, ICSOUT, of the module passes through a bus divider block. As mentioned in Section 2.1.2, “ICS Clock Select Logic,” the BDIV bits are able to divide the clock source that ultimately forms the initial part of the bus clock. The bus clock is derived from a further divide of ICSOUT by two.

Where power consumption is an issue; it is possible to disable the FLL in the bypass modes (discussed in Section 3, “Available Clock Modes”) by setting the LP bit in ICSC2.

As touched upon in Section 2.1.4, “ICS External Reference Clock,” ICSC2 contains bits that determine whether the optional ICSECLK is active (ERCLKEN bit) or the external reference clock is disabled in STOP mode (EREFSTEN bit).

2.1.5.2 ICS Control Register 1 (ICSC1)

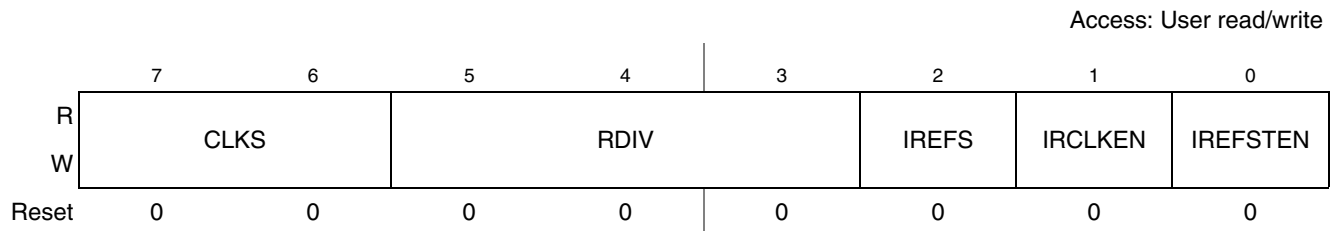


Figure 3. ICS Control Register 1

Within ICSC1 the IREFS bit determines whether the reference clock used is internal (set IREFS) or external (clear IREFS). Subsequently, the CLKS bits determine the clock source for the module shown in Table 6.

Table 6. ICS Clock Select Bits (CLKS)

CLKS	Clock Source
00	FLL Output
01	Internal reference
10	External reference
11	Reserved (defaults to 00)

The CLKST and IREFST bits of ICSSC should be read to determine that the correct clock source has been selected.

As mentioned in [Section 2.1.1, “ICS FLL,”](#) the RDIV bits divide an external reference into the range of 31.25 kHz – 39.0625 kHz. Within ICSC2, the RANGE bit also has a bearing on the divide factor as shown in [Table 8](#).

For example, using a 16 MHz crystal requires RANGE to be set and an RDIV of 512 to provide a reference frequency in the required range (in this case the reference frequency is 31.25 kHz).

Table 7. Reference Divide (RDIV) Factors

RDIV	RANGE=0	RANGE=1
0	1	32
1	2	64
2	4	128
3	8	256
4	16	512
5	32	1024
6	64	Reserved
7	128	Reserved

As discussed in [Section 2.1.3, “ICS Internal Reference Clock,”](#) ICSC1 contains bits that determine whether the optional ICSIRCLK is active (IRCLKEN bit) and whether the internal reference clock is disabled in STOP mode (IREFSTEN bit).

2.1.5.3 ICS Trim Register (ICSTRM)

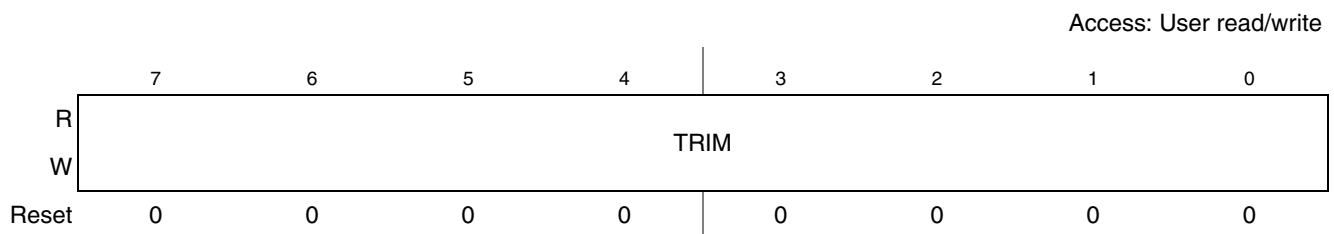


Figure 4. ICS Trim Register

The trim register (ICSTRM) controls the internal reference clock period (it has no affect upon an external reference), thus the clock frequency. Writing a high value to this register provides a slower frequency, whereas writing a lower value has the opposite effect. By default, the ICSTRM is set at 0x80.

To trim the clock, the flash location, 0xFFAE, should be used for storing FTRIM and 0xFFAF for storing the 8-bit trim value for ICSTRM register. The MCU does not automatically copy these values into these flash locations to their respective registers. Therefore, you must copy these values from flash to the registers.

2.1.5.4 ICS Status and Control Register (ICSSC)

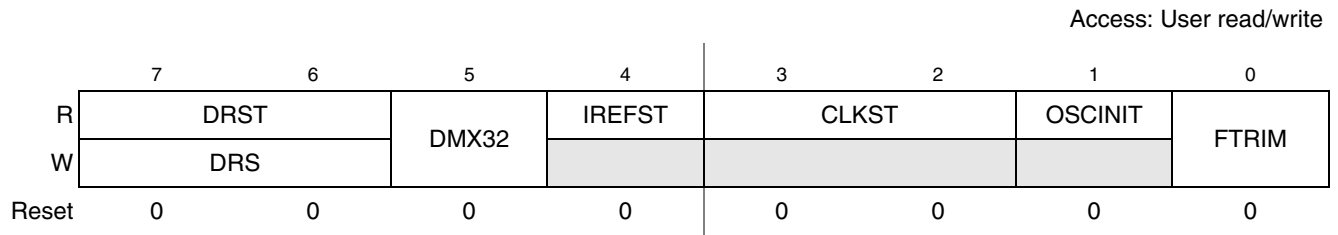


Figure 5. ICS Status and Control Register

The status and control register (ICSSC) contains the DCO range select bits (DRS) to select the frequency range of the FLL output. Reading the DRST bits returns the states. These bits should only be written if the LP bit in ICSC2 is cleared. [Table 4](#) provides a summary of the DCO ranges.

The register also contains the DCO maximum frequency bit (DMX32) that determines if a finely tuned reference frequency of 32.768 kHz is used. When using this reference, the DCO multipliers are greater when compared to general reference frequencies and this provides a fixed DCO output.

2.1.6 ICS Mode Selection

The operation modes are highlighted in [Table 2](#) with descriptions of each in [Section 3, “Available Clock Modes”](#). The ICS module has seven software selectable modes of operation. The selected mode determines factors such as clock accuracy and power consumption. Not discussed within [Section 3, “Available Clock Modes,”](#) is the off mode. The FLL is turned off to reduce power consumption. However, it is possible to maintain certain modules when in off mode, such as internal/external reference and RTI interrupt. To maintain the lowest power consumption reference, clocks should be disabled if not required.

[Figure 6](#) shows how to access the different modes available with the arrows dictating the allowed movements between modes. By default, the ICS is initially configured in FEI mode with BDIV set for dividing by two. The ICS is untrimmed and can operate in this state though accuracy is poor. For greater accuracy the IRC should be trimmed.

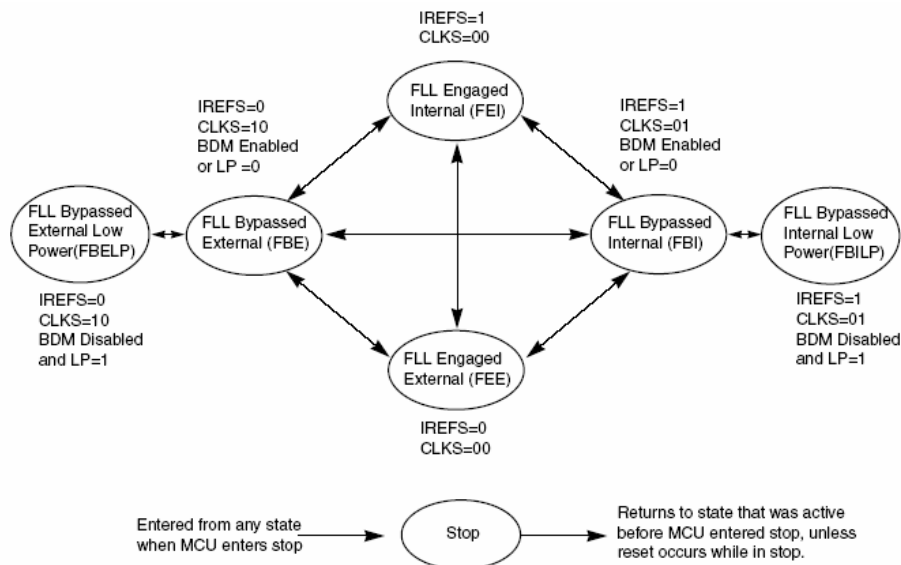


Figure 6. ICS Clock Switching Modes

Figure 6 shows the various steps in the clock switching modes. All but the low power modes can be accessed in one step when in default operation. If the newly selected mode is unavailable, the clock remains in the current mode. Example code on entering FEE mode from FEI is included in [Appendix A, “ICS Example Code”](#).

2.1.7 ICS System Protection

Being a less complicated subset of the ICG module, the ICS is primarily designed for lower power operation and has no features that allow for monitoring of loss of lock or loss of clock. The ICS contains a completely independent clock source for the COP watchdog timer that can reset the MCU if the CPU and bus clocks are corrupted.

In the event that a loss of clock was to occur, the software could no longer feed the COP watchdog and the MCU would reset.

In the event of a loss of lock, the ICS attempts to regain FLL on its own.

2.2 Internal Clock Generator (ICG)

The ICG module differs from the ICS as it does not contain any low power modes and has eight software selectable multiplier values.

The four main parts that constitute the ICG are:

- FLL
- Clock Select Logic
- Internal reference clock
- External oscillator

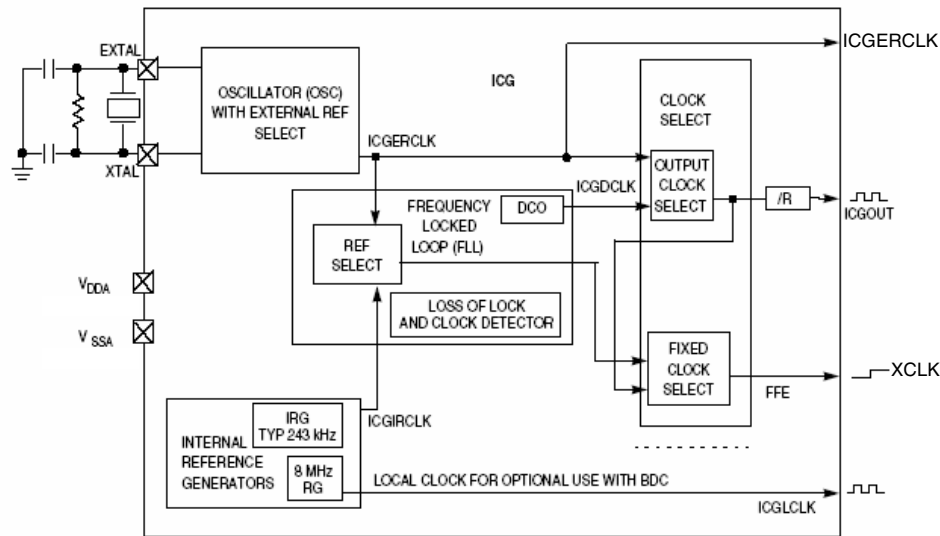


Figure 7. ICG Block Diagram

As shown in [Figure 7](#), the ICG contains four clock outputs that each has its own function as outlined in [Table 8](#). The main clock output is ICGOUT, which feeds the timers, communication buses and memory modules. The device bus clock is obtained from ICGOUT divided by two, which can provide bus rates up to 20 MHz. For further information on the clock outputs and the modules they serve, consult the specific S08 family data sheet.

Table 8. ICG Available Clock Signals

Clock Signal	Function
ICGERCLK	RTI
ICGOUT	Main Source/ bus clock (divided by two)
XCLK	Timers
ICGLCLK	BDC clock source

As multiple clock options are made available, greater flexibility is available across cost, precision, current draw, and performance.

2.2.1 ICG FLL

The main purpose of the FLL is to provide a greater range of frequencies for the MCU to operate at. The FLL can take an input from an external or internal reference source, selected by the internal reference select bit (REFS, control register 1).

The FLL contains multiplier values, by way of the digital controlled oscillator (DCO), that are capable of multiplying the input signal resulting in an overall greater bus frequency.

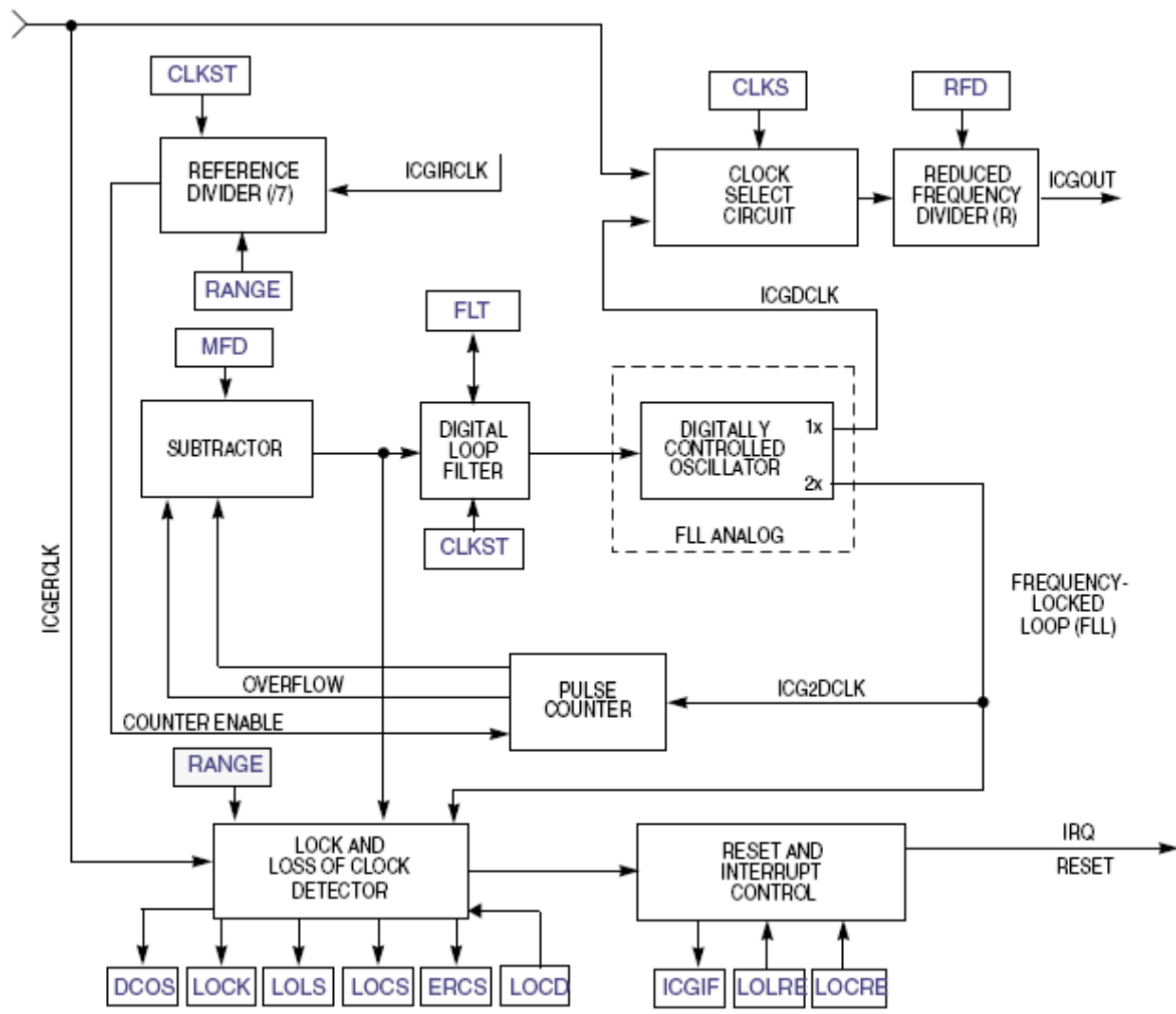


Figure 8. ICG FLL Block Diagram

2.2.2 ICG Clock Select Logic

This part provides several switch options for selecting different clock sources for the ICGOUT bus clock, as listed in [Table 8](#), to the system clock tree. The ability to choose a specific operating mode (see [Section 3](#), “Available Clock Modes”) as well as whether an internal or external reference clock is used is determined by the clock select bits (CLKS, control register 1). In contrast to the ICS, the ICG has a reduced frequency divider function (RFD, control register 2) with the ability to divide the ICGOUT by eight different factors (as shown in [Table 9](#)) that subsequently determines the main bus clock.

2.2.3 ICG Internal Reference Generator

The ICG contains two fixed-clock sources. The ICGLCLK is approximately 8 MHz and used exclusively with the BDC. The ICGIRCLK is typically 243 kHz \pm 25% and can be used as the FLL internal reference clock (IRC). [Figure 8](#) shows a reference divider of seven which is only applicable to the ICGIRCLK when the FLL is being utilized, i.e. FEI mode. This allows a wide range of system clock frequencies ranging from 34.47 kHz to 19.99 MHz derived from the internal reference.

The IRC can be trimmed for greater accuracy by writing to trim register (ICGTRM). By trimming IRC, you can target a specific bus frequency and provide a clock signal with greater accuracy. Increasing ICGTRM by one increases the oscillator period by 0.2%. Decreasing ICGTRM by one decreases the oscillator period by 0.2%. After trimming, the IRC remains within \pm 5% of the trimmed frequency across operating temperature and voltage. The main advantages to using the IRG or the IRC are that quick start-up times are realized (after being powered down), it requires no external components and lowers system costs, and this releases the XTAL and EXTAL pins for use as GPIO. Application notes AN2494 and AN2496 provide further details on configuring and trimming the ICG.

2.2.4 ICG External Reference Clock

The external oscillator block provides a means for connecting an external clock, crystal, or resonator. The main advantage of utilizing this is that external sources can provide a precise clock source, in comparison to internal clock sources.

The external reference clock can be one of three external clock sources. It can be a low frequency oscillator for use with a 32 kHz to 100 kHz crystal; a high frequency oscillator for use with 1 MHz to 16 MHz crystals or resonators, or a square wave input clock approximately between 0 – 40 MHz. If the square wave input clock is used, it should be connected to the EXTAL pin only, leaving XTAL free for use as a GPIO pin. To increase the choice of bus frequency, the external reference can be fed through the FLL circuit by selecting the appropriate CLKS bits and REFS configuration in ICGC1 and ICGC2 registers. The operational modes are discussed in [Section 3](#), “Available Clock Modes”. When using a mode that engages the FLL, multiplication and division factors can be applied to produce the bus frequency.

The HGO and RANGE bits from register ICGC1 have an impact upon the external reference clock. The high gain select (HGO) bit controls the external oscillator by allowing you to define whether the device should run with high gain or low power. Applications in noisy environments would benefit from the high gain facility because the higher amplitude clock signals provide greater noise immunity. The RANGE bit is similar in that it allows crystals or resonators of low range (32 – 100 kHz) or high range (1 MHz – 16 MHz) to be used as the external oscillator.

2.2.5 ICG Operation

As shown and discussed in [Section 3, “Available Clock Modes,”](#) the module has five modes of operation that utilize an internal or external clock source. The source used decides whether the module runs with high clock accuracy or consumes less power.

This section provides a practical walkthrough guide on configuring the ICG. [Appendix B, “ICG Example Code,”](#) contains a coded example.

NOTE

These registers refer to V4 (S08ICGV4) of the ICG module. Differences may exist with registers of other module versions.

2.2.5.1 ICG Control Register 2

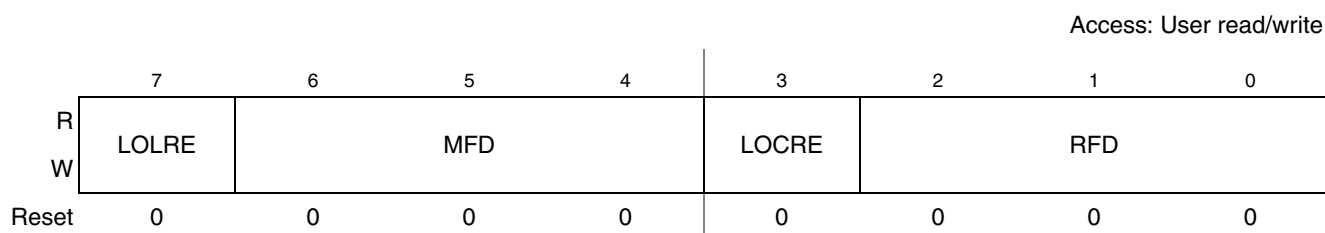


Figure 9. ICG Control Register 2

When working with the ICG, control register 2 (ICGC2) should be written first because this register sets the multiplier value before the FLL is enabled.

The multiplication factor (MFD) bits form part of the FLL circuit and this allows the reference frequency to be multiplied by values shown in [Table 9](#). Take care to avoid exceeding the DCO clock range (8 – 40) when choosing values for MFD and RFD. Although the combination may result in an ICGOUT frequency within the DCO range, the DCO output may be in excess of its own limits. The reduced frequency divider stage is after the DCO stage. Therefore, consideration should be given to the MFD bits to ensure DCO output remains within its permitted range.

ICGC2 also contains the reduced frequency divider bits (RDIV) as part of the clock select logic, which subsequently determines the main clock ICGOUT and therefore the module bus clock frequency.

Table 9. ICG Multiplication and Division Factors

MFD/RDIV bit states	MFD Factor	RDIV Factor
000	4	1
001	6	2
010	8	4
011	10	8

Table 9. ICG Multiplication and Division Factors (continued)

MFD/RDIV bit states	MFD Factor	RDIV Factor
100	12	16
101	14	32
110	16	64
111	18	128

If the application calls for lower power consumption and minimum jitter, the MFD and RFD bits should be chosen as small as possible.

As described further in [Section 2.2.6, “ICG Mode Selection,”](#) the ICG has a form of clock protection as reset/interrupt requests can be set by the loss of lock reset enable (LOLRE) and loss of clock reset enable (LOCRES) bits.

2.2.5.2 ICG Control Register 1

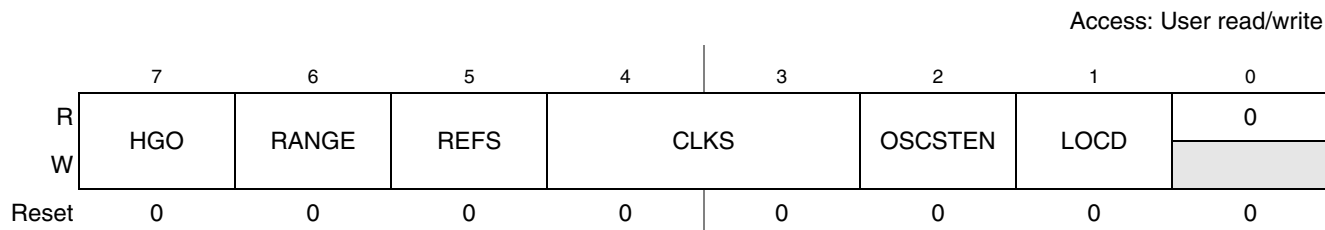


Figure 10. ICG Control Register 1

The clock mode select (CLKS) bits define if the clock module utilizes an internal or external reference as summarized in [Table 10](#).

Table 10. ICG Clock Select Bits (CLKS)

CLKS	Clock Mode ¹
00	Self Clock Mode (SCM)
01	Internal reference (via FLL) – FEI
10	External reference (direct) – FBE
11	External reference (via FLL) – FEE

¹ The full definitions of the operating modes are discussed in [Section 3, “Available Clock Modes”](#).

If the first write after a reset to CLKS is 0X (SCM or internal modes), the CLKS cannot be written to 1X (external modes) after the next reset because EXTAL pin was not reserved.

To enable high gain operation (useful in noisy environment applications), the HGO bit should be set. However, if lower power consumption is important to the application, this bit should be left cleared.

The frequency range select (RANGE) bit of the register is only considered if the reference clock is external. When configured in low-frequency range (< 100 kHz), this sets the FLL prescale factor to 64. In

high-frequency range (< 10 MHz), the prescale factor is set equal to 1. The prescale factor is important in determining the overall ICGOUT frequency.

Table 11. ICGOUT Frequency Calculation Options

Clock Scheme	f_{ICGOUT}^1	P
SCM — self-clocked mode (FLL bypassed internal) ²	$f_{ICGDCLK}/R$	—
FBE — FLL bypassed external	f_{ext}/R	—
FEI — FLL engaged internal ³	$\frac{f_{irg}}{7} \times \left(64 \times \frac{N}{R}\right)$	64
FEE — FLL engaged external	$f_{ext} \times \left(P \times \frac{N}{R}\right)$	Range = 0; P = 64 Range = 1; P = 1

¹ Ensure that $f_{ICGDCLK}$, which is equal to $f_{ICGOUT} \times R$, does not exceed $f_{ICGDCLKmax}$.

² Typically, $f_{ICGOUT} = 8$ MHz immediately after reset.

³ Typically, $f_{IRG} = 243$ kHz.

The external reference select (REFS) bit is utilized to select an oscillator/crystal (set bit) or an external clock (clear bit) as the reference clock source for ICGERCLK. Take care when writing to the RANGE and REFS bits because they are write-once after a reset. Table 14 shows the realizable frequency ranges dependant upon the state of REFS.

Table 12. External Frequency Ranges Allowable When Using an Oscillator Crystal/Resonator

		Allowable Frequency Ranges		
REFS = 1	CLKS	RANGE and HGO = 1 (MHz)	RANGE = 1, HGO = 0 (MHz)	RANGE = 0 (kHz)
	10	1 – 16	1 – 8	32 – 100
	11	2 – 10	2 – 8	32 – 100

The frequency range is greater when a direct frequency source is used (REFS=0), using frequencies up to 40 MHz.

This register also has the capability to control whether or not the oscillator circuit remains active in STOP mode by setting the OSCSTEN (oscillator enable in stop mode) bit. This provides an advantage as long as oscillator startup times can be avoided when recovering from STOP mode. However, it causes higher current consumption in stop mode. This bit has no effect when HGO=RANGE=1.

2.2.5.3 ICG Status Register 1 (ICGS1)

Access: User read/write

	7	6	5	4	3	2	1	0
R	CLKST		REFST	LOLS	LOCK	LOCS	ERCS	ICGIF
W								
Reset	0	0	0	0	0	0	0	1

Figure 11. ICG Status Register 1

ICGS1 is predominately read only with one read/write bit, the ICG interrupt flag (ICGIF). Writing a 1 to this bit clears the interrupt flag. The register also provides status on the security, as discussed in [Section 2.2.6, “ICG Mode Selection,”](#) as well as status information on the clock, such as what clock mode is being used (CLKST), whether the reference is internal or external (REFST), and indication of the external reference clock stability (ERCS).

2.2.5.4 ICG Status Register 2 (ICGS2)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	DCOS
W								
Reset	0	0	0	0	0	0	0	0

Figure 12. ICG Status Register 2

ICGS2 bit 0 is read only and provides an indication on whether the DCO clock is stable or not.

2.2.5.5 ICG Filter Registers (ICGFLTU, ICGFLTL)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	FLT			
W								
Reset	0	0	0	0	0	0	0	0

Figure 13. ICGFLTU Register

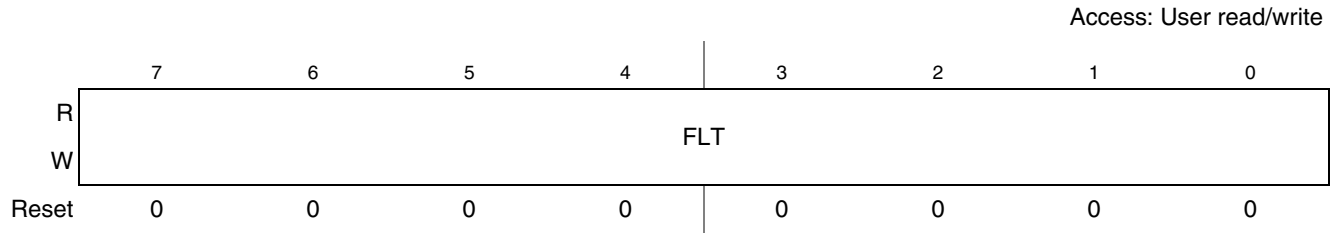


Figure 14. ICGFLT Register

The ICG includes two filter registers (ICGFLT and ICGFLTU) that can only be written when the module is programmed to operate in self-clock mode. The FLT bits indicate the current filter value, which controls the DCO frequency.

2.2.5.6 ICG Trim Register (ICGTRM)

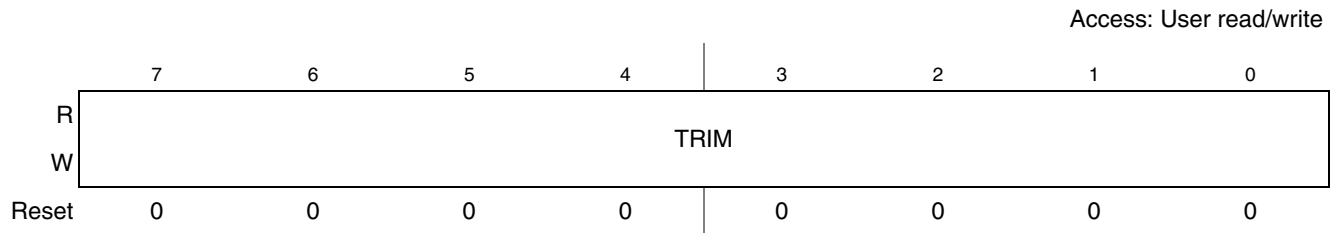


Figure 15. ICG Trim Register

As before, a trim register (ICGTRM) is included that allows a $\pm 25\%$ adjustment of the nominal period of the internal reference only. The untrimmed frequency range is approximately 182.25 – 303.75 kHz. The typical internal reference is 243 kHz.

By utilizing this register, the operating frequency can be accurately selected and fine tuned.

2.2.6 ICG Mode Selection

The ICG allows for flexibility on different configurations dependant upon the application such as whether lowest power consumption, accurate clock, or lowest cost are the major considering factors. [Table 13](#) summarizes the operating modes of the ICG and mentions typical characteristics expected in these modes. These operating modes are discussed further in [Section 3, “Available Clock Modes”](#).

Table 13. ICG Configuration Considerations

	Internal Clock	External Clock
FLL Engaged	FEI 4 MHz < fbus < 20 MHz Medium Power (less than FEE if oscillator range = high) Good clock accuracy Lowest system cost IRG is on. DCO is on ¹	FEE 4 MHz < fbus < 20 MHz Medium Power (less than FEE if oscillator range = low) High clock accuracy Medium/high system cost IRG is off. DCO is on
FLL Bypassed	SCM 3 MHz < fbus < 5 MHz (default) 3 MHz < fbus < 20 MHz (via filter bits) Medium power Least accurate IRG is off. DCO is on and open loop	FBE fbus range ≤ 8 MHz when crystal resonator is used. Lowest power Medium/high system cost IRG is off. DCO is off

¹ The IRG typically consumes 100µA. The FLL and DCO typically consumes 0.5 to 2.5mA, depending upon output frequency. For minimum power consumption and jitter, multiplication and division factors should be as small as possible.

Table 13 shows the differences that separate each mode. Lower system cost is achieved by utilizing the internal clock and not having to spend on external components. However, this reduces clock accuracy. The opposite occurs for devices with external clock components.

FEI produces the lowest system cost, FBE provides the lowest power consumption, and FEE mode demonstrates a highly accurate clock. The SCM mode is mainly used for quick and reliable system start-up. Two coded examples of using the ICG are given in [Appendix B, “ICG Example Code”](#).

2.2.7 ICG System Protection

Similar to the MCG module, the ICG contains fail-safe measures for loss of lock and loss of clock.

The lock status of the FLL is in ICG status register 1 (ICGS1), which indicates whether the FLL has acquired lock. Lock is acquired when the FLL output is within ±1.5 % of its target frequency. Lock is lost if the FLL output exceeds ±3 % of its target frequency.

When loss of lock occurs, the status (LOLS) bit in ICGS1 is set and remains set until cleared by software or until the MCU has been reset.

An interrupt or reset can be generated by using the loss of lock reset enable (LOLRE) bit in ICG control register 2 (ICGC2). The LOLS bit should also be cleared by reading ICGS1 and then writing 1 to ICGIF.

The ICG module also contains a clock monitor system that monitors the DCO, via the DCO clock stable bit (DCOS) in ICGS2, as well as the external reference clock, via the external reference clock status bit (ERCS) in ICGS1, for loss of clock events. Through this monitoring system, the module allows for automatic clock switching to a bypassed mode or to an internal clock reference upon loss of clock.

Table 14 shows the results of mode switching upon loss of clock.

Table 14. Mode Switching During Loss of Clock

Current Mode	Loss of DCO	Loss of External Clock
SCM	N/A	N/A
FBE	N/A	SCM
FEE	FBE	SCM
FEI	SCM	N/A

In each case, the CLKST and CLKS bits automatically change to reflect the new states.

Similar to the loss of lock, an interrupt or reset can be generated in the event of loss of clock by enabling loss of clock enable (LOCRE) bit in ICGC2. At this point, the loss of clock status (LOCS) bit in ICGS1 should also be cleared.

When in FEE or FEI mode and a loss of clock event occurs, this triggers a loss of lock. Because the method of clearing the LOCS and LOLS bits are the same, this is only an issue in the unlikely case that LOLRE is set and LOCRE is reserved. In this case, the interrupt would be overridden by the reset for the loss of clock.

2.3 Multi-Purpose Clock Generator (MCG)

The MCG module provides several clock sources for the MCU because it contains a phase-locked loop (PLL), frequency locked loop (FLL), and internal oscillator. The internal reference clock is served by nine trim bits for greater accuracy. The FLL can use an internal or external clock reference. The internal reference clock is 32 kHz with 0.2% resolution and a 2% deviation over voltage and temperature when trimmed. The PLL is used with the external reference only and consists of a voltage controlled oscillator (VCO), a modulo VCO frequency divider, phase/frequency detector, integrated loop filter, and a lock detector with interrupt capabilities.

Regardless of its source, the clock signal is passed through a bus frequency divider (BDIV) that can scale down the clock by 1, 2 (default), 4, or 8, depending upon the state of bits 6 and 7 of the MCG control register 2 (MCGC2).

Figure 5 shows the main sub-modules of the MCG as:

- FLL
- PLL
- Clock Select Logic
- Internal reference clock
- External Oscillator

The MCG has many similarities with the ICS module, with exceptions being the PLL circuit in the MCG.

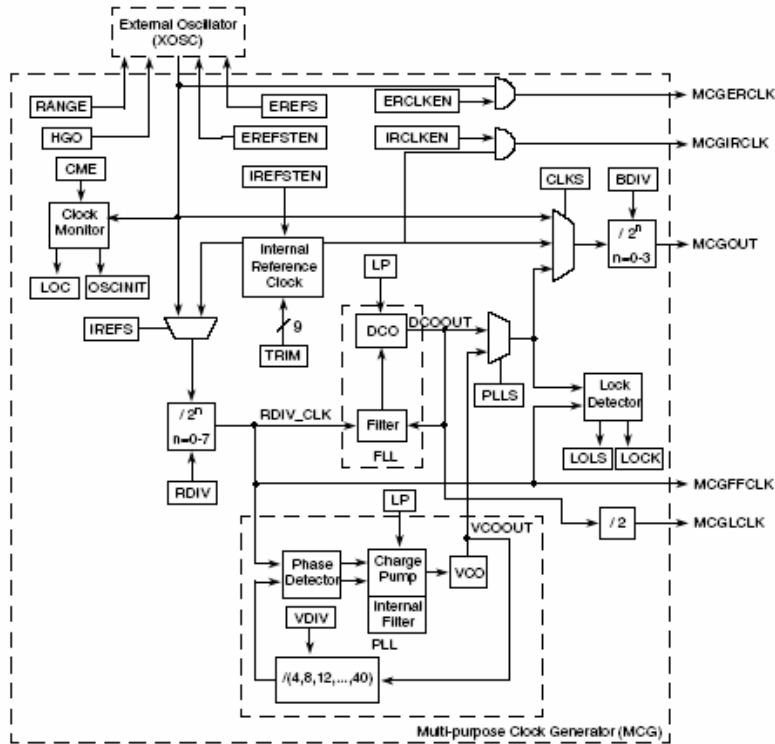


Figure 16. MCG Block Diagram

Table 15 lists the various functions the module output signals are used for. MCGOUT is the main clock output signal used for the CPU clock. The bus frequency is derived from MCGOUT divided by two. For further information on these clocks and the modules they serve, consult the specific S08 family data sheet.

Table 15. MCG Available Clock Sources

Clock Signal	Function
MCGERCLK	Optional ADC Clock
MCGIRCLK	RTI
MCGOUT	Main source/bus clock when divided by two
MCGFFCLK	DCO Clock source
MCGLCLK	BDC

2.3.1 MCG FLL

The main purpose of the FLL is to provide a wider range of frequencies for the MCU to operate. The FLL can take an input from an external or internal reference source, selected by the internal reference select (IREFS) as shown in Figure 16. If an external reference clock is used, the signal must be divided into the range of 31.25 – 39.0625 kHz by the reference divider bits (RDIV). The RDIV bits have no bearing if the internal reference clock is used.

The DCO of the FLL contains a fixed multiplier value of 1024.

2.3.2 MCG PLL

The FLL and PLL provide similar functions within this module, whereby the FLL locks frequency and the PLL locks phase. The PLL circuit is able to provide a clock source with a higher degree of stability and reliability. The PLL select bit (PLLS) in MCGC3 determines whether the FLL or PLL shall be used. The PLL cannot be used with an internal reference. When the external reference clock is used, the signal must be divided into the range of 1 – 2 MHz via the RDIV bits from MCGC1.

The PLL has several stages the input clock signal must go through as shown in [Figure 17](#).

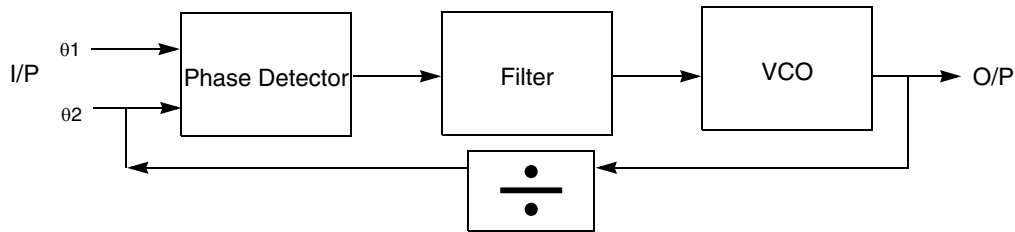


Figure 17. Basic Block Diagram of PLL Operation

The purpose of the PLL is to maintain a frequency signal by constantly comparing the phases of the input signal with the phases of the output signal and adjusting any differences. In basic terms, the PLL includes a phase detector, low-pass filter, and voltage control oscillator (VCO). The phase detector compares the phases of the two input values and provides an output proportional to the phase difference. The low-pass filter suppresses high frequency components in the phase detector output and produces a DC-controlled voltage for the VCO input. The VCO produces an output frequency proportional to its input voltage. The last stage provides negative feedback via a divider block to the input to begin the process again.

Bypassing the PLL (or FLL) stages and using the internal/external reference clock directly utilizes less power. However, this causes a reduction in the available bus frequencies.

2.3.3 MCG Clock Select Logic

The clock select logic chooses whether an external, internal, PLL, or FLL derived clock source is used to generate MCGOUT. The chosen signal can then be divided down by a factor of 1, 2, 4, or 8 via the clock divider circuit (BDIV), providing greater flexibility with bus speeds and crystal choice. As [Table 15](#) shows, the bus clock, used throughout the MCU, is derived by dividing MCGOUT by two.

2.3.4 MCG Internal Reference Clock

The internal reference clock (IRC) ranges from 25 – 41.66 kHz (untrimmed). The internal reference clock can be used with the FLL or directly as selected by the CLKS bits. The main advantages to using it via the FLL is a wider available range of bus frequency. If the internal reference is used directly, it does not have the use of the DCO multiplier value. The internal reference is also responsible for the MCGIRCLK clock signal, which is produced via activating the internal reference clock enable bit (IRCLKEN). Because the IRC is an independent clock source, the MCGOUT can run off the external clock while the IRC continues to generate MCGIRCLK.

To increase the accuracy of the internal clock signal, it is recommended to facilitate the available trimming feature, which would mean writing to the trim register (MCGTRM). Writing a high value to this register provides a slower frequency, whereas writing a lower value has the opposite effect. For an even finer adjustment of the clock frequency, the MCGSC register contains a fine trim bit (FTRIM) that can be written to.

2.3.5 MCG External Oscillator

The external reference clock can be one of three external clock sources. It can be a low-frequency oscillator for use with a 32 – 38.4 kHz crystal, a high frequency oscillator for use with 1 MHz to 16 MHz crystals or resonators, and a square wave input clock between 0 – 40 MHz. If the square wave input clock is used, it should be connected to the EXTAL pin only, leaving XTAL free for use as a GPIO pin. Moreover, the external reference clock can be fed through the FLL or PLL by clearing the IREFS bit in MCGC1 register. When using the FLL or PLL the external reference clock frequency should be divided into the range of 31.25 – 39.0625 kHz for the FLL and between 1 – 2 MHz for the PLL by the RDIV bits.

The HGO and RANGE bits from register MCGC2 have an impact upon the external reference clock. The high gain select (HGO) bit controls the external oscillator by allowing you to define whether the device should run with high gain or low power. Applications in noisy environments benefit from high gain facility because the higher amplitude clock signals provide greater noise immunity. The RANGE bit is similar in that it allows crystals or resonators of low range (32 kHz – 38.4 kHz) or high range (1 – 16 MHz) to be used as the external oscillator.

Choose to operate with a square wave input clock or an external crystal by writing to the external reference select bit (EREFS). Similar to the internal reference clock, the MCGERCLK is activated as a clock source by setting the ERCLKEN bit.

2.3.6 MCG Operation

It is possible to operate this module in eight different operating modes (discussed in [Section 3, “Available Clock Modes”](#)) that can be switched at any time during the application. This module can also provide the broadest functionality because the clock can be generated with an FLL, PLL, internal reference clock, or external reference clock. This makes the MCG suitable for different applications that have various demands in terms of performance and power consumption. A PLL circuit provides designers with high clock accuracy, whereas an internal reference clock has the potential for greatest cost savings.

NOTE

These registers refer to V1 (S08MCGV1) of the MCG module. Differences may exist with registers of other module versions.

2.3.6.1 MCG Control Register 2 (MCGC2)

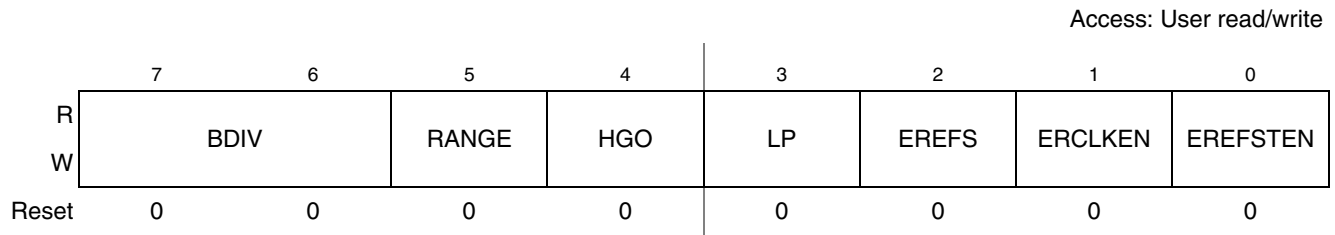


Figure 18. MCG Control Register 2

There are several bits within the control registers fundamental to operating the MCG. When using the MCG with an external reference clock, MCGC2 should be set before MCGC1 because EREFS of MCGC2 decides whether a crystal or square wave input clock drives the module. When the clock source has been selected, run a check to make sure the clock source has been initiated. This is carried out by checking the status of the OSCINIT bit in the status and control register (MCGSC).

Because the MCG uses a varied range of external reference clock frequencies, the RANGE bit of MCGC2 should be set according to [Table 16](#).

When using the internal reference clock, the RANGE bit should always be cleared.

Table 16. Frequency Range for External Oscillator and External Clock Source

Range	External Oscillator	External Clock Source
0	32 – 38.4 kHz	32 kHz – 1 MHz
1	1 – 16 MHz	1 – 40 MHz

Only influencing the external reference source, the HGO bit can provide high gain or low power. To minimize power consumption, the low-power mode limits the voltage swing on the oscillator pins, whereas high gain operation drives rail-to-rail voltage swing on the oscillator pins, which is suitable for use in noisy environments. The combination of HGO and RANGE affect the allowable frequency values of an external oscillator as shown in [Table 17](#).

Table 17. MCG RANGE and HGO Settings with Resultant External Oscillator Frequency Range

RANGE	HGO	External Frequency Oscillator Range ¹
0	0	32 – 38.4 kHz
1	—	1 – 5 MHz ²
1	0	1 – 8 MHz ³
1	1	1 – 16 MHz ³

¹ Obtained when EREFS and ERCLKEN are set.

² FEE or FBE modes only.

³ In BLPE mode only.

As [Figure 16](#) shows, the main output clock, MCGOUT, passes through a bus divider block. As mentioned in [Section 2.3.3, “MCG Clock Select Logic,”](#) the BDIV divides the clock source, therefore, allowing the

module to operate at lower frequencies. The bus clock is derived from a further divide of MCGOUT by two.

Where there are demands to reduce the power consumption of the application, the FLL and PLL can be disabled by setting the LP bit in MCGC2 when the MCG is utilizing one of the bypass modes (as discussed in Section 3, “Available Clock Modes”).

As Table 16 shows, the MCGERCLK clock source can be activated by the ERCLKEN bit of MCGC2. If necessary for the application, it is possible to have this clock source operational at the same time as the main clock source MCGOUT.

Finally, the EREFSTEN bit determines whether the external reference clock is disabled in STOP mode. Lower power consumption in STOP mode can be achieved by this action. STOP mode operations are outside the scope of this application note. For further details on this topic, see the appropriate datasheets.

2.3.6.2 MCG Control Register 1

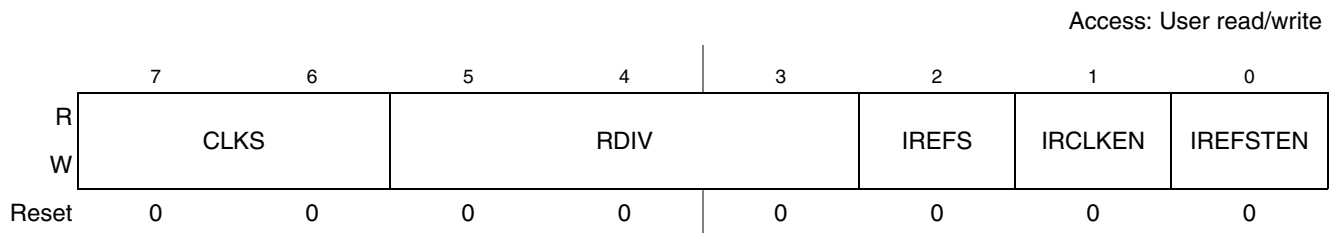


Figure 19. MCG Control Register 1

Within MCGC1, the IREFS bit determines whether the reference clock used is internal (set IREFS) or external (clear IREFS).

The CLKS bits determine the clock source for the module.

Table 18. MCG Clock Select Bits (CLKS)

CLKS	Clock Source
00	FLL or PLL Output
01	Internal reference
10	External reference
11	Reserved (defaults to 00)

The CLKST and IREFST bits of MCGSC should be read to determine that the correct clock source and reference clock has been selected as shown in the code example in Appendix C, “MCG Example Code”.

As mentioned in Section 2.3.1, “MCG FLL,” the RDIV bits divide an external reference into the range of 31.25 – 39.0625 kHz for the FLL and into 1 – 2 MHz for the PLL.

As Table 16 shows, the MCGIRCLK clock source can be activated by the IRCLKEN bit of MCGC1. If necessary for the application, it is possible to have this clock source operational at the same time as the main clock source MCGOUT.

Finally, the IREFSTEN bit determines whether the internal reference clock is disabled in STOP mode. Lower power consumption in STOP mode can be achieved by this action. STOP mode operations are outside the scope of this application note. For further details on this topic, see the appropriate datasheets.

2.3.6.3 MCG Control Register 3 (MCGC3)

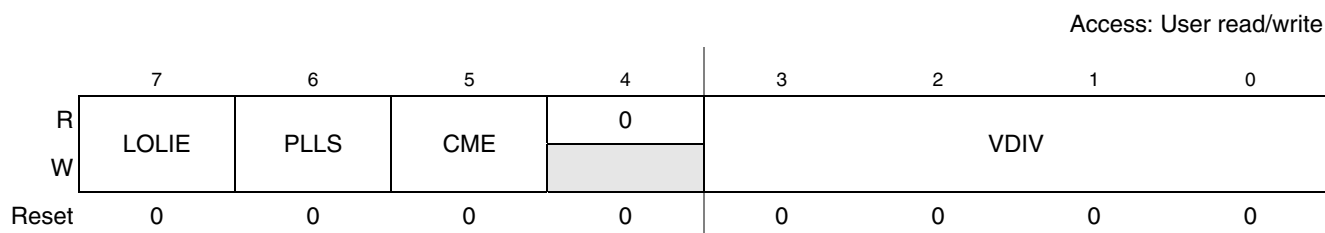


Figure 20. MCG Control Register 3

Unlike the ICG and ICS, the MCG contains a third control register, MCGC3.

The PLLS bit controls whether the PLL or FLL is selected. If the PLLS bit is clear, the PLL is disabled in all modes. If the PLLS bit is set, the FLL is disabled in all modes. The PLLST bit of MCGSC should be read to determine that PLLS is in the required state as shown in the code example in [Appendix C, “MCG Example Code”](#).

The VCO divider (VDIV) bits divide the VCO output of the PLL. The output of the VCO divider provides PLL feedback that allows the PLL to attain its target frequency. Because the PLL multiplies the reference frequency in direct proportion to its feedback, the resultant output frequency is the input reference frequency multiplied by the VCO divide factor.

The VCO divide factors range from 1 – 40 in multiples of four as shown in [Table 19](#).

Table 19. VCO Divide Factors

VCO bit states	Multiple factor
0000	4
0001	8
0010	12
0011	16
0100	20
0110	24
0111	28
1000	32
1001	36
1010	40
1011	Reserved (default to M=40)
11xx	Reserved (default to M=40)

MCGC3 also contains functionality for clock security in the form of the loss of lock interrupt enable (LOLIE) bit and clock monitor enable (CME) bit. These are explained in detail in [Section 2.3.8, “MCG System Protection”](#).

2.3.6.4 MCG Status and Control Register (MCGSC)

The status and control register is important to the overall clock module operation because it monitors the clock modes and contains security features that are able to indicate if a loss of lock or loss of clock were to occur.

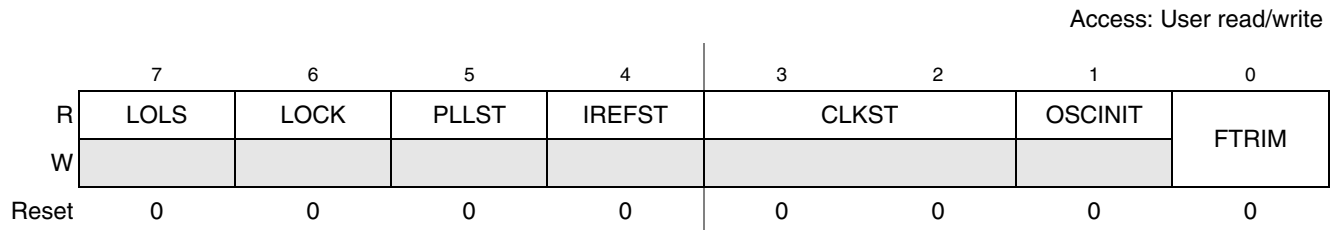


Figure 21. MCG Status and Control Register

The register provides scope for checking for loss of clock and loss of lock via the LOLS and LOCK bits.

The LOLS bit is a sticky indication of lock status for the FLL or PLL. LOLS is set when the FLL or PLL output frequency has unexpectedly fallen outside the lock exit frequency tolerance, and remains set until cleared by reset or by writing a logic 1 to LOLS. The loss of lock interrupt enable (LOLIE) bit in MCGC3 allows the program to determine if an interrupt will be requested when the loss of lock status (LOLS) bit is set.

The lock status (LOCK) bit indicates whether the FLL or PLL has acquired lock. If the LOCK bit is cleared, the MCG has lost lock and is operating at a frequency outside 6% of the target frequency. Entering stop mode, BLPI or BLPE modes, or by changing the configuration of the FLL or PLL causes a loss of lock. Further details of clock security are found in [Section 2.3.8, “MCG System Protection”](#).

PLLST reflects the status of the PLLS setting. It should be checked to ensure that changes to the PLLS bit have taken effect.

IREFST reflects the reference clock being used, internally or externally. It should be read to ensure that the correct reference is enabled. [Table 20](#) outlines the state for internal or external reference.

CLKST reflects the current clock mode and should be read to ensure that the correct mode is enabled. [Table 20](#) outlines the states and corresponding modes.

Table 20. State of PLLS, IREFST, and CLKST Bits

State of PLLS bit	
PLL	1
FLL	0
State of IREFST bit	
Internal	1
External	0
State of CLKST bit	
Output of FLL	00
Internal reference	01
External reference	10
Output of PLL	11

If the external reference clock is selected by ERCLKEN, the OSCINIT bit reflects the status of an external oscillator. This indicates that an external oscillator is initialized and ready for use. The OSCINIT should be read to determine that an external oscillator has been initiated prior to entering into FEE, FBE, PEE, PBE, or BLPE mode.

The FTRIM bit provides a fine adjustment of the internal reference clock frequency. Setting FTRIM increases the period and clearing FTRIM decreases the period by the smallest amount possible.

2.3.6.5 MCG Trim register (MCGTRM)

The trim register (MCGTRM) controls the internal reference clock period (it has no effect upon an external reference) and the clock frequency. Writing a high value to this register provides a slower frequency, whereas writing a lower value has the opposite effect. By default, the MCGTRM is set at 0x80. To trim the clock, the flash location (0xFFAE) should be used for storing FTRIM and 0xFFAF for storing the 8-bit trim value for MCGTRM register. The MCU does not automatically copy these values into flash locations to their respective registers. Therefore, you must copy these values from flash to the registers.

2.3.7 MCG Mode Switching

Figure 22 indicates the allowed movements between each of the states. Certain configuration bits must be changed to move properly between the modes. Each time any of these bits are altered (e.g. PLLS, IREFS, CLKS), the corresponding status bits in the MCGSC register (PLLST, IREFST, CLKST) must be checked before moving forward in the application software.

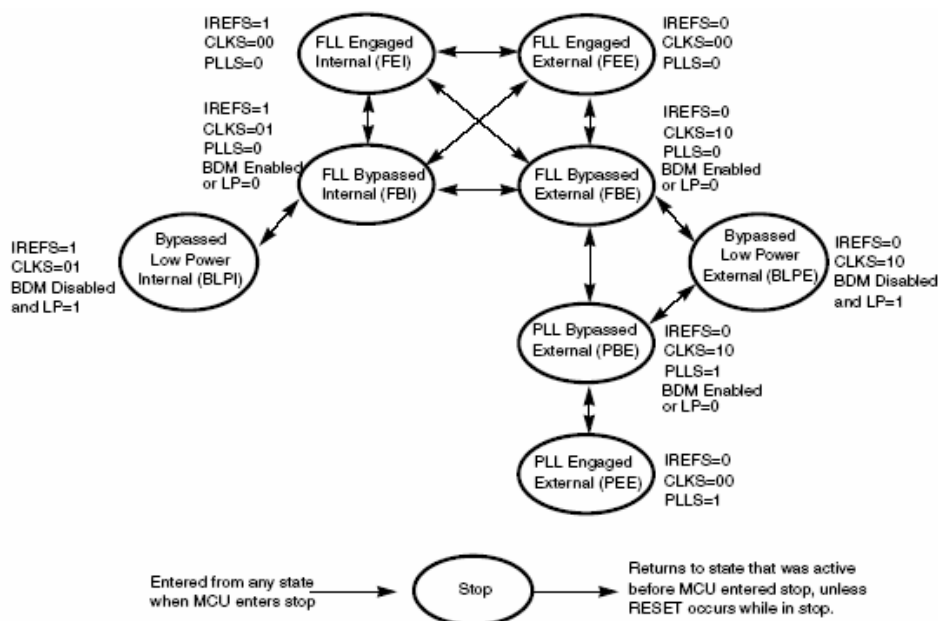


Figure 22. MCG Mode Configurations

As FEI is the default mode when the MCG comes out of reset, the only other MCG modes directly accessible are FEE, FBE and FBI modes (see [Figure 22](#)). Reaching the other modes requires the MCG to transition through one of these modes initially.

NOTE

The MCGSC register values must reflect these configuration changes.

The following explanation details how to switch from FEI mode to PEE mode (via FBE and PBE modes), using a 4 MHz external crystal to achieve a bus frequency of 8 MHz. An example is given in [Appendix C](#), “MCG Example Code 3.

- The first transition is from FEI mode to FBE mode. MCGC2 should be configured to utilize the external reference clock. This is achieved by setting the RANGE for high frequency range (4 MHz crystal), EREFS to select external oscillator, and ERCLKEN to initialize the oscillator (refer to code example for bit states).
- It is important to wait for OCSINIT in the MCGSC register to be set to indicate that the oscillator has been initialized.
- To complete the transition to FBE mode, the appropriate bits in MCGC1 should be set. The external reference clock should be selected as the system clock source using the CLKS bits. The external reference clock should be selected as the FLL reference clock via the IREFS bit. The reference divider (RDIV) bits should be configured so that the FLL reference clock is between the required range of 31.25 – 39.0625 kHz.
- Again, wait for the clock mode status (CLKST) and internal reference status (IREFST) bits to update. Both bits should indicate the external reference clock is being used. The MCG should now be running in FBE mode.
- The next stage is to transition to PBE mode. The example does not go into BLPE mode, although it is possible to go via this mode.



- MCGC1's RDIV bits must be set appropriately so that the PLL uses a reference clock in the range of 1 – 2 MHz.
- To enter PBE mode, the FLL must be disabled and PLL enabled by setting the PLLS bit in MCGC3. As the intention is to migrate to PEE mode it is convenient to set the VDIV multiplier, to the appropriate value, at this point.
- Confirmation that the MCG is in PBE mode is achieved by waiting on the PLLST bit of the MCGSC register to become set.
- To achieve PEE mode, wait until the LOCK status bit in MCGSC is set indicating the PLL is at its target frequency. Now, configure the CLKS bits in MCGC1 to select the output of the PLL as the system clock source.
- Finally, wait for CLKST bits of MCGSC to indicate the PLL output is the system clock source. The MCG is now configured in PEE mode.

2.3.8 MCG System Protection

The MCG contains a clock monitor that can detect loss of lock and loss of clock events. The clock protection bits (bits 5, CME, and bit 7, LOLIE) are found within MCG control register 3 (MCGC3). The loss of lock interrupt enable (LOLIE) bit allows the program to determine if an interrupt is requested when the loss of lock status (LOLS) bit is set. LOLS indicates whether FLL or PLL has lost lock since it was last cleared (from a reset or writing 1 to LOLS).

If LOLIE is set, the software can manage the loss of lock condition by switching the clock mode or waiting until lock has been re-acquired in an interrupt service routine.

The clock monitor enable (CME) bit of MCGC3 is responsible for the detection of loss of clock. It is only valid when the MCG is using an external reference clock (i.e. FEE, FBE, PEE, PBE, or BLPE). Setting the CME bit in any other mode causes the clock monitor to reset the MCU continuously. When CME has been set, it generates a reset request when the external clock is lost.

3 Available Clock Modes

Common to the clock modules are the various operating modes that they can operate in. The ability to operate in different modes gives rise to increased/decreased bus frequencies, greater accuracy and enhanced power utilization properties if required.

NOTE

For the various clock modules it is important to carefully monitor the mode switching procedures to move from one mode to another, as deviation from these could produce clock in-accuracies.

NOTE

Where reference is made to the PLL, only the MCG is applicable as the ICS and ICG do not contain a PLL.

3.1 FLL Engaged Internal (FEI)

FEI is the default mode of operation for the ICS and MCG. FEI clock mode uses the internal reference clock coupled through the FLL to produce the bus clock. The FLL can create frequencies that are multiples of the internal reference clock, thus providing a large range of bus frequencies. Because no external components are required, this mode provides the lowest system cost and has good clock accuracy when trimmed. Another advantage is that XTAL and EXTAL pins, normally associated with the external oscillator, can be used as general purpose I/O. The other main advantage to using an internal oscillator is that the start up times are faster on power-up and recovering from a STOP instruction.

The drawbacks of utilizing this mode are the small initial inaccuracies of the internal reference. However, this can be trimmed by software. It is possible to trim the oscillator to allow a wide range of frequencies including maximum bus rate. AN2496 goes into greater detail about trimming the internal reference clock. The internal reference clock is designed so it can be trimmed by up to $\pm 25\%$. It can be fine-tuned to within 0.1% of a specific target frequency by writing to the trim register and the FTRIM bit. The internal reference clock has a maximum deviation of $\pm 2\%$ over voltage and temperature.

3.2 FLL Engaged External (FEE)

FEE is similar to FEI mode, except the clock source is external. As a result, it is able to provide a system clock source with a higher accuracy than FEI mode, but this incurs an increased system cost and power consumption. Furthermore, the module can operate with a wide range of frequencies in low or high range. This allows operating frequencies across the full range of the clock module.

When using the FLL, it is important to enable the RDIV (reference divider) bits to divide the reference clock into the range of 31.25 – 39.0625 kHz to prevent over-clocking the device.

3.3 FLL Bypass Internal (FBI)

FBI mode has similarities to FEI mode except for the fact that the FLL has been bypassed and the output clock is derived from the internal reference clock directly. As well as being low cost because no external parts are required, this source can provide good accuracy when trimmed.

In FBI mode, the FLL remains operational but its output clock is not used. This allows the FLL to acquire its target frequency before switching into FEI or FEE mode. Similar to FEI mode, the XTAL and EXTAL pins are freed up and can be used as GPIO pins.

3.4 FLL Bypass External (FBE)

FBE mode shares many similarities with FBI mode, notably bypassing the FLL, but the external reference directly produces the output clock. The accuracy of the clock produced by the external source is derived from the accuracy of the external source itself. As with FBI, the FLL circuit remains active (but unused) and allows the circuit to acquire lock before the module switches into FEI and FEE modes. The accuracy of the clock is as high as the external reference and is unaffected by the FLL as it has been bypassed.

3.5 Bypass Low-Power Internal Mode (BLPI)

This operating mode is a subsidiary of FBI mode previously mentioned. To enter BLPI, set the low-power (LP) bit when running in FBI mode.

The benefit of BLPI mode is the power savings gained due to the FLL and PLL being disabled.

In BLPI mode, BDC communications are not possible. If BDC communications are requested in this mode, the clock module automatically switches to the bypassed mode FBI where BDC communications are possible.

3.6 Bypass Low-Power External Mode (BLPE)

This operating mode is a subsidiary of FBE/PBE mode(s) previously mentioned. To enter BLPE, set the low-power (LP) bit when running in FBE/PBE mode.

The benefit of BLPE mode is the power savings gained due to the FLL and PLL being disabled.

In addition, it is good practice when using the MCG module to use BLPE mode to make the transition from FLL modes to PLL modes (or vice versa). With the FLL and PLL disabled, changes to the RDIV bits can be made without causing them to run using an out of range reference clock (31.25 kHz to 39.625 kHz for FLL, 1.0 MHz to 2.0 MHz for PLL).

In BLPE mode, BDC communications are not possible. If BDC communications are requested in this mode, the clock module automatically switches to one of the bypassed modes (FBE/PBE) where BDC communications are possible.

3.7 PLL Engaged External (PEE)

Only applicable on the MCG, the system clock is derived from the PLL using an external reference clock. The external reference clock must be filtered into the range of 1 MHz – 2 MHz by the RDIV bits. The PLL clock locks to a frequency equal to the reference frequency times a multiplication factor as selected by the VDIV bits. This mode provides high clock accuracy due to the use of the PLL and external reference. However, the acquisition of the target frequency requires a longer time than FEE mode through the use of the PLL.

3.8 PLL Bypassed External (PBE)

Only applicable to the MCG, PBE mode has a similar function to FBE, except the PLL has been bypassed and the clock is derived from the external reference. The PLL does not generate the output frequency. However, as the PLL remains active, it can acquire lock at its target frequency. It is good practice to set the RDIV bits to divide the PLL reference frequency into the required range of 1 – 2 MHz in preparation for mode switching. The accuracy of the clock is as high as the external reference and is unaffected by the PLL as it has been bypassed.

3.9 Self-Clock Mode (SCM)

This operational mode is only applicable to the ICG in its default mode. The FLL is open loop and the DCO is free-running at a frequency set by the filter registers (ICGFLTH and ICGFLTL). This is the only mode in which the filter registers can be written, allowing direct control over the bus frequency. Writing a high value to the ICG filter registers provides a high bus frequency and writing a lower value to the registers has the opposite effect.

One of the main advantages this operation mode provides is that no external oscillator components are required, resulting in the XTAL and EXTAL pins being available as GPIO. This mode is most appropriate in systems where timing requirements are not critical.

4 Clock Module Comparison

All of the clock modules have similar properties. The ICS and MCG have evolved from the ICG. The MCG clock module has been designed with high-end applications in mind whereas the ICS is intended for smaller, lower power, and cost-sensitive applications.

Each of the clock modules contains an FLL (with the MCG also containing a PLL) and through the use of multiplier values, each module is capable of producing a different range of output frequencies. The ICS has six selectable multipliers in the low, middle, or high DCO frequency range given in [Table 4](#). The ICS depends on the other modules on the reference clock frequency to generate the desired system clock frequency. The ICS has a bus divider to provide extra flexibility in generating the system clock frequency. The bus divider is selectable from 1, 2, 4, or 8.

The ICG has eight software selectable multiplier values and eight software selectable frequency divider values allowing greater control over the system clock frequency.

The FLL on the MCG module has a fixed multiplication factor of 1024. This has similarities to the ICS FLL because it is dependent upon the reference clock to generate the desired system clock frequency. The MCG FLL has a bus divider to provide extra flexibility in generating the system clock frequency. The bus divider is selectable from 1, 2, 4, or 8.

The MCG is the only module to contain a PLL. The PLL uses a VCO divider and a bus divider to generate the desired system clock. The VCO divider is selectable in integer steps of four from 4 – 40. The same bus divider used on FLL is same as used on the PLL.

[Table 21](#) details some of the clock module properties and provides a short summary of the differences that exist between them.

Table 21. Clock Module Comparison

	MCG	ICG	ICS
Clock Source	PLL, FLL, OSC	FLL, OSC	FLL, OSC ¹
Number of operational modes²	8	4	6
Total clock status bits	8	9	3
Loss of lock	Interrupt	Interrupt or reset ³	N/A
Loss of clock	Reset	Reset or clock switching ³	N/A

¹ Some MCUs featuring an ICS module may not have external oscillator pins (EXTAL, XTAL) due to pin count and package limitations. In this case, the module would only have three operational modes.

² These do not include off modes.

³ Software selectable.

5 Conclusion

It should now be evident that each of the clock modules (MCG, ICG, and ICS) present within Freescale's family of HCS08 MCUs perform similar tasks, but have the potential to operate in different modes specific to different applications.

The ICS offers a cost-effective option for applications that require a lower powered clock module.

The ICG offers greater flexibility to generate a system clock and is more suitable for applications that require clock monitoring. On the other hand, the ICG does not have specific low-power modes such as FBELP and FBILP.

The MCG offers the low-power modes of the ICS and clock monitoring of the ICG. Furthermore, it's PLL makes the MCG suitable for time critical applications requiring accurate high frequency system clocks.

Appendix A

ICS Example Code

The code example uses a 32.768 kHz crystal and sets the ICS in FEE mode.

```

/*****
*
* PROGRAM Using S08QE128, the program will run uC in FEE Mode
*
* AUTHOR Steven McLaughlin, Applications Engineer, East Kilbride, Scotland
*
* DATE August 2007
*
* NOTES
*
*****/

/*****
*
* Copyright (C) 2006 Freescale Semiconductor, Inc.
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*
* Filename: ICS_demo.c
*
* Description:
*
* Notes:
* *****
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* * FREESCALE CW COMPILER AND HAS ONLY BEEN GIVEN A MIMIMUM *
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* *****
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*****/

/* include files */
#include "MC9S08QE128.H" /* include peripheral declarations */

```

```

/*****
*
* FUNCTION      main
*
* DESCRIPTION   - main routine
*               - sets up the ICS in FEE Mode
*
* RETURNS      None
*
* NOTES:       Fext = 32.768kHz (ext crystal)
*
*****/
void main(void) {

    /*Disable COP*/
    SOPT1_COPT=0b00;

/*****Set up the clock registers to enter FEE mode *****/

    ///////////////////////////////////ICS Control Register 2 (ICSC2)////////////////////////////////////
    //
    //      bit 7      bit 6      bit 5      bit 4      bit 3      bit 2      bit 1      bit 0
    //      -----
    //      |          BDIV          | RANGE |   HGO   |   LP   |  EREFS  | ERCLKEN | EREFSTEN|
    //      -----
    //      |    0          0    |    0   |    0   |    0   |    1    |    1    |    0    |
    //      -----
    //
    //
    //      BDIV      = 00      Set clock to divide by 1
    //      RANGE     = 0      Low Freq range selected (i.e. 32.768 kHz in high freq range)
    //      HGO       = 0      Ext Osc configured for low gain
    //      LP        = 0      FLL is not disabled in bypass modes
    //      EREFS     = 1      Osc requested
    //      ERCLKEN   = 1      IC SERCLK active
    //      EREFSTEN  = 0      Ext Reference clock is disabled in stop
    //
    ///////////////////////////////////
    ICSC2=0b00000110;

    /* Loop until OSCINIT = 1 - indicates crystal selected by EREFS bit has been initialised*/
    while(ICSSC_OSCINIT!=1);

    ///////////////////////////////////ICS Control Register 1 (ICSC1)////////////////////////////////////
    //
    //      bit 7      bit 6      bit 5      bit 4      bit 3      bit 2      bit 1      bit 0
    //      -----
    //      |          CLKS          |          RDIV          |  IREFS  | IRCLKEN | IREFSTEN |
    //      -----
    //      |    0          0    |    0   |    0   |    0   |    0    |    0    |    0    |
    //      -----
    //
    //
    //      CLKS      = 00      Select clk source via FLL

```

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```

//   RDIV      = 000   Set to divide by 1 (i.e. 31.768kHz/1 = 31.768kHz - in range required
by FLL)
//   IREFS     = 0     Ext Ref clock selected
//   IRCLKEN   = 0     ICSIRCLK inactive
//   IREFSTEN  = 0     Internal ref clock disabled in stop
//
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////

ICSC1=0b00000000;

/*loop until IREFST = 0 - indicates ext ref is current source*/
while(ICSSC_IREFST!=0);

/*loop until CLKST = 00 - indicates ext ref clk selected to feed ICSOUT*/
while(ICSSC_CLKST!=0b00);

ICSSC_DRST_DRS = 0b00;      /*set DCO factor at 512*/

PTED_PTEDO = 0;      /* Set port as o/p*/
PTEDD = 0x01;

for(;;) {

    PTED_PTEDO ^=1;      /* Toggle PTE0 */
    __RESET_WATCHDOG(); /* feeds the dog */
} /* loop forever */
/* please make sure that you never leave main */
}

```

Appendix B

ICG Example Code

B.1 Program One

The following program enables the clock in FEI mode to run the bus frequency at 5.4 MHz. Without trimming the clock, frequency is approximately 5.5 MHz. When the clock is trimmed with a weighting of 8F, this reduces the clock frequency to 5.42 MHz.

```

/*****
 *
 * PROGRAM - Demonstration of the ICG Modes - Used S08GB60
 *
 * VERSION - Ver 1.0
 *
 * Author - Steven McLaughlin, Application Engineer, East Kilbride
 *
 * DATE - August 2007
 *
 *****/

/*****
 *
 * Copyright (C) 2006 Freescale Semiconductor, Inc.
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 *
 * Filename: main.c
 *
 * Description:
 *
 * Notes:
 * *****
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 * * FREESCALE CW COMPILER AND HAS ONLY BEEN GIVEN A MIMIMUM *
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```

```

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*****/
#include <hidef.h> /* for EnableInterrupts macro */
#include "derivative.h" /* include peripheral declarations */
#include<MC9S08GB60.h>
volatile unsigned char NVICGTRIM @0x000FFBE;

void main(void)
{

    /*DISABLE THE COP - PREVENTS MCU RESETTING*/
    SOPT_COPE=0;

    ICGTRM=NVICGTRIM; //store ICG trim value from NV ICG trim reg into ICG trim reg

/*****
* Configuration FLL engaged; internal clock reference (FEI MODE)
*
* f(IRG) = 243 kHz
* f(BUS) = 5.4 MHz
* P = 64 (low frequency range)
*
* N/R = (2*f(BUS))/((f(IRG)/7) * P) = 10,2
*
* N = 10
* R = 2
*****/

/***** ICG Control register 1 settings *****/

    bit 7   bit 6   bit 5   bit 4   bit 3   bit 2   bit 1   bit 0
    -----
    |  0   | RANGE |  REFS |   CLKS   | OSCSTEN |  LOCD  |   0   |
    -----
    |  0   |   0   |   1   |   0   |   1   |   0   |   0   |   0   |
    -----

    HGO      = 0      configure OSC for low power
    RANGE    = 0      configure OSC for low frequency range; FLL prescale factor is 64
    REFS     = 1      Osc using crystal or resonator requested (don't care term)
    CLKS     = 0b01   FEI Mode
    OSCSTEN  = 0      disable oscillator
    LOCD     = 0      Loss of clock enabled

*****/

    ICGC1=0b00101000;

/***** ICG Control register 2 settings *****/

    bit 7   bit 6   bit 5   bit 4   bit 3   bit 2   bit 1   bit 0
    -----
    | LOLRE |           MFD           | LOCRE |           RFD           |
    -----

```

```
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
-----
```

```
LOLRE = 0      Generates an interrupt request on loss of lock
MFD   = 011    Set MFD to 10 (multiplier)
LOCRE = 0      Generates an interrupt request on loss of clock
RFD   = 001    Sets the RFD division factor to R=2
```

```
*****/

ICGC2=0b00110001;

while(ICGS1_LOCK!=1); //wait until FLL is locked

PTFD_PTFD0 = 0;      /* Set port as o/p*/
PTFDD = 0x01;

for(;;) {

    PTFD_PTFD0 ^=1;      /* Toggle PTF0 */
    __RESET_WATCHDOG(); /* feeds the dog */
} /* loop forever */
/* please make sure that you never leave main */
}
```

B.2 Program Two

The following program utilizes the real time interrupt (RTI) to generate a periodic interrupt, which is based on the source clock period. The LEDs on the demo board are programmed to flash to indicate a wake-up event.

```
*****/
*
* PROGRAM - Demonstration of the RTI interrupt to toggle the GB60 EVB LED1 periodically*
*
* VERSION - Ver 1.1
*
* Author - Steven McLaughlin
*
* DATE - August 2007
*
*****/

/*****
*
* Copyright (C) 2006 Freescale Semiconductor, Inc.
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*
* Filename: main.c
*
* Description:
*
* Notes:
```

```

* *****
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*****/

#include <hidef.h> /* for EnableInterrupts macro */
#include "derivative.h" /* include peripheral declarations */
#include <MC9S08GB60.h>

/*****Prototypes*****/
extern void init_ICG (void);
extern void vector (void);

/*****DEFINES*****/
/*COMMON BIT DEFINITIONS*/
#define BIT0 0x01
#define BIT1 0x02
#define BIT2 0x04
#define BIT3 0x08
#define BIT4 0x10
#define BIT5 0x20
#define BIT6 0x40
#define BIT7 0x80

/* DEFINES FOR CHANGES STATUS OF LEDS*/
#define SWITCH_OFF 1
#define SWITCH_ON 0

/*INIT LEDS FOR GB60DEMO EVB*/
#define init_LED() PTFDD = (BIT3|BIT2|BIT1|BIT0);/* Set Port F bit0-3 as output */\
PTDDD_PTDDD0 = 1; /* Set Port D bit0 as output */\
PTDD_PTDD0 = SWITCH_OFF; /* Switch off LED 5 */\
PTFD = (BIT3|BIT2|BIT1|BIT0) /* Switch off LED 1-4 */\

```



```

/* definition of the LED macros */
#define LED1 PTFD_PTFD0
#define LED2 PTFD_PTFD1
#define LED3 PTFD_PTFD2
#define LED4 PTFD_PTFD3
#define LED5 PTDD_PTDD0

/***** FUNCTIONS *****/

/*****
 *
 * FUNCTION - Main
 *
 * DESCRIPTION - Setup registers
 *               - Blink LED1 in time with RTI
 *
 * RETURNS      - None
 *****/

void main(void) {

    /*initiate ICG clock*/
    init_ICG();

    /*initiate LEDs*/
    init_LED();

    /*****SYSTEM OPTION REGSITER (SOPT)*****/

    BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0
    -----
    | COPE | COPT | STOPE | 1 | 0 | 0 | BKGDPPE | 1 |
    -----
    | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
    -----

    COPE=0; COP WATCHDOG TIMER DISABLED
    COPT=1; LONG TIMEOUT PERIOD (2^18)
    STOPE=1; STOP MODE ENABLED
    BKGDPPE=1; BKGDP PIN DISABLED

    /*****/

    SOPT = 0b01100010;

    /*****SYSTEM POWER MANAGEMENT STATUS & CONTROL REGISTER 1 (SPMSC1)*****/

    BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0
    -----
    | LVDF | LVDACK | LVDIE | LVDRE | LVDSE | LVDE | 0 | 0 |

```

Clock Options on the HC9S08 Family, Rev. 0

```

-----
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
-----

```

```

LVDF=0;   READ ONLY STATUS BIT INDICATING LOW VOLTAGE DETECT
LVDACK=0; WRITE ONLY BIT TO ACK LOW VOLT DETECT ERRORS
LVDIE=1;  REQUEST H/W INTERRUPT
LVDRE=0;  LVDF DOES NOT GENERATE H/W RESETS
LVDSE=1;  LOW VOLT DETECT ENABLED DURING STOP
LVDE=1;   LVD LOGIC ENABLED

```

*****/

```
SPMSC1=0b00101100;
```

```
/*****SYSTEM POWER MANAGEMENT STATUS & CONTROL REGISTER 2 (SPMSC2)*****/
```

```

      BIT7 |  BIT6 |  BIT5 |  BIT4 |  BIT3 |  BIT2 |  BIT1 |  BIT0
-----
| LVWF | LVWACK | LVDV | LVWV | PPDF | PPDACK | PDC | PPDC |
-----
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | X |
-----

```

```

LVWF=0; LOW VOLTAGE WARNING NOT PRESENT
LVWACK=0;
LVDV=1; LOW TRIP POINT SELECTED
LVWV=1; HIGH TRIP POINT SELECTED
PPDF=0; NOT STOP2 MODE RECOVERY
PPDACK=0;
PDC=1; POWER DOWN MODES ARE ENABLED (0 for STOP3)
PPDC=1;STOP2, FULL PWR DOWN (WRITE ONCE) (X for STOP3)

```

*****/

```
SPMSC2=0b00110011;
```

```
/*****SYSTEM RTI STATUS & CONTROL REGISTER (SRTISC)*****/
```

```

      BIT7 |  BIT6 |  BIT5 |  BIT4 |  BIT3 |  BIT2 |  BIT1 |  BIT0
-----
| RTIF | RTIACK | RTICLKS | RTIE | 0 | RTIS2 | RTIS1 | RTIS0 |
-----
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
-----

```

```

RTIF=0;   (READ ONLY) PERIODIC WAKE-UP TIMER NOT TIMED OUT
RTICLKS=1; REAL TIME INTERRUPT REQUEST CLOCK SOURCE IS EXTERNAL
RTIE=1;   REAL TIME INTERRUPTS ENABLED
RTIS2:RTIS1:RTIS0 = 1:1:1 INTERRUPT PERIOD ENABLED (external source)

```

*****/

```
SRTISC=0b00110111;
```

```

EnableInterrupts; /* enable interrupts */

for(;;) {

    __RESET_WATCHDOG(); /* feeds the dog */
    /* loop forever */

}

/* please make sure that you never leave main */
/*****
* Interrupt :   RTI_ISR
*
* Description: RTI interrupt
*
* Returns:      none
*
* Notes:        clear flags
                 toggle LED1
*****/
interrupt void RTI_ISR( void )
{
/* clear RTI flag */
SRTISC_RTIACK = 1;

/*clear partial power down flag*/
SPMSC2_PPDACK = 1;

/* toggle LED1 */
LED1 = ~ LED1;}

```

Appendix C

MCG Example Code

```

/*****
*
* PROGRAM Using DZ60, the program will switch from FEI mode
*         to PEE Mode
*
* AUTHOR Steven McLaughlin, Application Engineer, East Kilbride
*
* DATE August 2007
*
* NOTES
*
*****/

/*****
*
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*
* Filename: main.c
*
* Description:
*
* Notes:
* *****
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*****/

#include <hidef.h> /* for EnableInterrupts macro */
#include "derivative.h" /* include peripheral declarations */

```

```
#include "MC9S08DZ60.h"

/*****
*
* FUNCTION      main
*
* DESCRIPTION   - main routine
*               - sets up the MCG to switch from initial mode of FEI to
*               PEE.
*
* RETURNS      None
*
* NOTES:
*
* Fext = 4MHz (ext crystal)
* want to change the bus frequency to 8MHz and will do this
* by switching modes from FEI to PEE
*
* Fmcgout = [(Fext/R)*M/B] - for PEE mode
* Fbus = Fmcgout/2
*
*****/
void main(void) {

    /*Disable COP*/
    SOPT1_COPT=0b00;

    /*Set up the clock registers */

/*****MCG Control Register 2 (MCGC2)*****/
*
*   bit 7   bit 6   bit 5   bit 4   bit 3   bit 2   bit 1   bit 0
*   -----
*   |   BDIV   | RANGE |   HGO   |   LP   |  EREFS | ERCLKEN | EREFSTEN|
*   -----
*   |    0    |    1   |    1   |    0   |    1   |    1   |    0   |
*   -----
*
*   BDIV      = 00    Set clock to divide by 1
*   RANGE     = 1    High Freq range selected (i.e. 4MHz in high freq range)
*   HGO       = 1    Ext Osc configured for high gain
*   LP        = 0    FLL or PLL is not disabled in bypass modes
*   EREFS     = 1    Oscillator requested
*   ERCLKEN   = 1    MCGERCLK active
*   EREFSTEN  = 0    Ext Reference clock is disabled in stop
*
*****/
    MCGC2=0b00110110;

    /* Loop until OSCINIT = 1 - indicates crystal selected by EREFS bit has been initialised*/
    while(MCGSC_OSCINIT!=1);

/*****MCG Control Register 1 (MCGC1)*****/
```

Clock Options on the HC9S08 Family, Rev. 0

```

*
*   bit 7   bit 6   bit 5   bit 4   bit 3  bit 2   bit 1   bit 0
*   -----
*   |       CLKS       |       RDIV       |  IREFS  | IRCLKEN | IREFSTEN |
*   -----
*   |   1       0   |   1   |   1   |   1   |   0   |   0   |   0   |
*   -----
*
*
*   CLKS    = 10    Select Ext reference clk as clock source
*   RDIV    = 111  Set to divide by 128 (i.e. 4MHz/128 = 31.25kHz - in range required by FLL)
*   IREFS   = 0    Ext Ref clock selected
*   IRCLKEN = 0    MCGIRCLK inactive
*   IREFSTEN = 0   Internal ref clock disabled in stop
*
*****/
MCGC1=0b10111000;

/*loop until IREFST = 0 - indicates ext ref is current source*/
while(MCGSC_IREFST!=0);

/*loop until CLKST = 10 - indicates ext ref clk selected to feed MCGOUT*/
while(MCGSC_CLKST!=0b10);

/*-----ABOVE CODE ALLOWS ENTRY FROM FEI TO FBE MODE-----*/

/*****MCG Control Register 1 (MCGC1)*****/
*
*   bit 7   bit 6   bit 5   bit 4   bit 3  bit 2   bit 1   bit 0
*   -----
*   |       CLKS       |       RDIV       |  IREFS  | IRCLKEN | IREFSTEN |
*   -----
*   |   1       0   |   0   |   1   |   0   |   0   |   0   |   0   |
*   -----
*
*
*   CLKS    = 10    Select Ext reference clk as clock source
*   RDIV    = 010  Set to divide by 4 (i.e. 4MHz/4 = 1 MHz - in range required by FLL)
*   IREFS   = 0    Ext Ref clock selected
*   IRCLKEN = 0    MCGIRCLK inactive
*   IREFSTEN = 0   Internal ref clock disabled in stop
*
*****/
MCGC1=0b10010000;

/*****MCG Control Register 3 (MCGC3)*****/
*
*   bit 7   bit 6   bit 5   bit 4   bit 3  bit 2   bit 1   bit 0
*   -----
*   | LOLIE |  PLLS |  CME |   0   |           VDIV           |
*   -----
*   |   0   |   1   |   0   |   0   |   0   |   1   |   0   |   0   |
*   -----
*
*

```

```

*   LOLIE = 0    No request on loss of lock
*   PLLS  = 1    PLL selected
*   CME   = 0    Clock monitor is disabled
*   VDIV  = 0100 Set to multiply by 16 (1Mhz ref x 16 = 16MHz)
*
*****/

MCGC3=0b01000100;

/*loop until PLLST=1 - indicates current source for PLLS is PLL*/
while(MCGSC_PLLST!=1);

/*loop until LOCK=1 - indicates PLL has aquired lock*/
while(MCGSC_LOCK!=1);

/*-----ABOVE CODE ALLOWS ENTRY FROM FBE TO PBE MODE -----*/

/*****MCG Control Register 1 (MCGC1)*****/
*
*   bit 7   bit 6   bit 5   bit 4   bit 3   bit 2   bit 1   bit 0
*   -----
*   |   CLKS   |   RDIV   |   IREFS   |   IRCLKEN   |   IREFSTEN   |
*   -----
*   |   0     0   |   0     |   1     0   |   0     0   |   0     0   |
*   -----
*
*   CLKS    = 00    Select PLL clock source
*   RDIV    = 100   Set to divide by 4 (i.e. 4MHz/4 = 1 MHz - in range required by PLL)
*   IREFS   = 0     Ext Ref clock selected
*   IRCLKEN = 0     MCGIRCLK inactive
*   IREFSTEN = 0    Internal ref clock disabled in stop
*
*****/

MCGC1=0b00010000;

/*loop until CLKST =11 - PLL O/P selected to feed MCGOUT in current clk mode*/
while(MCGSC_CLKST!=0b11);

/*-----ABOVE CODE ALLOWS ENTRY FROM PBE TO PEE MODE-----*/

/*****
**
*   Therefore, RDIV - 4
*               BDIV - 1
*               VDIV - 16
*
*           Fmcgout = [(4MHz/4)*16]/1
*                   = 16MHz
*
*   Also         Fbus = Fmcgout/2
*                 = 8MHz
*
**

```

* Note: Expect the MCLK to display clk.

*

**/

```
/*Output the clock on PTA0 using MCLK - set the MCSEL bits on SOPT2 register to divide by 1*/  
SOPT2 = 0b10000001;
```

```
for(;;) {  
    __RESET_WATCHDOG(); /* feeds the dog */  
} /* loop forever */  
/* please make sure that you never leave main */  
}
```


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Document Number: AN3499
Rev. 0
01/2008

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