Freescale Semiconductor
Application Note

Document Number: AN3624
Rev. 0, 04/2008

S12X Temperature Sensor

Considerations for Using the S12X Temperature Sensor

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Many S12X devices feature temperature monitoring circuitry. This application note outlines considerations for using the temperature sensor in applications.

Section 1 introduces the temperature sensor circuit.

Section 2 describes temperature monitoring.

Section 3 describes using the high temperature interrupt.

Section 4 discusses general thermal considerations.

For more information, see the MC9S12XE, MC9S12XF, and MC9S12XS reference manuals available at Freescale.com.

Contents

1 Introduction to the Temperature Sensor

The temperature sensor is an integral part of the on-chip voltage regulator on MC9S12XE, MC9S12XF, and MC9S12XS family devices. Where temperature monitoring is supported by the device, this is detailed in

the device overview VREG configuration subsection and main VREG sections of the reference manual. The internal temperature sensor is not intended to be a high accuracy temperature sensor but can be used for temperature monitoring in many applications.

1.1 Objectives

The objectives of this document are:

- To provide an overview of the S12X temperature sensor features and their limitations
- To explain how to use the S12X temperature sensor features in an application environment
- To summarize thermal considerations in association with temperature sensor use

1.2 Overview

The temperature sensor monitors the device junction temperature (T_J), which may differ considerably from ambient temperature. The relationship between ambient and junction temperature is discussed in more detail in Section 4, “General Thermal Considerations.”

The temperature sensor offers the following basic features:

- A linearly temperature-dependent voltage with analog-to-digital module (ATD) interface for temperature monitoring
- A high temperature interrupt including hysteresis and offset trimming

The circuit provides a linear dV/dT across process and supply voltage within the operating range — however, the untrimmed absolute voltage precision may be unacceptable for some applications. To overcome this inaccuracy, software-programmable offset trimming via a trimming register is featured.

The linearly temperature-dependent voltage (V_{HT}) is connected to an ATD special channel input within the device. For temperature sensor ATD channel mapping, please refer to the reference manual device overview VREG subsection, as this is device-dependent. The MC9S12XE, MC9S12XF and MC9S12XS families map V_{HT} to ATD0[17].

The S12X devices are offered with different temperature ratings (C, V, and M) as shown in Table 1.

Table 1. Temperature Ratings (S12XE, S12XF, S12XS Families)

Classification	Parameter	Min	Typ	Max	Unit
C Operating junction temperature range Operating ambient temperature range	T_J T_A	–40 –40	— 27	110 85	°C
V Operating junction temperature range Operating ambient temperature range	T_J T_A	–40 –40	— 27	130 105	°C
M Operating junction temperature range Operating ambient temperature range	T_J T_A	–40 –40	— 27	150 125	°C

At the characterized trim value (0x88) the high-temperature interrupt feature can be used only on devices with temperature rating M, because the interrupt assert level at this trim value could lie above 140 °C. However, this does not restrict the use of the temperature sensor for temperature monitoring via the ATD on devices rated C or V. Furthermore, devices rated C or V can use the HTI feature at higher trim values.

1.2.1 Modes of Operation

The temperature sensor can be enabled in any device resource mapping mode.

The temperature sensor is disabled automatically in system stop mode (VREG reduced power mode).

1.3 Temperature Sensor Theory of Operation

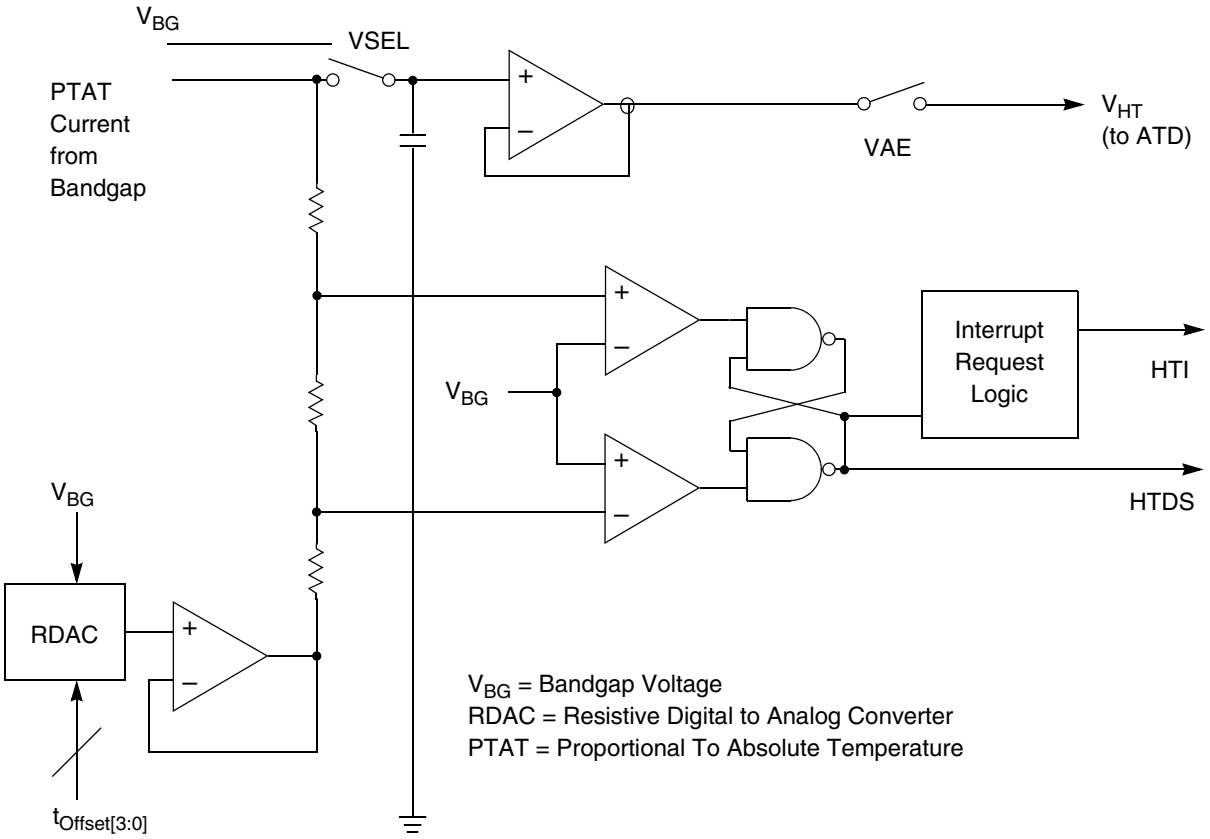

Figure 1. Temperature Sensor Principle

A temperature-dependent output from the VREG bandgap is used to bias a stack of resistors. The resulting voltage (V_{HT}) is connected to the ATD through a buffer amplifier.

Two taps of the resistor ladder are compared with a fixed voltage from the bandgap reference (V_{BG}) to generate assert and deassert signals for the high temperature interrupt feature and thus guarantee hysteresis.

The circuit provides reasonable dV/dT accuracy — however, the untrimmed absolute voltage may be unacceptable for many applications. To overcome this inaccuracy, the bottom node of the resistor ladder is forced to a programmable fraction of V_{BG} to allow trimming of the sensor offset.

The range of V_{HT} voltages generated in the device operating range does not exceed 2.5 V and is thus compatible with the ATD configured for the 3.3 V range. This is however less accurate than the preferred 5 V ATD range.

1.4 Temperature to Voltage Relationship

The dV/dT slope is linear across the operating temperature range, so the junction temperature can be determined from the voltage V_{HT} after the voltage has been calibrated (Figure 2).

The slope dependence on device processing is very small. The current specification is:

$$dV/dT(min) = 5.05\ mV/°C \quad \textit{Eqn. 1}$$

$$dV/dT(max) = 5.45\ mV/°C \quad \textit{Eqn. 2}$$

$$(\sim 5.25\ mV/°C \pm 4\%) \quad \textit{Eqn. 3}$$

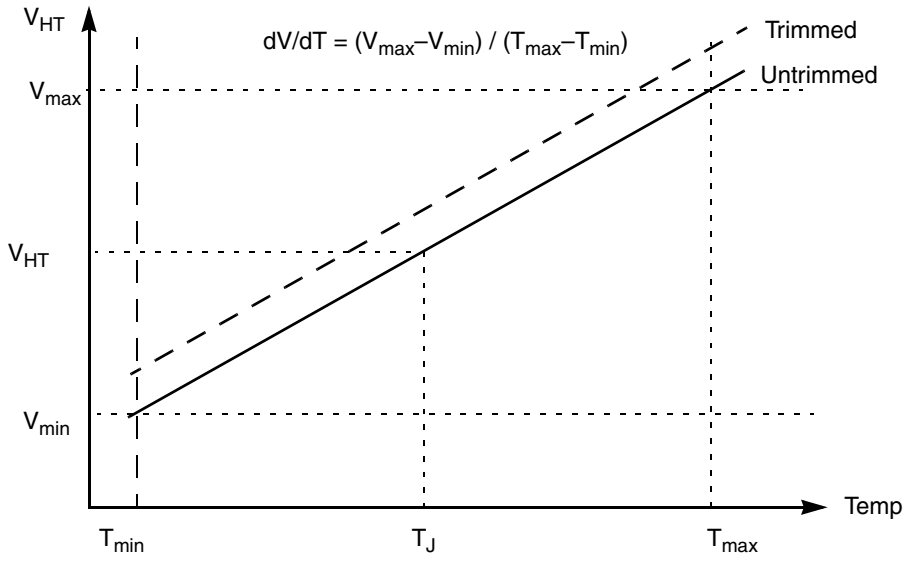

Figure 2. Voltage Temperature Dependence

Trimming provides a constant offset, as depicted in Figure 2. Trimming does not affect the slope but can be used for setting the HTI level (see Section 3, “Using the High Temperature Interrupt”).

2 Temperature Monitoring

Temperature monitoring can be performed on the dedicated ATD channel, after calibration of the V_{HT} voltage at known temperatures. Because the dV/dT slope is linear, the junction temperature can be determined from the voltage V_{HT} after the voltage has been calibrated at a known temperature, as shown in Figure 2.

Perform calibration at a minimum and maximum temperature for a more exact slope coefficient, independent of device processing.

The temperature T_J is then given by the equation $T_J = \frac{(V_{HT} - V_{min})}{(dV)/(dT)} + T_{min}$.

2.1 Temperature Monitoring Configuration

The temperature sensor is configured using the control register VREGHTCL and trimmed using the trim register VREGHTTR. For monitoring the temperature on the internal ATD channel, it is also necessary to configure the ATD registers. Register configuration is described in the following subsections.

2.1.1 Temperature Sensor Control Register VREGHTCL

Address Offset = VREG offset + 0

	7	6	5	4	3	2	1	0
R	0	0	VSEL	VAE	HTEN	HTDS	HTIE	HTIF
W								
Reset	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

Figure 3. VREGHTCL Register

Table 2. VREGHTCL Field Descriptions

Field	Description
7, 6 Reserved	These reserved bits are used for test purposes and are writable only in special modes. They must remain clear for correct temperature sensor operation.
5 VSEL	**Voltage Access Select Bit** — Selects either the temperature sensor or the bandgap voltage (V_{BG}) as VREG source for the ATD channel input. 0 Temperature sensor voltage is mapped to the ATD channel. 1 Bandgap voltage (V_{BG}) is mapped to the ATD channel.
4 VAE	**Voltage Access Enable Bit** — If this bit is set the voltage selected by VSEL is connected to the ATD channel (see device level specification for connectivity). 0 Voltage selected by VSEL is not connected to the ATD channel. 1 Voltage selected by VSEL is connected to the ATD channel.
3 HTEN	**High Temperature Enable Bit** — If this bit is set the temperature sensor is enabled. 0 The temperature sensor is disabled. 1 The temperature sensor is enabled.
2 HTDS	**High Temperature Detect Status Bit** 0 Temperature T_{DIE} is below level T_{HTID} or VREG is in reduced power mode (RPM) or shutdown mode. 1 Temperature T_{DIE} is above level T_{HTIA} and VREG is in FPM.
1 HTIE	**High Temperature Interrupt Enable Bit** 0 Interrupt request is disabled. 1 Interrupt will be requested whenever HTIF is set.
0 HTIF	**High Temperature Interrupt Flag** — HTIF is set to 1 when HTDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (HTIE=1), HTIF causes an interrupt request. 0 No change in HTDS bit. 1 HTDS bit has changed. **Note:** On entering the reduced power mode the HTIF is not cleared by the VREG.

To enable the temperature sensor, the HTEN bit must be set by software. To route the V_{HT} voltage to the ATD, set the VAE bit and clear the VSEL bit. VREGHTCL[7:6] must also remain cleared. The bits

VREGHTCL[2:0] do not affect the V_{HT} input to the ATD. These bits are discussed in Section 3, "Using the High Temperature Interrupt."

Write VREGHTCL = 0x18 to configure for temperature monitoring without HTI functionality.

2.1.2 High Temperature Trimming Register VREGHTTR

The VREGHTTR register allows trimming of the VREG temperature sensor offset to adjust the HTI temperature. HTOEN enables the trimming feature and HTTR[3:0] determines the trim level. The contents of the trimming register are loaded from an information row location of the flash memory in the reset phase. This facilitates factory programming of the trim value. Currently the value loaded in the reset phase is 0x0F. The dV/dT is not influenced by the value in this register.

Address Offset = VREG offset + 7

	7	6	5	4	3	2	1	0
R	HTOEN	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	1[1]	1[1]	1[1]	1[1]

1. Reset value is either 1 or preset by factory.

= Unimplemented or Reserved

Figure 4. VREGHTTR

Table 3. VREGHTTR Field Descriptions

Field	Description
7 HTOEN	**High Temperature Offset Enable Bit** — If set, the temperature sense offset is enabled. 0 The temperature sense offset is disabled. 1 The temperature sense offset is enabled.
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 4 for trimming effects.

Table 4. Trimming Effect of HTTR

Bit	Trimming Effect
HTTR[3]	Decreases the effective HTI temperature by twice an HTTR[2] step
HTTR[2]	Decreases the effective HTI temperature by twice an HTTR[1] step
HTTR[1]	Decreases the effective HTI temperature by twice an HTTR[0] step
HTTR[0]	Decreases the effective HTI temperature (to apply offset)

Each trim step is typically equivalent to –5°C offset in the HTI assert and deassert levels T_{HTIA} and T_{HTID}.

2.1.3 ATD Configuration

ATD0 is used for devices with more than one ATD module.

To obtain a resolution of more than one count/°C, the ATD must be configured for 12-bit mode conversions by configuring ATDCTL1[6:5] = 0x2.

To select the V_{HT} voltage for conversion ATDCTL5 must be configured to select the correct channel. For the MC9S12XE, MC9S12XF, and MC9S12XS families, the configuration ATDCTL5 = 0x41 selects Channel[17] for the conversion and uses a single sequence of conversions from that channel.

Using an ATDCTL3 value of 0x40, the sequence consists of eight conversions. Using this configuration it is possible to average the reading to minimize the effect of noise, or to filter out any outlying conversion results.

2.1.4 Summary of Recommended Register Values

Table 5. Recommended Register Value Summary

Register	Value
VREGHTCL	0x18
VREGHTTR	0x88
ATDCTL1	0x4F
ATDCTL5	0x41
ATDCTL3	0x40

2.2 Calibration

For maximum accuracy, calibrate the temperature sensor voltage V_{HT} at the two extremes of the application's temperature range — T_{max} and T_{min} — to determine the slope dV/dT (Figure 3) and the V_{min} value.

To perform calibration properly, the V_{min} and V_{max} values must be sensed at known temperatures T_{min} and T_{max}, respectively. Then the dV/dT slope can be calculated and stored together with the V_{min} value in NVM.

Calibration must be performed in a low-noise environment and use the ATD configuration described in Section 2.1.3, "ATD Configuration," to reduce the effect of noise.

The device must be allowed time to stabilize at the calibration temperatures to ensure that the silicon has attained the correct temperature for calibration.

To account for the difference between ambient and junction temperature, the power consumption during calibration can be measured and the true junction temperature calculated using the equation:

$$T_J = T_A + (P_D \times \Theta_{JA})$$

If it is not possible to do this on each device, a measurement on a single device using a low power configuration may be sufficient.

If the temperature sensor is to be used to monitor junction temperature (for example, to avoid excessive temperatures by reducing activity) then calibration must be carried out with low device power dissipation

to minimize the junction-to-ambient differential temperature. For the purpose of calibration, it is advisable to disable output drivers, where possible, and run the part at low bus frequency without peripheral activity.

If the temperature sensor is to be used to calculate ambient temperature, it is recommended that temperature measurements always be taken with a consistent device activity. In this case, calibration must be carried out using the defined device activity at which temperature is measured in the application.

The dV/dT slope dependency on V_{DDA} supply voltage is negligible in the V_{DDA} range 3.15 to 5.5 V.

Calibration at a single temperature, with the same considerations mentioned above, is also possible, whereby the temperature is then estimated from the specified dV/dT (Section 1.4, “Temperature to Voltage Relationship”). In this case the accuracy is worse because the specified slope includes production process variation, which is eliminated when calibrating at T_{max} and T_{min}.

2.3 Temperature Monitoring Accuracy

Factors that could affect dV/dT accuracy are described in the following subsections.

2.3.1 Process Dependency

Using the above calibration method removes device process inaccuracy, because the slope for a given device is constant over the operating range.

2.3.2 Linearity of the dV/dT Slope

Characterization showed a negligible variation in linearity.

2.3.3 Supply Voltage Dependency

The dV/dT slope dependence on V_{DDA} is negligible, although a minor offset in absolute voltage exists. For applications with a V_{DDA} variation of ±10%, the supply-voltage-dependent offset is equivalent to less than 1 °C. For applications with a large V_{DDA} range, an error may exist that equates to up to 2 °C. It is possible to calibrate the minor offset to reduce the total error as explained in Section 2.3.5, “ATD Inaccuracy.”

2.3.4 Shifting of Bandgap Current Over Time

Characterization results show a negligible variation in linearity.

2.3.5 ATD Inaccuracy

The typical dV/dT slope is 5.25 mV/°C. To obtain a resolution of more than one ATD count/°C, the ATD must be configured for 12-bit conversions, which corresponds to 1.25 mV/count at 5.12 V ATD reference voltage. Generally the absolute error of the ATD in 12-bit conversion mode is ±7 counts and integral nonlinearity is ±5 counts. The temperature is monitored with respect to a calibrated value, so the offset can be ignored and integral nonlinearity can be used to calculate the inaccuracy. The ±5 counts translates to

±6.25 mV, which equates to ±1.2°C. To limit the effects of noise and increase ATD accuracy, use a sequence of conversions and average the result, as described in Section 2.1.3, “ATD Configuration.”

The ATD accuracy is limited by the accuracy of the ATD reference voltage. This can have a very large impact on temperature monitoring accuracy as illustrated in the following example.

Assuming a perfect ATD V_{REF} reference, with a dV/dT inherent inaccuracy of 4%, the accuracy of the temperature sensor is given by:

$$(4\% \times \text{target temperature range}) + 1.2\ ^{\circ}\text{C (ATD integral non-linearity)} + 1\ ^{\circ}\text{C (supply voltage dependency)} \qquad \textit{Eqn. 4}$$

Over a range from 0 °C to 100 °C this gives (0.04 × 100) + 2.2 = ±6.2 °C.

However with a V_{REF} tolerance of $V_{REF} = V_{DDA} = 5V \pm 5\% = 100$ mV.
At a minimum slope of 5.05 mV/°C, this equates to 19.8 °C.

So the total inaccuracy could be as much as ±26 °C with over 75% of this coming from changes in V_{REF}.

The V_{REF} effect can be limited by calibrating the ATD offset using the bandgap reference. The bandgap reference voltage is accessible on the same ATD channel as the temperature sensor. To select the bandgap voltage as the input to the ATD channel, set the VSEL bit, VREGHTCR[5]. By performing ATD conversions using different values of V_{REF}, the V_{REF} variation can be calibrated. Because the bandgap voltage variation over the whole specified temperature range is only 5 mV, an ATD conversion of V_{BG} can be used to estimate V_{REF}.

2.3.6 Junction and Ambient Temperature Differentials

If the application is monitoring the silicon temperature, for example to limit power dissipation then the temperature calculated from V_{HT} is mainly subject to the inaccuracies listed in Section 2.3.1 through Section 2.3.5.

If the application is monitoring the ambient temperature, then the largest factor contributing to inaccuracy is the junction-to-ambient differential temperature, also discussed in Section 4, “General Thermal Considerations.” This can be accounted for to a certain extent if the application can estimate power dissipation at points in time when the temperature is sensed. One method of accounting for the differential is to always measure the temperature with a consistent configuration and to use the same configuration during calibration. Configuration in this context means internal activity, supply voltage, and output driver loading.

2.3.7 Device Temperature Gradient

The T_J sensed is the temperature at the physical location of the device temperature sensor circuit. Note that temperature can vary across the die. This temperature will be highest in the region of active outputs driving into low impedances.

3 Using the High Temperature Interrupt

3.1 Configuration

The VREGHTCL register (see Section 2.1.1, “Temperature Sensor Control Register VREGHTCL”) includes an interrupt enable bit (HTIE), an interrupt flag (HTIF), and a status bit (HTDS). When HTIE is set, an interrupt is requested each time the HTIF bit is set, which occurs both on assertion and deassertion of the HTDS bit. The HTDS bit is set when the temperature exceeds the assert level (T_{HTIA}) and cleared when the temperature drops below the deassert level (T_{HTID}). The HTIF flag is set if HTDS has changed state. After HTIF is set, it can only be cleared by writing a 1 to the bit position or by a reset.

The VREGHTTR register (see Section 2.1.2, “High Temperature Trimming Register VREGHTTR”), allows trimming of the VREG temperature sensor offset. It applies a constant offset to the V_{HT} voltage. This allows the HTI temperature to be shifted from $T_{HTI}(u)$ to $T_{HTI}(t)$ so that the HTI can be adjusted to a particular temperature, as shown in Figure 5.

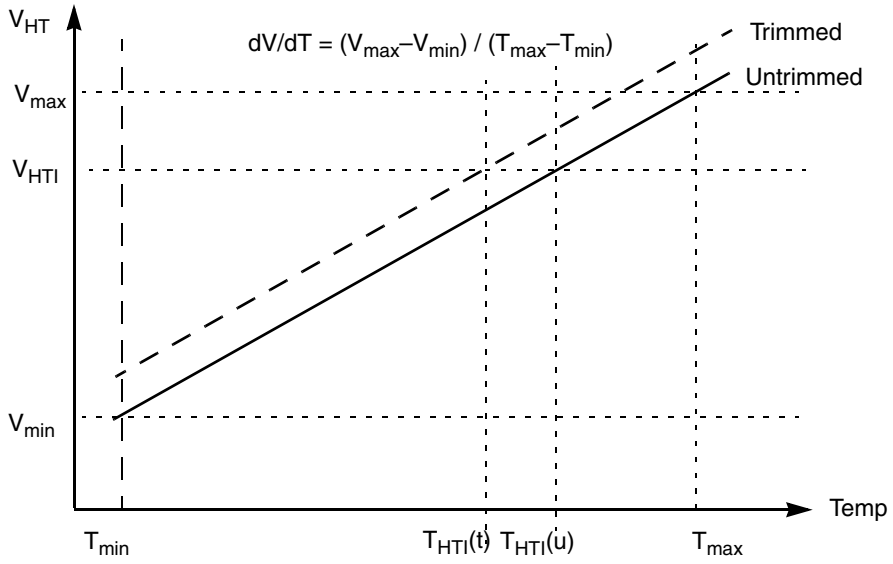

Figure 5. HTI Trimming Effect

The same offset applies to both assert and deassert levels. Hysteresis is guaranteed by design and inherent in the T_{HTIA} and T_{HTID} electrical specification (See Appendix A).

The contents of the trimming register are loaded with 0x0F from an information row location of the flash memory in the reset phase. This information row address is not accessible in an application. Thus to adjust trimming, VREGHTTR must be configured by the application software. Each positive trim step typically corresponds to 5 °C reduction in the HTI level. Therefore it is possible to trim from an assert level above 140 °C to an assert level below 110 °C.

3.2 HTI Calibration and Application

General calibration considerations described in Section 2.2, “Calibration,” also apply here.

To set the HTI level to the desired temperature:

1. Increase the temperature to the target temperature.
2. Set the trim value to VREGHTTR=0x80 (untrimmed).
3. Write a 1 to HTIF to clear it.

If HTIF is immediately set again, then the desired HTIF temperature lies out of operating range. If HTIF is not immediately set again, then increment the trim level, checking HTIF after each step. Repeat this until the interrupt flag is set, then store the trim value in NVM.

At a given temperature, the V_{HT} variation with respect to supply voltage is typically less than 5 mV over V_{DDA} operating voltage range. The slight, positive offset can be accounted for during calibration if necessary.

If the device is to be used in an application with a wide range of possible V_{DDA} supply voltages, the device can be calibrated at both the highest and lowest supply voltages. But in this case, the application must allow a measurement of the V_{DDA} supply voltage to determine whether adjustment is required due to supply voltage variations. This requires a V_{RH} reference separate from the V_{DDA} supply, which, in most applications, is not generally available.

The HTI feature is typically used to indicate that the junction temperature is near the maximum operating temperature. This allows the application to react by disabling features to reduce power consumption and prevent exceeding the maximum temperature. Effective ways of reducing the power consumption are by switching off ports driving low impedance loads and reducing the bus frequency using the PLL.

Because temperature changes are slow relative to processing routines, in many applications it would be sufficient to poll HTIF as an alternative to using the interrupt.

4 General Thermal Considerations

The temperature sensed is the device junction temperature, which differs from the ambient temperature. The differential depends on device activity, whereby high activity and high output drive load currents cause a larger differential between ambient and junction temperature.

4.1 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. It must be assured that the maximum operating junction temperature is not exceeded. The junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

where P_{INT} is the chip internal power:

$$P_{INT} = I_{DDR} \times V_{DDR} + I_{DDA} \times V_{DDA}$$

$$P_{IO} = \sum_{i} R_{DSON} \times I_{IO_i}^{2}$$

I_{IO} is the sum of all output currents on I/O ports associated with V_{DDX}, whereby

$$R_{DSON} = \frac{V_{OL}}{I_{OL}} \text{ ; for outputs driven low}$$

$$R_{DSON} = \frac{V_{DD35} - V_{OH}}{I_{OH}} \text{ ; for outputs driven high}$$

For more information, refer to the device reference manual electrical parameter section. As an example, the thermal resistance for the S12XEP100 device in LQFP144 is given in Table 6.

Table 6. Thermal Package Characteristic Example for S12XEP100

C	Rating	Symbol	Min	Typ	Max	Unit
D	Thermal resistance LQFP144, single sided PCB	θ_{JA}	—	—	41	°C/W
D	Thermal resistance LQFP144, double sided PCB with 2 internal planes	θ_{JA}	—	—	32	°C/W

For this device and package running at V_{DDR} = 5 V with I_{DDR} = 40 mA then P_{INT} = 200 mW, given that P_{IO} = 100 mW, P_D = 300 mW. Then at T_A = 100 °C on a single-sided PCB,
T_J = 100 + (0.3 x 41) = 112 °C.

For this device and package running at V_{DDR} = 5 V with I_{DDR} = 40 mA then P_{INT} = 200 mW, given that P_{IO} = 100 mW, P_D = 300 mW. Then at T_A = 100 °C on a double-sided PCB,
T_J = 100 + (0.3 x 32) = 109.6 °C.

Appendix A Electrical Parameters

Table A-1. S12XE-Family Temperature Sensor Parameter Table

Class	Description	Symbol	Min	Typ	Max	Unit
T	Temperature Sensor Slope	dV_{TS}	5.05	5.25	5.45	mV/°C
T	High Temperature Interrupt Assert (VREGHTTR=$88)[1] High Temperature Interrupt Deassert (VREGHTTR=$88)	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C

1 A hysteresis is guaranteed by design.

Appendix B Code Examples

B.1 Read Temperature

An example of code to read the temperature is shown here. The converted and averaged V_{HT} is stored to TempRes+16.
This same code can be used in the dV/dT calibration process with the minimum and maximum values from TempRes+16 stored in NVM for future use.

```
TempRes     ds.w 9
ReadTemp    MOVB  #$18,VREGHTCL
            MOVB  #$4F,ATD0CTL1 ; Configure for 12-bit ATD resolution
            MOVB  #$C0,ATD0CTL3 ; DJM set, right aligned to avoid overflow
            MOVB  #$41,ATD0CTL5 ; Start Conversion ADC0[17] 1 sequence
            LDX   #ATD0DR0
            LDY   #TempRes
            CLRA
            CLRB
SCF         BRCLR ATD0STAT0,#$80,SCF   ; Wait For SCF
NextTRes    ADDD  X
            MOVW  2,X+,2,Y+
            CPX   #ATD0DR9
            BNE   NextTRes
            LSRD                       ; Rough Average of 8 readings
            LSRD
            LSRD
            STD   TempRes+16
EndCal      RTS                   ; ReadTemp
```

B.2 Calibrate HTI

First heat the device to the desired HTI temperature, then execute the following code.
The trim value for the required temperature is stored at HTItrim. This must be moved to an NVM location for future use (NVM programming not shown here).

```
HTItrim     ds.w 1
HTICal MOVB  #$80,VREGHTTR    ; Initialise trim
            MOVB  #$19,VREGHTCL    ; Clear HTIF
Trimadj     LDAB  VREGHTCL
            ANDB  #$01
            BNE   HTIFSet          ; If HTIF set store trim value to RAM
            INC   VREGHTTR         ; Adjust trim
            LDAA  VREGHTTR
            CMPA  #$8F
            BEQ   Error1           ; No HTI level found
            BRA   Trimadj          ; Try next trim setting
HTIFSet     MOVB  VREGHTTR,HTItrim
End         BRA   *
Error1      BRA   *                ; No HTI detected
```

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Document Number: AN3624
Rev. 0
04/2008

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