



Migrating from the MC9S08QE32 to the MCF51QE32

and other MCF51QE and MC9S08QE devices

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From the RS08 to our highest performance ColdFire® V4 devices, the Controller Continuum provides compatibility for an easy migration path up or down the performance spectrum. The connection point on the Controller Continuum is where complementary families of S08 and ColdFire V1 microcontrollers share a common set of peripherals and development tools to deliver the ultimate in migration flexibility. Pin-for-pin compatibility between many Flexis devices allows controller exchanges without redesigning the board.

The term Flexis means a single development tool to ease migration between 8-bit and 32-bit — a common peripheral set to preserve software investment between 8-bit and 32-bit, and pin compatibility wherever practical to maximize hardware reuse when moving between 8-bit and 32-bit.

Freescale provides the MC9S08QE32 as a lower cost, lower performance alternative to the MCF51QE32 device.

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Flexis QE Family Features Comparison

This document introduces QE32 users to the differences between these two devices and the differences between these and the other QE Flexis family members. This application note does not describe in detail how to use new features of the MC9S08QE32. Consult the specific MCU reference manuals for more detailed programming and design information.

NOTE

With the exception of mask set errata documents, if any other Freescale document contains information that conflicts with the information in the device reference manual, the reference manual should be considered to have the most current and correct data.

1 Flexis QE Family Features Comparison

There are five main products in the Flexis QE family:

- MCF51QE128
- MC9S08QE128
- MCF51QE32
- MC9S08QE32
- MC9S08QE8

Differences between these and the 96K, 64K, 16K, and 4K derivatives are detailed in the device reference manuals and are not discussed in this document.

[Table 1](#) compares the five main Flexis QE family devices' feature sets.

NOTE

The term “Up to”, used in the table signifies that the number of modules, channels, or pins is package dependent — the smaller the package, the fewer features are available.

Port I/O count does not include the output-only PTA4 or input-only PTA5 pins.

Table 1. Flexis QE Family Feature Comparison

	MCF51QE128	MC9S08QE128	MCF51QE32	MC9S08QE32	MC9S08QE8
Core	ColdFire V1	HCS08	ColdFire V1	HCS08	HCS08
Flash Size	128K	128K	32K	32K	8K
RAM Size	8K	8K	8K	2K	512
Debugger	CF Debug	DBG & BDC	CF Debug	DBG & BDC	DBG & BDC
Pin Quantity	Up to 80	Up to 80	Up to 64	Up to 48	Up to 32
ACMP	2	2	2	2	Up to 2
ADC	Up to 24ch	Up to 24ch	20ch	10ch	Up to 10ch
ICS	Yes	Yes	Yes	Yes	Yes

Table 1. Flexis QE Family Feature Comparison

	MCF51QE128	MC9S08QE128	MCF51QE32	MC9S08QE32	MC9S08QE8
I ² C	2	Up to 2	2	1	1
KBI	16	16	16	Up to 16	8
Port I/O	Up to 70	Up to 70	Up to 54	Up to 38	Up to 26
Rapid GPIO	Yes	No	Yes	No	No
COP Watchdog	Yes	Yes	Yes	Yes	Yes
RTC	Yes	Yes	Yes	Yes	Yes
SCI	2	2	2	2	1
SPI	2	2	2	1	1
Interrupt Controller	Yes	No	Yes	No	No
External IRQ	Yes	Yes	Yes	Yes	Yes
LVD	Yes	Yes	Yes	Yes	Yes
TPM	3+3+6ch	3+3+6ch	3+3+6ch	3+3+6ch	Up to 3+3ch
XOSC	Yes	Yes	Yes	Yes	Yes

1.1 Generic ColdFire Versus HCS08 Device Differences

There are three architectural differences between the ColdFire V1 and HCS08 devices that the programmer or designer must consider.

1.1.1 Core and Debugger

The ColdFire core executes instructions at the CPU frequency (2 x bus frequency), whereas the S08 core executes instructions at bus frequency (0.5 x CPU frequency). This difference enables a performance improvement from S08 to ColdFire but means that cycle counting based software routines should be avoided to maintain compatibility. The core and the debugger differences are managed by the CodeWarrior[®] environment through the MCU Change Wizard, as described in AN3465 “Migrating within the controller continuum”.

1.1.2 Rapid I/O

The HCS08 devices do not have the Rapid I/O module on chip. The port I/O on the 9S08QE128 device have port SET, CLEAR and TOGGLE registers, which reclaim the Rapid I/O functions. These features are available on Port C and Port E. The 9S08QE32 and 9S08QE8 do not have these registers; however, the function can be achieved through software.

	S08 I/O Standard	S08 I/O Extended	ColdFire V1 RGPIO
Enable	Set port/pin as output	Set port/pin as output	RGPIO_ENB = 0xFFFF; RGPIO_DIR = 0xFFFF;
Set	BitMask = 0xhh; PTxD = BitMask;);	PTxSET = 0xhh;	RGPIO_SET = 0xhhhh;
Clear	BitMask = 0xhh; PTxD &= (~BitMask);	PTxCLR = 0xhh;	RGPIO_CLR = 0xhhhh;
Toggle	BitMask = 0xhh; PTxD ^= BitMask;	PTxTOG = 0xhh;	RGPIO_TOG = 0xhhhh;

Notes:

“h” is hexadecimal number

BitMask is a local variable - unsigned char BitMask

1.1.3 Interrupt Controller

The interrupt controller on the ColdFire V1 family derivatives have support for up to 256 interrupt/reset exceptions. However, only 39 are used on MCF51QE128 and MCF51QE32. Exception priorities are fixed; however, up to two interrupts can be remapped to the highest maskable level and priority. This gives system designers more flexibility to escalate critical application issues.. There are seven levels of interrupt grouping and hardware support for interrupt nesting. To enable all possible interrupts, as with the HCS08 devices, the interrupt wakeup control register enable bit, INTC_WCR bit 7, must be set. This is not managed by the MCU Change Wizard or the use of the EnableInterrupts macro.

The CPU on the HCS08 family derivatives supports up to 32 interrupt/reset exceptions. Exception priorities are fixed; there is one level of interrupt grouping and no hardware support for nesting. This feature is turned on and off via the I bit in the CPU’s condition code register (CCR), and specific module interrupts are switched on and off in the module registers.

2 MC9S08QE32 and the MCF51QE32

The 8-bit and 32-bit QE32 devices cover the same portfolio space, but have many differences that the programmer or designer must consider. The main differences are emphasized using bold text in [Table 2](#).

Table 2. QE32 Devices Comparison

	MCF51QE32		MC9S08QE32	
	Feature	Detail	Feature	Detail
Core	ColdFire V1	-	HCS08	-
Flash Size	32K	32 pages of 1K bytes	32K	64 pages of 512 bytes
RAM Size	8K	1:4 ratio	2K	1:16 ratio
Debugger	ColdFire Debug	-	DBG and BDC	-

Table 2. QE32 Devices Comparison (continued)

	MCF51QE32		MC9S08QE32	
	Feature	Detail	Feature	Detail
Pin Quantity	64	64 LQFP	Up to 48	48-pin QFN 44-pin LQFP 32-pin LQFP 28-pin SOIC
ACMP	2	Output can connect to TPM Input Capture channel	2	Output can connect to TPM Input Capture channel
ADC	20ch	8, 10 or 12-bit resolution	10ch	8, 10 or 12-bit resolution
ICS	Yes	-	Yes	-
I²C	2	Compatible with I ² C bus standard	1	Compatible with I ² C bus standard
KBI	16	PTA0-3, PTB0-3, PTD0-7	Up to 16	PTA0-3, PTB0-3, PTD0-7 Number is package dependent
Port I/O	54	Number is package dependent	Up to 38	Number is package dependent
Rapid GPIO	Yes	-	No	-
COP Watchdog	Yes	LPO or Bus driven	Yes	LPO or Bus driven
RTC	Yes	With ADC Trigger	Yes	With ADC Trigger
SCI	2	-	2	-
SPI	2	No Filters on Inputs	1	SPI Ports Input Filter Enable
Interrupt Controller	Yes	-	No	Interrupts managed by CPU
External IRQ	Yes	-	Yes	-
LVD	Yes	-	Yes	-
TPM	3+3+6ch	16-bit	3+3+6ch	16-bit
XOSC	Yes	-	Yes	-

2.1 Memory

2.1.1 Flash

The MCF51QE32 Flash memory is arranged in 32 pages (also referred to as sectors) of 1024 bytes. The MC9S08QE32 Flash memory is arranged in 64 pages of 512 bytes. Flash “Read while Write” is not supported on either device due to each device having a single flash array. The “read while write” feature requires at least two arrays so that one can be programmed while running code.

2.1.2 RAM

There is a significant difference between the RAM sizes on the two devices. The MCF51QE32 has 8K bytes of RAM on chip, whereas the MC9S08QE32 has 2K. All other RAM features and functions are the

same. The ColdFire core accesses RAM at the CPU frequency, whereas the S08 core accesses RAM at the bus frequency, in line with the respective core’s instruction speed; this does not cause any code compatibility issues.

2.2 Package

The MCF51QE32 is a 64-pin LQFP packaged part with 54 general purpose I/O, one input-only pin (PTA5), and one output-only pin (PTA4). The MC9S08QE32 is available in 48-pin QFN, 44-pin LQFP, 32-pin LQFP, and 28-pin SOIC packages with 38, 34, 26 and 22 I/O respectively, one input-only pin (PTA5), and one output-only pin, PTA4.

	MC9S08QE32				MC9S08QE128			
Package	48-pin QFN	44-pin LQFP	32-pin LQFP	28-pin SOIC	80-pin LQFP	64-pin LQFP	48-pin QFN	44-pin QFP
I/O	38	34	26	22	70	54	38	34
Input Only	PTA5	PTA5	PTA5	PTA5	PTA5	PTA5	PTA5	PTA5
Output Only	PTA4	PTA4	PTA4	PTA4	PTA4	PTA4	PTA4	PTA4

Although the packages are not compatible, the common functions are relatively located on the devices as shown in Figure 1. The inner green section shows the S08 peripheral mapping; the outer grey section shows the ColdFire mapping. The peripherals are located on the same sides at relatively the same locations, making layout of the PCB relatively simple.

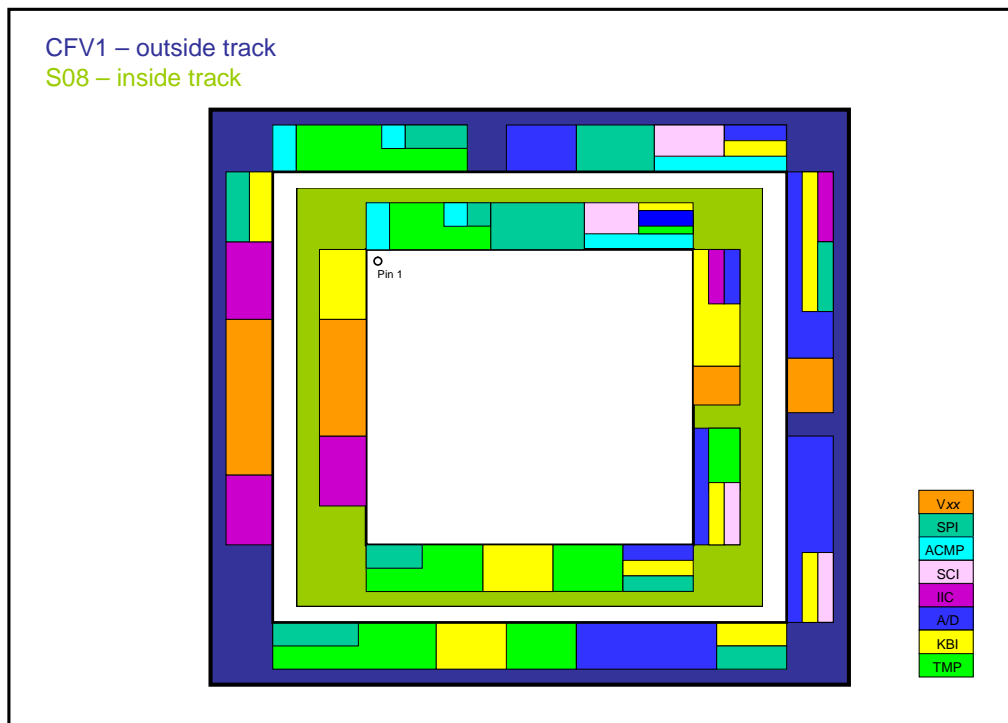


Figure 1. MCF51QE32 and MC9S08QE32 Pin Placement

2.3 Modules

In general terms, the modules on the two devices are the same; however, a few minor differences exist in some of the modules. The following differences are taken from the reference manual. You are advised to refer also to the relevant device mask set errata documents for any other differences.

2.3.1 ADC

The ADC on the MC9S08QE32 has ten fewer channels than the MCF51QE32 — 10 channels versus 20 channels. The resolution options, clock sources, functions, and registers are otherwise the same.

2.3.2 I²C

The MC9S08QE32 has only one I²C module on chip, whereas the MCF51QE32 has two.

2.3.3 SPI

The MC9S08QE32 has only one SPI module on chip, whereas the MCF51QE32 has two.

One other difference exists between the two SPIs — the MC9S08QE32 SPI has a filter on the port pins to protect the SPI from noise during data transfers; this restricts the maximum baud rate to 5 MHz. By default, the input filters on the SPI port pins are enabled. The SPI Ports Input Filter Enable bit (SPIFE) in the SOPT2 register can disable the use of this filter if higher baud rates are required.

3 MC9S08QE32 and the MC9S08QE128

The MC9S08QE32 and the MC9S08QE128 are both 8-bit devices with many similarities; however, there are some important differences that the programmer or designer must consider. The main differences are emphasized using bold text in [Table 3](#).

Table 3. S08QE32 to S08QE32 Device Comparison

	MC9S08QE32		MC9S08QE128	
	Feature	Detail	Feature	Detail
Core	HCS08	-	HCS08	-
Flash Size	32K	64 pages of 512 Bytes	128K	256 pages of 512 Bytes
RAM Size	2K	1:16 ratio	8K	1:16 ratio
Debugger	DBG and BDC	-	DBG and BDC	-
Pin Quantity	Up to 48	48-pin QFN 44-pin LQFP 32-pin LQFP 28-pin SOIC	Up to 80	80-pin LQFP 64-pin LQFP 48-pin QFN 44-pin QFP
ACMP	2	Output can connect to TPM Input Capture Channel	2	Output can connect to TPM Input Capture Channel
ADC	10ch	8, 10 or 12-bit resolution	Up to 24ch	8, 10 or 12-bit resolution

Table 3. S08QE32 to S08QE32 Device Comparison (continued)

	MC9S08QE32		MC9S08QE128	
	Feature	Detail	Feature	Detail
ICS	Yes	-	Yes	-
I ² C	1	Compatible with I ² C bus standard	Up to 2	Compatible with I ² C bus standard. Number is package dependent
KBI	Up to 16	PTA0-3, PTB0-3, PTD0-7 Number is package dependent	16	-
Port I/O	Up to 38	Number is package dependent	Up to 70	Number is package dependent
Rapid GPIO	No	-	No	-
COP Watchdog	Yes	LPO or Bus driven	Yes	LPO or Bus driven
RTC	Yes	With ADC Trigger	Yes	With ADC Trigger
SCI	2	-	2	-
SPI	1	SPI Ports Input Filter Enable	2	SPI Ports Input Filter Enable
Interrupt Controller	No	Interrupts managed by CPU	No	Interrupts managed by CPU
External IRQ	Yes	-	Yes	-
LVD	Yes	-	Yes	-
TPM	3+3+6ch	16-bit	3+3+6ch	16-bit
XOSC	Yes	-	Yes	-

3.1 Memory

3.1.1 Flash

The MC9S08QE32 Flash memory is arranged in one array of 64 pages of 512 bytes; the MC9S08QE128 Flash memory is arranged in two arrays of 128 pages of 512 bytes. Flash “Read while Write” is not supported on the QE32 device, due to the Flash being one single array. Flash “Read while Write” is supported on the QE128 due to the presence of two separate arrays.

3.1.2 RAM

There is a significant difference between the RAM sizes on the two devices; however the RAM to flash ratio remains the same (1:16). The MC9S08QE32 has 2K of RAM on chip, whereas the MC9S08QE128 has 8K. All other RAM features and functions are the same.

3.2 Package

The MC9S08QE32 is available in 48-pin QFN, 44-pin LQFP, 32-pin LQFP, and 28-pin SOIC packages with 38, 34, 26 and 22 I/O, respectively. The MC9S08QE128 is available in 80-pin LQFP, 64-pin LQFP,

48-pin QFN, and 44-pin QFP packages, with 70, 54, 38 and 34 I/O, respectively. Both devices have one input-only pin (PTA5) and one output-only pin (PTA4).

	MCF51QE32	MC9S08QE32			
Package	64-pin LQFP	48-pin QFN	44-pin LQFP	32-pin LQFP	28-pin SOIC
I/O	54	38	34	26	22
Input Only	PTA5	PTA5	PTA5	PTA5	PTA5
Output Only	PTA4	PTA4	PTA4	PTA4	PTA4

The MC9S08QE32 48-pin QFN package and the MC9S08QE128 48-pin QFN package are compatible.

3.3 Modules

In general terms, the modules on the two devices are the same; however, a few minor differences exist. The differences discussed below are taken from the reference manual. You are advised to refer also to the relevant device mask set errata documents for any other differences.

3.3.1 ADC

The ADC on the MC9S08QE32 has ten channels; the MC9S08QE128 has up to 24 channels, depending on the package option chosen. The MC9S08QE128 90-pin LQFP has 24 channels; the 64-pin LQFP 22 channels; the 48-pin QFN and 44-pin QFP both have ten channels.

The resolution options, clock sources, functions, and registers are otherwise the same.

3.3.2 I²C

The MC9S08QE32 has one I²C module on chip, whereas the MC9S08QE128 may have up to two, depending on the package option.

The MC9S08QE128 90-pin LQFP and the 64-pin LQFP have two I²C modules; the 48-pin QFN and the 44-pin QFP have only one.

3.3.3 KBI

The MC9S08QE32 may have up to sixteen keyboard interrupts (KBI) on chip, depending on the package option. The MC9S08QE128 has sixteen KBI on chip, regardless of the package option chosen.

3.3.4 SPI

The MC9S08QE32 has one SPI module on chip, whereas the MC9S08QE128 has two.

4 MC9S08Q32 and the MC9S08QE8

The MC9S08QE32 and the MC9S08QE8 are both 8-bit devices with many similarities; however, there are some important differences that the programmer or designer must consider. The main differences are emphasized using bold text in [Table 4](#).

Table 4. S08QE8 and S08QE8 Device Comparison

	MC9S08QE32		MC9S08QE8	
	Feature	Detail	Feature	Detail
Core	HCS08	-	HCS08	Limited to 10 MHz bus/ 20 MHz CPU
Flash Size	32K	64 pages of 512 Bytes	8K	16 pages of 512 Bytes
RAM Size	2K	1:16 ratio	512	1:16 ratio
Debugger	DBG and BDC	-	DBG and BDC	-
Pin Quantity	Up to 48	48-pin QFN 44-pin LQFP 32-pin LQFP 28-pin SOIC	Up to 32	32-pin LQFP 28-pin SOIC 20-pin SOIC 16-pin PDIP 16-pin TSSOP
ACMP	2	Output can connect to TPM Input Capture Channel	Up to 2	Output can connect to TPM Input Capture Channel
ADC	10ch	8, 10 or 12-bit resolution	Up to 10ch	8, 10, 12 bit resolution 12-bit resolution availability package dependent.
ICS	Yes	-	Yes	DCOL multiplier only
I ² C	1	Compatible with I ² C bus standard	1	Compatible with I ² C bus standard
KBI	Up to 16	PTA0-3, PTB0-3, PTD0-7 Number is package dependent	8	PTA0-3, PTB0-3
Port I/O	Up to 38	Number is package dependent	Up to 26	Number is package dependent
Rapid GPIO	No	-	No	-
COP Watchdog	Yes	LPO or Bus driven	Yes	LPO or bus driven
RTC	Yes	With ADC Trigger	Yes	With ADC Trigger
SCI	2	-	1	-
SPI	1	SPI Ports Input Filter Enable	1	SPI Ports Input Filter Enable
Interrupt Controller	No	Interrupts managed by CPU	No	Interrupts managed by CPU

Table 4. S08QE8 and S08QE8 Device Comparison

	MC9S08QE32		MC9S08QE8	
	Feature	Detail	Feature	Detail
External IRQ	Yes	-	Yes	-
LVD	Yes	-	Yes	Low Trip/Warning points only
TPM	3+3+6ch	16-bit	Up to 3+3ch	16-bit
XOSC	Yes	-	Yes	-

4.1 Memory

4.1.1 Flash

The MC9S08QE32 Flash memory is arranged in 64 pages of 512 bytes; the MC9S08QE8 Flash memory is arranged in 16 pages of 512 bytes. Flash “Read while Write” is not supported on either device, due to the NAND Flash used in both technologies and to the Flash being one single module.

4.1.2 RAM

There is a difference between the RAM sizes on the two devices. The MC9S08QE32 has 2K of RAM on chip, whereas the MC9S08QE128 has only 512 bytes. All other RAM features and functions are the same.

4.2 Package

The MC9S08QE32 is available in 48-pin QFN, 44-pin LQFP, 32-pin LQFP, and 28-pin SOIC packages, with 38, 34, 26 and 22 I/O, respectively. The MC9S08QE8 is available in 32-pin LQFP, 28-pin SOIC, 20-pin SOIC, 16-pin PDIP/TSSOP packages, with 26, 22, 16 and 12 I/O, respectively. Both devices have one input-only pin (PTA5) and one output-only pin (PTA4).

Package	MC9S08QE32				MC9S08QE8			
	48-pin QFN	44-pin LQFP	32-pin LQFP	28-pin SOIC	32-pin LQFP	28-pin SOIC	20-pin SOIC	16-pin PDIP/TSSOP
I/O	38	34	26	22	26	22	16	12
Input Only	PTA5	PTA5	PTA5	PTA5	PTA5	PTA5	PTA5	PTA5
Output Only	PTA4	PTA4	PTA4	PTA4	PTA4	PTA4	PTA4	PTA4

The MC9S08QE32 28-pin SOIC package and the MC9S08QE8 28-pin SOIC package are compatible.

4.3 Modules

In general terms, the modules on the two devices are the same; however a few minor differences exist. The differences discussed below are taken from the reference manual. You are advised to refer also to the relevant device mask set errata documents for any other differences.

4.3.1 ACMP

There are two analog comparators (ACMP) on the MC9S08QE32, whereas the MC9S08QE8 can have up to two, depending on the package option chosen.

The MC9S08QE8 32-pin LQFP and the 28-pin SOIC packages have two ACMPs; the 20-pin SOIC and the 16-pin PDIP/TSSOP packages have one.

4.3.2 ADC

The analog to digital converter (ADC) on the MC9S08QE32 has ten channels, whereas the MC9S08QE128 can have up to ten channels, depending on the package option chosen. The MC9S08QE8 32-pin LQFP and the 28-pin SOIC packages have ten channels, whereas the 20-pin SOIC and the 16-pin PDIP/TSSOP packages have only eight channels.

In addition, the maximum resolution available on the 32-pin LQFP and 28-pin SOIC packages is 12-bit; the maximum resolution on the 20-pin SOIC and the 16-pin PDIP/TSSOP packages is only 10-bit.

4.3.3 KBI

The MC9S08QE32 may have up to sixteen keyboard interrupts (KBI) on chip, depending on the package option chosen. The MC9S08QE8 has only eight KBI on chip.

4.3.4 SCI

The MC9S08QE32 has two SCI modules on chip, whereas the MC9S08QE8 has one.

4.3.5 TPM

The MC9S08QE32 has one 6-channel and two 3-channel timer/pulse width modulators (TPM) on chip; the MC9S08QE8 has two 3-channel TPMs on chip.

4.3.6 ICS

As the QE8 is limited to 10 MHz bus frequency, the ICS module supports only the DCOL (512) multiplier range, whereas the QE32 supports DCOL, M and H up to 25.165 MHz bus frequency.

4.3.7 LVD

The QE8 device LVD system has only the low trip (1.84V) and warning (2.14V) levels. The QE32 device supports both High and Low warning and trip levels in all combinations.

5 Further Reading

The following documents can be obtained from <http://www.freescale.com>.

1. AN3460 — *Low-Power Design Enabled by MC9S08QE128 and MCF51QE128 Microcontrollers*
2. AN3465 — *Migrating within the controller continuum*
3. QE128COMPWP — *Comparison of MC9S08QE128 and MCF51QE128 Microcontrollers*
4. MCF51QE128RM — *MCF51QE128 Reference Manual*
5. BRQE128OVRV — *Controller Continuum Brochure*

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