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Application Note

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MPC567xF/MPC5676R Hardware Requirements/Example Circuits

Including Operation of the On-Chip Regulators and Regulator Controller

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Contents

1 Introduction 1
2 MPC567xF/MPC5676R package options overview 2
3 Power supply options 3
4 Hardware system requirements for oscillator 23
5 Device reset configuration 26
6 Recommended debug connectors and connector pin out definitions 33
7 Monitoring internal analog signals 37
8 eQADC overview 38
9 Example communication peripheral connections 46
10 Pin Overview 66
A Summary of recommended power supply bypass capacitors 70
B MPC567xF and MPC5676R ADC Input Model 71
C References 72
D Revision History 73

1 Introduction

The MPC567xF[1] and the MPC5676R are advanced microcontrollers initially intended for automotive powertrain applications. They are both based on the e200z7 Power Architecture® core. The core has a maximum operating frequency of 264 MHz (nominal). The MPC567xF is a single e200z760 core based MCU and the MPC5676R is a dual e200z759 core MCU that runs up to 180 MHz (nominal) with all of the same peripheral as the MPC567xF devices. However, the MPC5676R has additional peripherals that are not available on the MPC567xF devices.

The MPC567xF and MPC5676R require multiple internal power supply voltages, but the device can run from a single 5 V power supply by generating the other voltages with internal regulators and an internal regulator controller. The major power supplies for the devices are 5 V for powering the internal regulator, the Analog to Digital Converter, and can be used for the pin input and output voltages. In addition, 3.3 V is required for the internal pad prebuffers and flash memory. The majority of the internal logic is powered by 1.2 V. The SRAM has a separate supply input for keep-alive features, if SRAM keep-alive functionality is required. 3.3 V and 1.2 V can be generated from the internal regulators and regulator controller.

1. MPC567xF refers to both the MPC5673F (3 MB Flash and 192 KB SRAM) and the MPC5674F (4 MB Flash and 256 KB SRAM). In addition to the MPC567xF devices, this document also covers the MPC5676R.

If using the external bus or external debug trace features or if any of the pin input/output segments require 3.3 V, an external 3.3 V supply is also required.

This application note shows the options of the MPC567xF and MPC5676R power supplies and the correct external circuitry required:

- Power supplies, including digital supplies, analog supplies, SRAM standby supply, and phase-locked loop supply
- Proper configuration of the PLL circuitry
- Other major external hardware required for the device
- Examples of other common external interfaces for communication physical devices, as well as typical analog circuitry
- Handling of injection current, including requirements for power supply ramp rates

2 MPC567xF/MPC5676R package options overview

The MPC567xF is available in three package options. The MPC5676R is available in two package options. All of the packages are Thermally Enhanced Plastic Ball Grid Arrays (TEPBGA). The table below shows the different packages that are available and the primary features that are different from the 416 TEPBGA standard package.

Table 1. MPC567xF/MPC5676R Package Options

Package	MPC567xF	MPC5676R	Feature differences due to the package
416 TEPBGA	√	√	Primary device with the base features of the device. No development bus (including no CLKOUT). BOOTCFG0 not available since there is no external bus from which to boot.
516 TEPBGA	√	√	All of the features of the 416 TEPBGA package with the addition of access to the development bus (External Bus Interface).
324 TEPBGA[1]	√		Same basic features of the 416 TEPBGA package except: • Reduced number of eTPU channels as the primary pin function on both eTPU's (eighteen channels fewer) • No "shared" ADC channels (AN24:39, sixteen channels fewer) • Reduced number of GPIO pins (five dedicated GPIO fewer) • Reduced number of DSPI chip selects as primary pin function (thirteen SPI chip selects fewer) • Reduced number of eMIOS channels as primary pin function (one fewer) • No BOOTCFG0 or WKPCFG pins • No eSCI pins as primary function are available; only eSCI A signals are available as alternate functions on other pins • Limited to a frequency of 200 MHz (due to thermal issues)

1. The MPC5676R is not available in the 324 TEPBGA package.

The decision of which package to use should be based on the number of input/output pins required for the application, whether the external bus is required in the system, and the area available for the target system. The following table shows the package size differences of the packages. See the device data sheet for complete package dimensions and ball placement. Drawings are also available on the Freescale web site; search for the case outline number shown in the table.

Table 2. Package Sizes

Package	Physical Size	Case Outline	Configuration
324 TEPBGA	23 mm x 23 mm	1158-3	1 mm ball pitch with four outer rows of balls with a center section of balls for thermal enhancement and power supplies
416 TEPBGA	27 mm x 27 mm	1494-01	1 mm ball pitch with four outer rows of balls with a center section of balls for thermal enhancement and power supplies
516 TEPBGA	27 mm x 27 mm	1164A-01	1 mm ball pitch with six outer rows of balls with a center section of balls for thermal enhancement and power supplies; outermost and innermost rows are not fully populated

The next figure provides a picture comparison of the different packages and ball configurations.

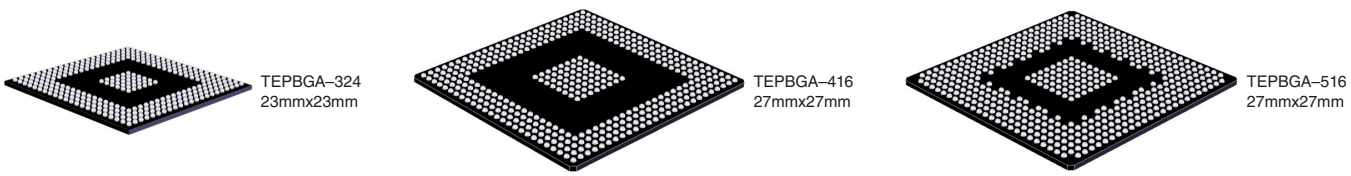


Figure 1. TEPBGA Packages (324, 416, and 516)

NOTE

This document uses the terms pins, balls, and pads interchangeably when referencing the external signals of the device.

3 Power supply options

The MPC5674F and MPC5676R MCUs are designed for a wide range of applications. Based on system requirements and available power supplies, some applications may require different methods of powering the device. The table below summarizes the options available for powering the MCUs. Two options require only a single 5 V supply and a few external components to power the MCUs. The MCU will generate its own 1.2 V and 3.3 V supplies. The final option is to provide 5 V, 3.3 V, and 1.2 V from an external power supply. Other options are available that use combinations of the internal and external power supplies.

NOTE

The overall power dissipation of the MPC5674F and the MPC5676R are approximately the same. However, the latest device data sheet should be consulted. The MPC5676R contains two cores and an extra eTPU, but operates up to a lower frequency (180 MHz nominal frequency) than the MPC567xF devices (264 MHz nominal operating frequency).

NOTE

The 1.2V regulator controller requires external circuitry when used. The 3.3V regulator is completely internal, with the exception of requiring external bypass capacitor.

Table 3. MPC567xF and MPC5676R power supply options

Configuration	Mode Name	3.3 V Supply	1.2 V regulator controller	REGSEL	VDDREG	Reference
Internal 3.3 V regulator with 1.2 V linear regulator controller	LDO5V	Internal regulator	Internal linear mode	Low/GND	5 V	See Using the internal regulator and regulator controller
Internal 3.3 V regulator with 1.2 V SMPS[1] regulator controller	SMPS5V	Internal regulator	Internal SMPS	VDDREG	5 V	
External 3.3 V regulator with internal 1.2 V linear regulator controller	LDO3V	External	Internal linear mode	Low/GND	External 3.3 V supply	See Using internal and external supplies
External supplies with on-chip low voltage detect	External[2]	External	External supply	Low/GND	External 3.3 V supply	See Using external supplies
External Supplies, except VDD33 powered by internal regulator[3]	External	External/ internal	External Supply	Low/GND	5 V	See Internal linear 3.3 V regulator
Mixed internal and external[4]	LDO5V or SMPS5V with additional external 3.3 V supply	External for VDDEHx, Internal VDDSYN supply powers VDD33	Internal linear or SMPS	Low/GND or VDDREG[5]	5 V	See Using the internal regulator and regulator controller

1. Switch Mode Power Supply (SMPS).
2. This mode is the same as LDO3V, except the internal low voltage (1.2 V) regulator controller is not used.
3. This option allows the use of the external power supplies, except that it allows the internal 3.3 V supply to power VDD33. It is highly recommended that VDD33 be powered by the internal 3.3 V regulator in all systems.
4. Primarily used when using the external development bus or Nexus trace.
5. REGSEL depends on whether the linear (low) or the SMPS mode controller will be used.

3.1 Power supply signals

The following table shows all pins related to the power supply. The nominal voltages are shown, the device data sheet should be referenced for the minimum and maximum voltages allowed on each of the pins.

Table 4. Power supply pins

	Pin name	Nominal voltage	Direction (relative to MCU)	Description
PLL supplies	VDDSYN	3.3 V	In or out[1]	PLL power supply — V_{DDSYN} is the power supply input for the FMPLL. It is also the 3.3 V regulator output, when enabled.
	VSSSYN	Ground	In	Return (ground) reference for the PLL.
Standby supply	VSTBY	1 V or 2 to 6 V	In	SRAM standby supply — V_{STBY} is the power supply input that is used to maintain a portion of the contents of internal SRAM during power-down. If not used, tie V_{STBY} to VSS.
Regulator pins	VDDREG	5 V or 3.3 V	In	VDD regulator input — source voltage for on-chip regulators and low-voltage detect circuits. Typically this should be 5 V, but in some cases 3.3 V can be supplied on this pin when using a 3.3V external supply (5 V is the preferred option).
	VDD33	3.3 V	In	VDD 3.3 V — supply for the IO pre-drivers and flash power supply. This pin should either be connected to VDDSYN (internal regulators enabled) or an external 3.3 V supply (internal supplies disabled).
	REGSEL	0 or VDDREG (5 V)	In	Regulator select determines the PMC regulator mode (linear/ switch mode). Low selects the linear 1.2 V regulator controller. High selects the SMPS 1.2 V regulator controller. If using the SMPS regulator, tie REGSEL to VDDREG.
	REGCTL	—	In	Regulator control is the output from the regulator that controls the external transistor for the 1.2 V regulator. In linear mode this is a current that is varied to change the gain of the external NPN transistor to hold a constant voltage on the transistor emitter (connected to the VDD signals). In SMPS mode this is a pulse width modulated (PWM) signal that drives the gate of an external N-MOSFET transistor. The duty cycle of the PWM is varied. The filter network, connected between the drain of the transistor and the VDD supply signals of the MCU, creates an analog DC voltage.
Internal Logic Supply	VDD	1.2 V	In	Internal voltage input — V_{DD} supplies the internal circuitry and can be powered by the 1.2 V internal regulator controller or an external 1.2 V supply.

Table continues on the next page...

Table 4. Power supply pins (continued)

	Pin name	Nominal voltage	Direction (relative to MCU)	Description
I/O Supplies	VDDEH1 VDDEH3 VDDEH4 VDDEH5 VDDEH6 VDDEH7	3.3 V or 5 V	In	"High Voltage" Input and Output Power Supply Input - V_{DDEHx} are the supplies for the high voltage input and output pins. Each segment can be set to different voltages if required (3.3 V or 5 V).
	VDDE2	3.3 V	In	"Low Voltage" Clock Output and Debug Supply Input - V_{DDE2} is the supply for the development debug port (Nexus trace, JTAG, and Engineering Clock [ENGCLK]) signals.
	VDDE8 VDDE9 VDDE10	3.3 V	In	V_{DDEn} are the supplies for the development bus signals (data, address, and control). These should be supplied from an external power supply.
Analog Supplies	VDDA_A0 VDDA_A1 VDDA_B0 VDDA_B1	5 V	In	Analog Power Supply Input — V_{DDAn} and V_{DDA_Bn} are the analog supply input pins for eQADC_A and eQADC_B.
	VSSA_A1 VSSA_B0	Ground	In	Analog Ground Return — V_{SS_An} and V_{SS_Bn} are the analog supply return pins for eQADC_A and eQADC_B.
	VRH_A VRH_B	5 V	In	Analog High Reference — V_{RH_A} and V_{RH_B} are the voltage reference high input pins for eQADC_A and eQADC_B.
	VRL_A VRL_B	Ground	In	Analog High Reference — V_{RL_A} and V_{RL_B} are the voltage reference low input pins for eQADC_A and eQADC_B.
	REFBYPCA REFBYPCB	Approximately 3.75 V (output)	Out	ADC Internal Reference Bypass Capacitor — REFBYPCA and REFBYPCB require external bypass capacitors pins for the eQADC 75% reference.
	REFBYPCA1 REFBYPCB1	Approximately 1.25 V (output)	Out	ADC Internal Reference Bypass Capacitor — REFBYPCA1 and REFBYPCB1 require external bypass capacitors pins for the eQADC 25% reference.[2]

1. This pin is an output if the 3.3 V regulator is enabled; otherwise it is an input. The 3.3 V regulator is disabled if VDDREG is less than 4.5 V.
2. REFBYPCA1 and REFBYPCB1 are not available on revision 1 of the MPC5674F. They were called VSSA_A0 and VSSA_B1 on revision 1.

3.1.1 I/O power and ground segmentation

Some of the supplies can be configured with different supply voltages. In particular, the MCUs allow flexibility in the selection of voltage levels on many of the supplies that power input and output pins. These supplies are labeled VDDE or VDDEH and are broken into segments. Each segment can be connected to different supply voltages if required. The VDDE

supplies are generally 3.3 V (nominal voltage) or lower. The VDDEH supplies are "high" supplies and can be connected to either a nominal 3.3 V or 5.0 V. See the data sheet for each specific device to learn what voltages can be connected to the power pins, but the generally used voltage is shown in the previous table.

The table below shows the different power supply segments that are available on the MPC567xF and MPC5676R devices. The modules associated with the pins shown are per the definitions in the "Signal Properties and Muxing Summary" table in the MPC567xF or MPC5676R reference manual.

NOTE

The internal 3.3 V regulator cannot supply enough current to power any of the IO segments of the device. An external supply is required if the FlexRay, Nexus, or external development bus will be used (VDDE2, VDDE8, VDDE9, and VDDE10).

Table 5. MPC567xF and MPC5676R I/O power/ground segmentation

Power segment	Voltage range	I/O pins powered by segment
VDDEH1	3.3 V to 5 V	**eTPU A:** TCRCLKA, eTPUA[0:31] **eSCI A and B:** TXDA, RXDA, TXDB, RXDB **Reset and Clocks:**$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, BOOTCFG[0:1], WKPCFG, PLLCFG[0:2] **JTAG and Nexus:** TEST
VDDE2	3.3 V	**FlexRay:** FR_A_TX, FR_A_RX, FR_A_TX_EN, FR_B__TX, FR_B_RX, FR_B_TX_EN **Reset and Clocks:** ENGCLK **JTAG and Nexus:**$\overline{\text{EVTI}}$, $\overline{\text{EVTO}}$, MCKO, MDO[0:15], $\overline{\text{MSEO}}$[0:1], TCK, TDI, TDO, TMS, $\overline{\text{RDY}}$, JCOMP
VDDEH3	3.3 V to 5 V	**DSPI A:** SCKA, SINA, SOUTA, PCSA0, PCSA1, PCSA2, PCSA3, PCSA4, PCSA5 **DSPI B:** SCKB, SINB, SOUTB, PCSB0, PCSB1, PCSB2, PCSB3, PCSB4, PCSB5
VDDEH4	3.3 V to 5 V	**EMIOS:** EMIOS[0:31] **eSCI C:** TXDC **DSPI:** SCKC, SINC, SOUTC, PCSC0, PCSC1
VDDEH5	3.3 V to 5 V	**eSCI C:** RXDC **DSPI C:** PCSC2, PCSC3, PCSC4, PCSC5
VDDEH6	3.3 V to 5 V	**eTPU B:** TCRCLKB, ETPUB[0:31]
VDDEH7	3.3 V to 5 V	**eTPU C:**[1] TCRCLKC, ETPUC[0:31] **FlexCAN:** CNTXA, CNRXA, CNTXB, CNRXB, CNTXC, CNRXC, CNTXD, CNRXD
VDDE8	3.3 V	**EBI:** D_CS2, DCS3, D_ADD[9:20], D_WE[0:3], D_BDIP
VDDE9	3.3 V	**EBI:** D_CS0, D_ADD[21:30], D_TS, D_TA, D_CS1, D_CLKOUT
VDDE10	3.3 V	**EBI:** A_ADD_DAT[0:15], D_RD_WR, D_OE, D_ALE
VDD33	3.3 V	**Reset and Clocks:** XTAL, EXTAL

1. The MPC567xF does not support the eTPUC. The GPIO[440:472] function is available on all of these balls. Alternate functions available on ETPUC[16:31] include FR_A_TX, FR_A_RX, FR_A_TX_EN, eSCI TXDA, eSCI RXDA, eSCI TXDB, eSCI RXDB, DSPI PCSD5, DSPI PCSD4, DSPI PCSD3, DSPI PCSD2, DSPI PCSD1, DSPI PCSD0, DSPI SCKD, DSPI SOUTD, DSPI SIND.

Alternate functions are powered by the supply that powers the primary function of each ball.

3.1.2 Power supply package differences

There are different numbers of balls available for the power supply in each of the different package options. In addition, for some package options, some power supplies are not available. The table below shows, for each package, the number of balls available for the power supply input to the device. All supply balls that are available on the package should be connected to a supply voltage.

Table 6. Number of power supply balls versus package

Power supply	Nominal voltage	324 PBGA package	416 PBGA package	516 PBGA package
VDD	1.2 V	14	14	15
VSTBY	1 V, or 2 V to 6 V	1	1	1
VDDSYN	3.3 V	1	1	1
VDD33	3.3 V	2	3	7
VDDREG	3.3 V or 5.0 V	1	1	1
VDDEH1	3.3 V to 5 V	2	2	2
VDDE2	3.3 V	10	16	16
VDDEH3	3.3 V to 5 V	0[1]	2	2
VDDEH4	3.3 V to 5 V	2	2	2
VDDEH5	3.3 V to 5 V	0	2	2
VDDEH6	3.3 V to 5 V	2	2	2
VDDEH7	3.3 V to 5 V	3	3	3
VDDE8	3.3 V	0	0	6
VDDE9	3.3 V	0	0	7
VDDE10	3.3 V	0	0	7
VDDA_A[0:1]	5 V	2	2	2
VDDA_B[0:1]	5 V	2	2	2

1. This supply is shorted internal to the package to VDDEH4. Therefore VDDEH3 is powered, although it does not have a package ball.

3.2 PMC overview

The power management controller (PMC) handles all of the on-chip voltage regulators, regulator controllers, power-on reset, and the low-voltage detect (LVD) circuitry. The figure below shows a block diagram of the PMC.

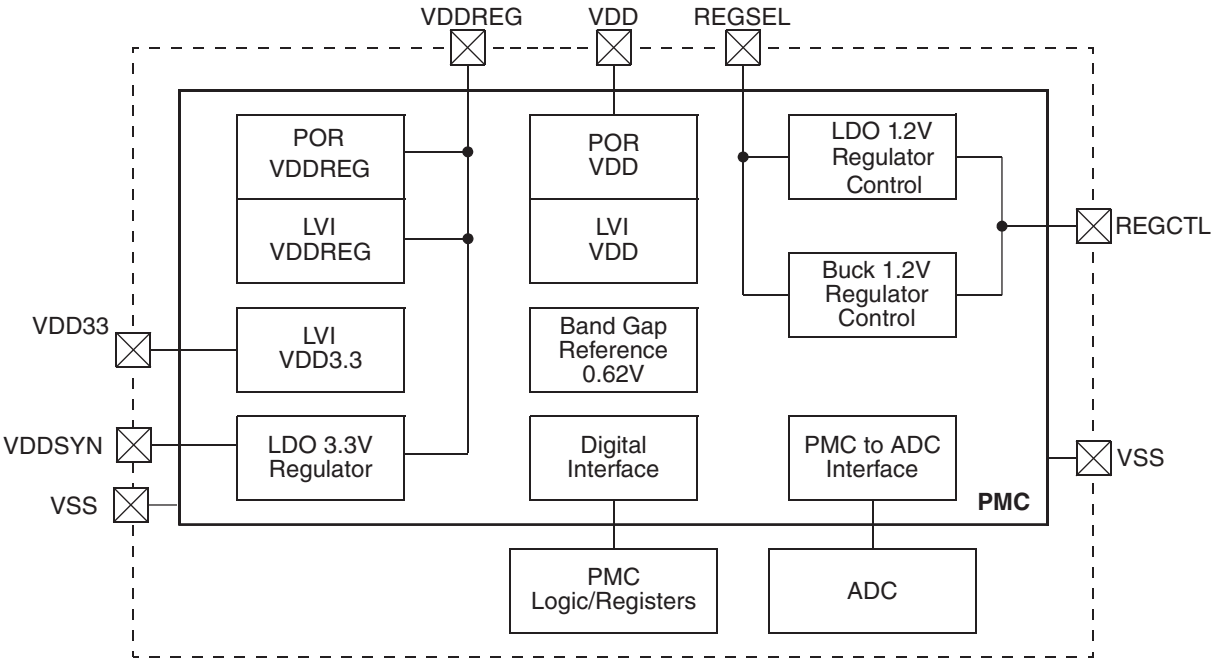


Figure 2. MPC567xF and MPC5676R PMC analog block diagram

The various sub-blocks of the PMC will be discussed in the other sections of this application note, but the features of the PMC include:

- Supporting the use of internal or external voltage regulators
- Two options for a 1.2 V regulator controller: either a linear regulator that uses an external NPN transistor or a switch-mode regulator with an external NMOS FET, Schottky diode, and external inductor. The operating mode of the 1.2 V regulator controller is selectable with the REGSEL pin.

3.3 Power-on reset

The PMC controls the internal power-on reset (POR) for the MCUs. When the critical power supplies are below minimum levels, the MCUs are held in a reset state. The PMC POR holds the device in reset until the power supplies have reached a level high enough that the $\overline{\text{RESET}}$ input can be propagated through the device. The key supplies that are monitored by the PMC are:

- The 1.2 V core voltage,
- VDDREG regulator input voltage,
- VDDEH1 power supply that powers the $\overline{\text{RESET}}$ pin.

During POR the device I/O pins are held in a safe state that depends on which power supplies are on and which are turned off.

The latest version of the MPC567xF or MPC5676R Data Sheet should be consulted for the latest specifications.

Table 7. Supplies that control $\overline{\text{POR}}$ Assertion

Supply	Symbol	Parameter	Minimum	Typical	Maximum	Units
VDD	V_{PORC}	POR rising VDD (1.2v)	—	0.7	—	Volts
	—	POR VDD variation	V_{PORC} - 30%	V_{PORC}	V_{PORC} + 30%	Volts
	—	POR VDD hysteresis	—	0.075	—	Volts

Table continues on the next page...

Table 7. Supplies that control $\overline{\text{POR}}$ Assertion (continued)

Supply	Symbol	Parameter	Minimum	Typical	Maximum	Units
VDDREG	V_{PORREG}	POR rising VDDREG	—	2	—	Volts
	—	POR VDD variation	V_{PORREG} - 30%	V_{PORREG}	V_{PORREG} + 30%	Volts
	—	POR VDD hysteresis	—	0.250	—	Volts
VDDEH1	—	$\overline{\text{RESET}}$ low-voltage detect (Enabled during reset)	2.0[1]	—	3.0	Volts

1. Full device operation is not guaranteed at this voltage, only that the $\overline{\text{RESET}}$ signal will be able to propagate through the device.

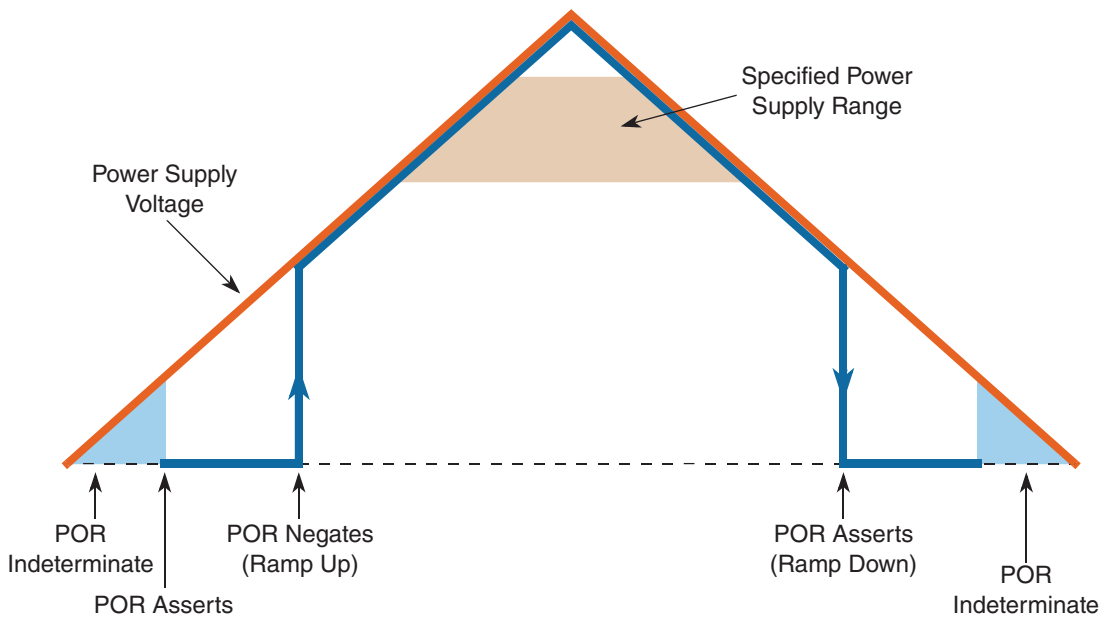


Figure 3. POR assertion/negation diagram

During the initial POR, the voltage on VDDEH1 (the power supply that powers the RESET input), as well as several other supplies, control the exit of the power-on reset. After the MCU exits reset, user software can enable even more supplies to cause a reset assertion if the supplies dip below the specified voltages. See the Power Management Controller Module Configuration register (PMC_MCR) in the MPC567xF or MPC5676R Reference Manual for a complete list of the bits in this register. The bits shown in the next table affect the internal RESET assertion initially after a POR (and consequently $\overline{\text{RSTOUT}}$): the first assertion of reset during POR, and also the Low Voltage Detect (LVD) circuits. They can be enabled or disabled by the user.

Table 8. Low-voltage reset control bits in the PMC_MCR

PMC_MCR Bit	Description	Default setting (following any reset)
LVRER	Reset supply (VDDEH1) low-voltage reset enable	1 (enabled)
LVREH	VDDEH low-voltage reset enable	0 (disabled)
LVRE50	VDDREG (3.3 V or 5 V) low-voltage reset enable	0 (disabled)
LVRE33	VDDSYN (3 V) low-voltage reset enable	1 (enabled)
LVREC	Core-voltage-supply VDD (1.2 V) low-voltage reset enable	1 (enabled)
LVREA	VDDA (analog supply) low-voltage reset enable	0 (disabled)

The following figure shows the relationship of the POR levels and the low-voltage detect circuits. The low-voltage detect circuits can be set to force a reset or an interrupt. An interrupt allows software to perform an orderly, controlled shut down of the MCU.

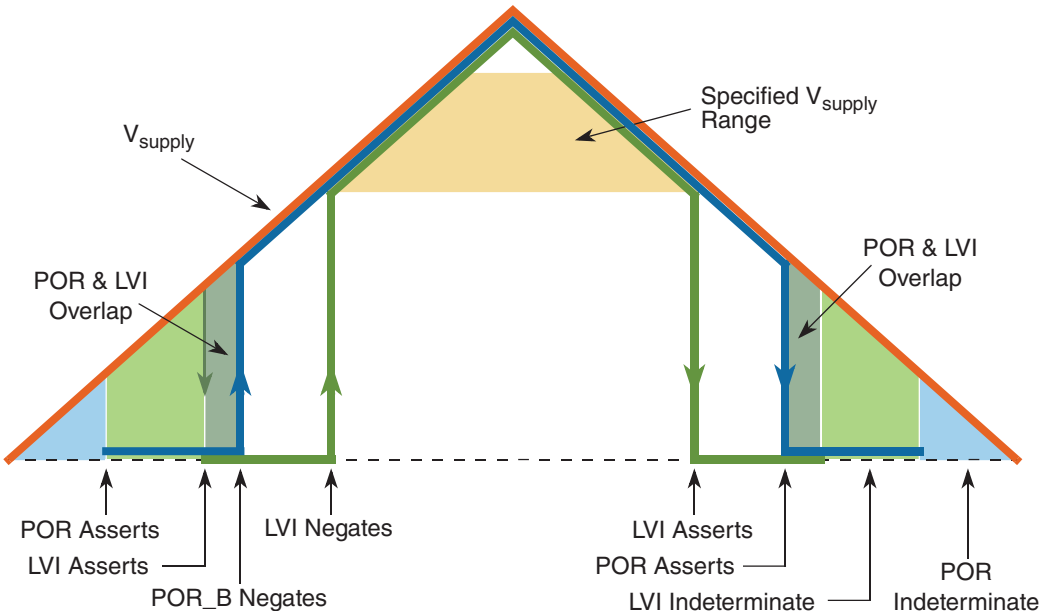


Figure 4. Low-voltage detect ramp up and down

3.4 Power up/down sequencing

As long as the following two rules are met, there is no power sequencing required among power sources during power up and power down in order to operate within specification:

- When V_{DDREG} is tied to a nominal 3.3 V supply, V_{DD33} and V_{DDSYN} must both be shorted to V_{DDREG}.
- When V_{DDREG} is tied to a 5 V supply, V_{DD33} and V_{DDSYN} must be tied together and be powered by the internal 3.3 V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each V_{DDE}/V_{DDEH} first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all V_{DDE}/V_{DDEH} supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements, to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to the following tables.

Table 9. Power sequence pin states for MH and AE pads

V_{DD}	V_{DD33}	V_{DDE}	MH pad	MH+LVDS pads[1]	AE/Up-Down pads[2]
High	High	High	Normal operation	Normal operation	Normal operation
—	Low	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs driven high	Pull-ups enabled, pull-downs disabled
Low	High	Low	Output low, pin unpowered	Outputs disabled	Output low, pin unpowered

Table continues on the next page...

Table 9. Power sequence pin states for MH and AE pads (continued)

V_{DD}	V_{DD33}	V_{DDE}	MH pad	MH+LVDS pads[1]	AE/Up-Down pads[2]
Low	High	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pullups enabled, pulldowns disabled

1. MH+LVDS pads are output-only.
2. Due to an erratum, the pull devices on the analog differential pins may be randomly enabled during POR and until the first clock edge propagates through the device. They will then be disabled until enabled by software. The pull-up, pull-down or both of the pull resistors could be enabled.

Table 10. Power sequence pin states for F and FS pads

V_{DD}	V_{D33}	V_{DDE}	F and FS pads
Low	Low	High	Outputs drive high
Low	High	—	Outputs disabled
High	Low	Low	Outputs disabled
High	Low	High	Outputs drive high
High	High	Low	Normal operation - except no drive current and input buffer output is unknown[1]
High	High	High	Normal operation

1. The pad pre-drive circuitry will function normally, but since V_{DDE} is unpowered the outputs will not drive high even though the output pmos transistors can be enabled.

3.4.1 Power sequencing and POR dependent on V_{DDA}

During power-up or power-down, V_{DDA} can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V. This prevents any forward-biasing of device diodes that cause leakage current and/or POR. If the voltage difference between V_{DDA} and V_{DDEH} is more than 1 V, the following will result:

- Triggering of POR (ADC monitors on $V_{DDEH}1$ segment which powers the $\overline{\text{RESET}}$ pin) if the leakage current path created, when VDDA is sufficiently low, causes sufficient voltage drop on $V_{DDEH}1$ node monitored crosses low-voltage detect level.
- If V_{DDA} is between 0–2 V, powering all the other segments (especially $V_{DDEH}1$) will not be sufficient to get the part out of reset.
- Each V_{DDEH} will have a leakage current to V_{DDA} of a magnitude of (($V_{DDEH} - V_{DDA} - 1$ V(diode drop)/200 KΩ) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V).
- Each V_{DD} has the same behavior; however, the leakage will be small even though there is no current limiting resistor since V_{DD} = 1.32 V max.

3.4.2 Power-down

If V_{DD} is powered down first, then all drivers are tri-stated. There is no limit to how long after V_{DD} powers down before V_{DDE}/V_{DDEH} must power down.

If V_{DDE}/V_{DDEH} is powered down first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DDE}/V_{DDEH} powers down before V_{DD} must power down.

There are no limits on the fall times for the power supplies.

3.4.3 Power-up

If V_{DDE}/V_{DDEH} is powered up first, then a threshold detector tri-states all drivers connected to V_{DDE}/V_{DDEH}. There is no limit to how long after V_{DDE}/V_{DDEH} powers up before V_{DD} must power up. If there are multiple V_{DDE}/V_{DDEH} supplies, they can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

If V_{DD} is powered up first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode voltage drop above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DD} powers up before V_{DDE}/V_{DDEH} must power up.

The rise times on the power supplies must be no faster than 25 V/millisecond.

3.5 Using the internal regulator and regulator controller

The MPC567xF and MPC5676R contain an internal regulator that can be used to generate 3.3 V. This regulator can be used along with the regulator controller for the low-voltage supply (1.2 V). External capacitors are required for both the 3.3 V and the 1.2 V supplies. Additional external circuitry is required for the 1.2 V regulator controller. The 1.2 V regulator can operate in either linear or switch mode.

Optionally, an external 3.3V supply can be used (while still using the internal 3.3V regulator for V_{DD33} and V_{DDSYN}) to power the 3.3V high speed I/O pins (the development bus, FlexyRay, and/or the Nexus trace signals).

3.5.1 Internal linear 3.3 V regulator

A 3.3 V regulator is fully contained within the device. This regulator is enabled automatically if V_{DDREG} is greater than 4.5 V. If V_{DDREG} is less than 4.5 V, then the 3.3 V regulator is drive strength may be reduced (and not capable pf sustaining the full load current during a flash erase procedure). In order to bypass the internal 3.3 V regulator, V_{DDREG}, V_{DDSYN}, and VDD33 must be shorted together and connected to an external 3.3 V supply.

NOTE

The 3.3 V supply sense signal is connected to V_{DD33}. Therefore, when using the internal 3.3 V regulator, V_{DDSYN} and V_{DD33} must be connected together with as little inductance as possible on the target circuit board.

The internal 3.3 V regulator can only provide a minimal amount of current (60 - 80 mA, see the data sheet for the exact specification). Therefore, it is not large enough to provide power to either the external development bus or the Nexus trace signals. When using the external bus, FlexRay, or Nexus trace, an external 3.3 V supply is required. However, the internal 3.3 V regulator can provide enough current to power just the JTAG pins, if needed.

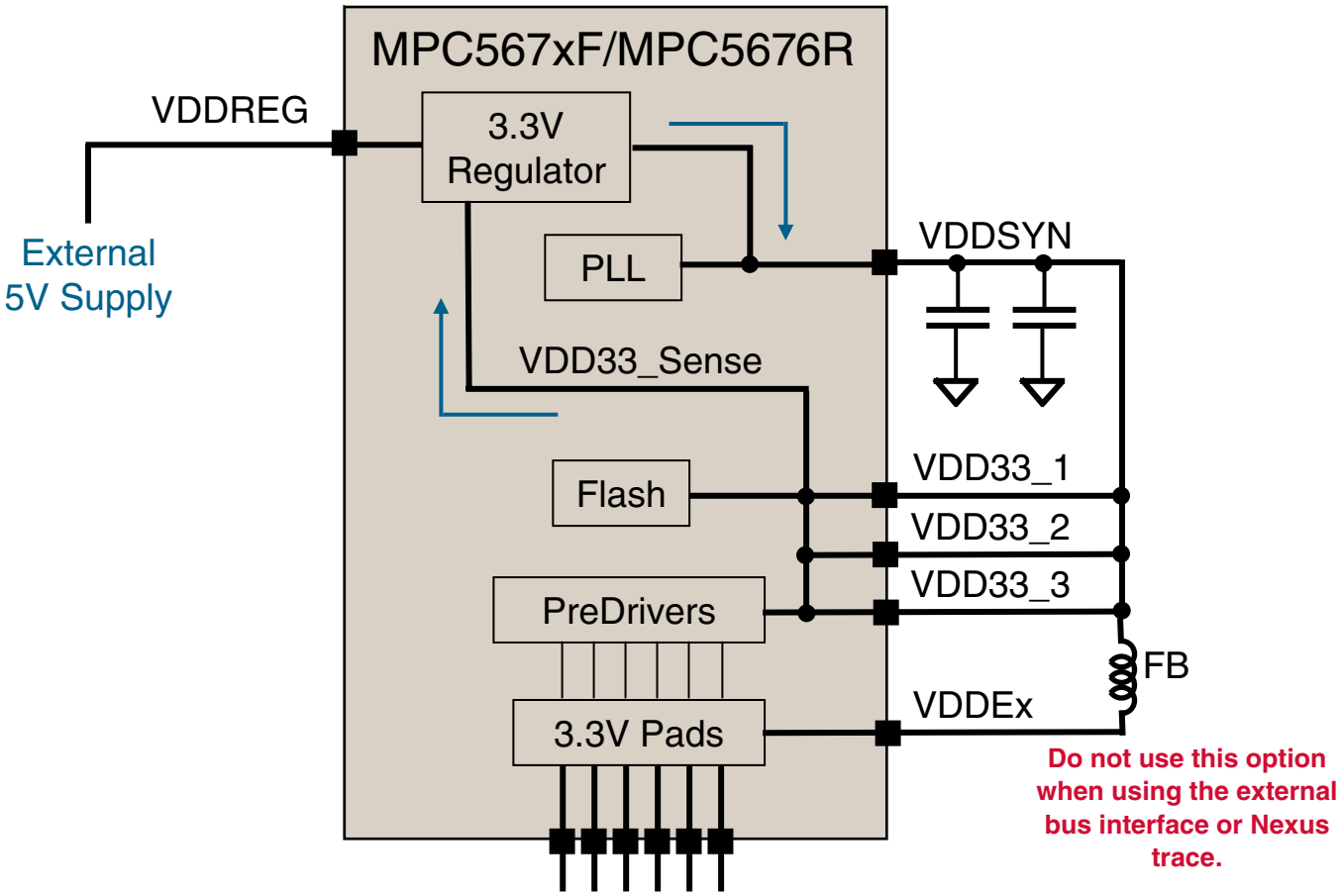


Figure 5. 3.3 V power connection options (JTAG only)

When using an external 3.3V supply (for powering the Nexus trace pins, FlexRay pins, or the external bus pins), the following configuration should be used. It is highly recommended that this configuration be used to power the internal flash from the internal regulator and use the external 3.3V power supply to power the pin driver supplies (V_{DDEHx}).

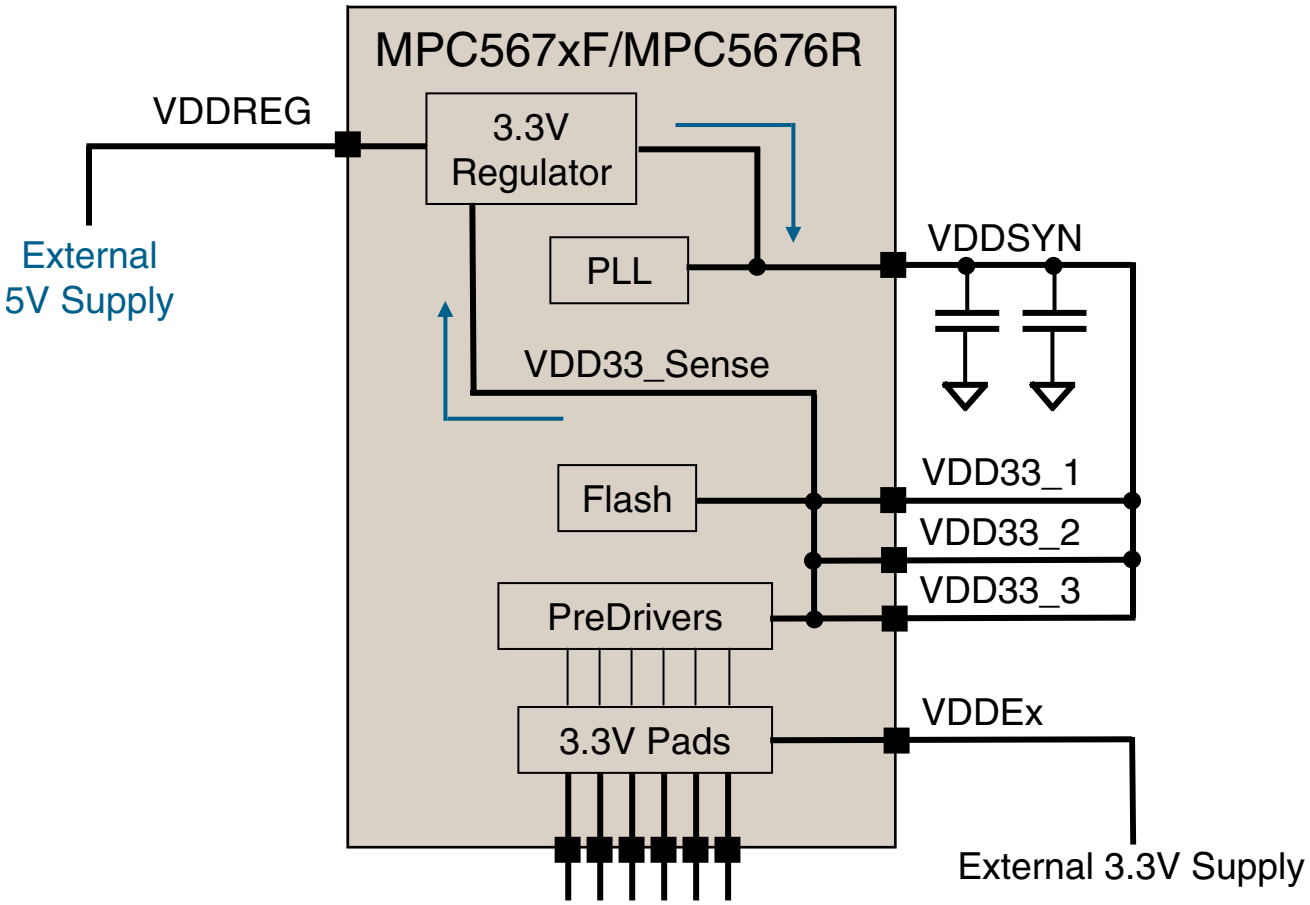


Figure 6. Recommended 3.3V power connections

3.5.2 1.2 V low-voltage regulator controller

The majority of the internal circuitry in the MPC567xF and MPC5676R operates on a 1.2 V nominal supply voltage. The devices include an on-chip regulator controller for providing this voltage. However, there are two options for the 1.2 V regulator controller: a linear regulator controller or a switch mode regulator controller. The linear regulator controller requires an external NPN transistor and the switch mode regulator controller requires an external NMOS[2] FET[3] with an external rectifier and inductor. The linear regulator circuit provides a low-noise, stable 1.2 V supply, but requires a significant amount of current and power dissipation. The switch mode regulator also provides a stable 1.2 V supply, but has a lower overall power dissipation. Care is needed to insure that the switching frequency is isolated from any noise-sensitive circuitry in the target system.

3.5.2.1 Linear 1.2 V regulator controller

The linear 1.2 V regulator controller requires an external transistor and bypass capacitors. It operates in a closed loop mode. The figure below shows the typical configuration of the regulator circuit.

2. N-Channel Metal Oxide Semiconductor
3. Field-Effect Transistor

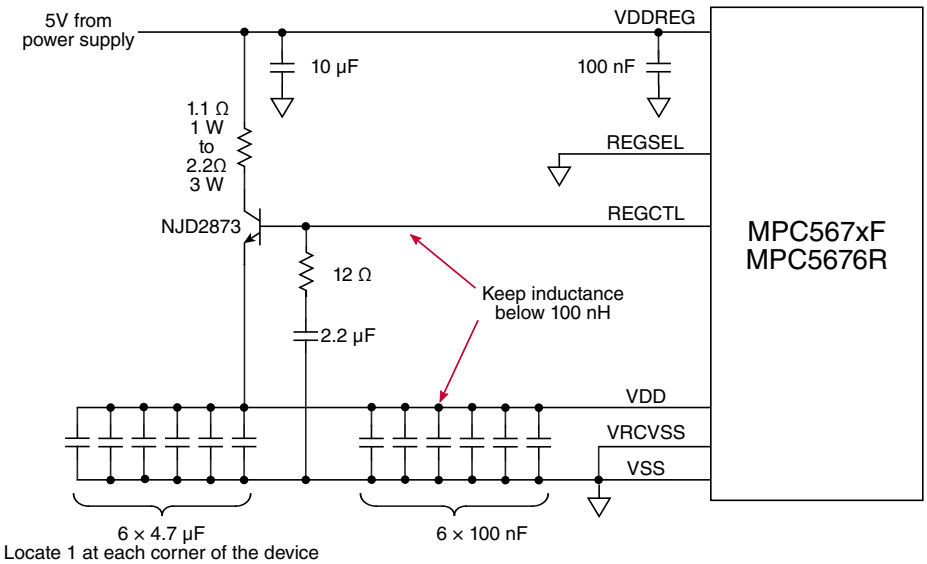


Figure 7. 1.2 V linear regulator circuitry

The PMC monitors the voltage on VDD via the VDD_{SENSE} signal. The VDD_{SENSE} signal is internal to the package of the device and does not have a physical ball on the package. The PMC controls the current on REGCTL, which drives the base of the external NPN transistor. This current is then amplified by the transistor to power VDD of the MCUs.

3.5.2.1.1 Bipolar transistor requirements

The table below shows the characteristics required for the external bipolar NPN pass transistor.

Table 11. Bipolar NPN Transistor Requirements

Symbol	Characteristic	Minimum	Maximum	Unit
hfe	Transistor gain (Beta)	60[1]	550	—
P_D	Absolute minimum power dissipation	1[2]	—	W
I_{CMaxDC}	Minimum peak collector current	1.0	—	A
VCE_{SAT}	Collector to emitter saturation voltage	200[3]	600	mV
V_{BE}	Base to emitter voltage	0.4	1.0	V

1. The minimum gain required depends on the current required by the MCU (on VDD) and the available current from the REGCTL (See the MPC567xF and MPC5676R Data Sheets).
2. 1.5W preferred.
3. Adjust collector to voltage supply source resistor value to avoid VCE < VCE_{SAT}

3.5.2.1.2 1.2 V linear regulator recommended components

The recommended bipolar NPN pass transistor is the NJD2873 or a generic BCP68 transistor. Care needs to be taken when selecting a BCP68 transistor to ensure that it meets the requirements over temperature. A series resistor is required to assist in power handling of the drop from 5 V to 1.2 V. Proper heat-sinking is also needed. The NJD2873 has been specified to meet the requirements for the MPC5500 and MPC5600 devices and is therefore the preferred transistor. In addition, the NJD2873 is in a DPAK package that allows a higher power dissipation (the typical package for the BCP68 is the SOT-223-4).

Table 12. Recommended Transistors

Part	Type	Manufacturer
NJD2873T4[1]	NPN transistor	ON Semiconductor™
BCP68T1	NPN transistor	ON Semiconductor™
BCP68	NPN transistor	NXP Semiconductors™

1. Preferred pass transistor

The linear pass transistor should be placed near the MCU with a minimum of trace resistance and inductance. VDD should be placed on a layer near the ground layer and should be laid out to make maximum utilization of the board inter-capacitance. VDD should not be routed, it should be a maximum size plane (placed under the MCU) with low inductance.

The rest of the components for regulator circuit, including the bypass capacitors, are shown in the following table.

Table 13. Passive Components

Component	Value	Quantity	Description
Capacitor	4.7 µF, 20 V	6	Ceramic low ESR
Capacitor	100 nF, 20 V	6	Ceramic
Capacitor	10 µF	1	Supply decoupling capacitor
Capacitor	2.2 µF	1	Phase compensation (snubber) capacitor
Resistor	12 Ω	1	Phase compensation (snubber) resistor
Resistor	2.2 Ω, 3W	1	Power sharing resistor for transistor collector.
	1.1 Ω, 1W	1[1]	

1. Only one resistor should be installed on the transistor collector, between 1.1 Ω to 2.2 Ω.

3.5.2.2 Switch mode 1.2 V power supply (SMPS)

The MPC567xF is the first automotive Powertrain 32-bit microcontroller to include an optional 1.2 V switching regulator controller that can be used instead of the linear 1.2 V on-chip regulator controller. The MPC5676R also includes the SMPS regulator controller. The switching regulator is much more efficient than the linear regulator. This allows the overall current requirements (power dissipation) to be lower when using the switching regulator.

The switch mode regulator is selected by connecting the regulator select input (REGSEL) to the regulator voltage input (VDDREG), instead of connecting REGSEL to 0 V. The switching regulator uses an external NMOS transistor, along with an external inductor, a Schottky rectifier, and a bulk capacitor.

The switch mode regulator controller circuitry contains a pulse-width modulated (PWM) controller that uses the duty cycle of the switching frequency to control the voltage that is applied to the VDD power supply input of the MCU. The switching frequency of the PWM circuit is between 1 MHz and 2 MHz. A voltage sense on VDD controls the actual duty cycle to control the voltage output of the regulator circuitry.

The layout of any switch mode regulator circuit is always critical and should be done with great care (see Switch mode supply layout guidelines).

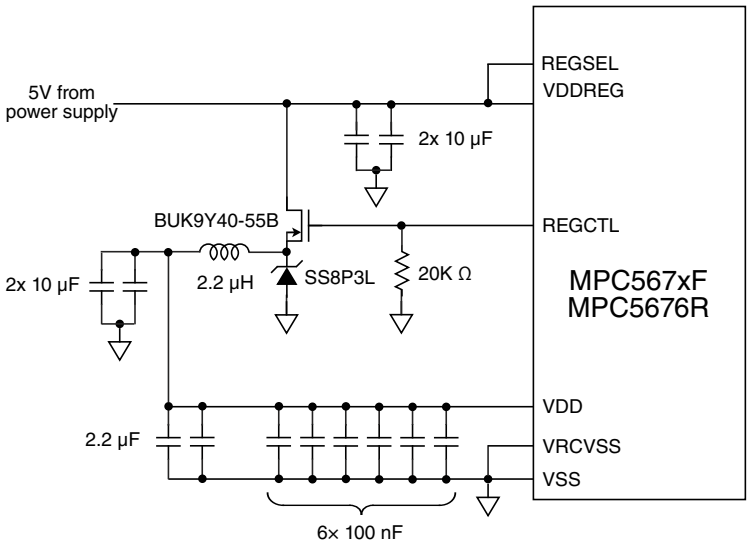


Figure 8. 1.2V SMPS regulator circuitry

3.5.2.2.1 SMPS NMOS transistor requirements

The table below shows the characteristics of the NMOS FET used for the SMPS.

Table 14. NMOS Transistor Requirements

Symbol	Characteristic	Minimum	Maximum	Unit
V_F	Maximum forward voltage drop	0.4	0.6	V
V_{TH}	Threshold voltage	—	2.0	V
I_{DS}	Drain to source current	1.5	—	A
V_{DS}	Drain to source voltage	12	—	V
$R_{DS(on)}$	Static drain-to-source on-resistance	—	100	Ω
C_G	Gate capacitance	—	5	nF
—	Turn on/off delay	—	50	ns
—	Rise time	—	90	ns

3.5.2.2.2 1.2 V SMPS recommended components

The SMPS regulator requires an external NMOS FET. This can either be an NMOS FET with an integrated low Vf Schottky diode or a separate NMOS FET and a separate low Vf Schottky diode.

Table 15. Recommended NMOS FET transistors

Part		Type	Manufacturer
Integrated	IRF7521	Power MOSFET and Schottky diode	International Rectifier™
Integrated	IR7353	High-speed NMOS FET + Schottky diode	International Rectifier™

Table continues on the next page...

Table 15. Recommended NMOS FET transistors (continued)

Part		Type	Manufacturer
Integrated	SI5856D	N-channel MOSFET with Schottky diode	Vishay General Semiconductor™
Separate FET/ Diode	SS8P3L	High current density surface mount Schottky barrier rectifiers	Vishay General Semiconductor™
	BUK9Y40-55B[1]	NMOS FET	NXP Semiconductor
	BUK9832-55A	NMOS FET	NXP Semiconductor
	SI3460f	NMOS FET	International Rectifier™

1. This is the preferred automotive solution.

The rest of the components for the SMPS regulator circuit, including the bypass capacitors, are shown in the following table. It should be noted that the component selection for the SMPS is more critical than for the linear regulator option, but has the benefit of overall lower current requirements.

Table 16. Passive components

Component	Part number	Value	Quantity	Description
Inductor	LQH66SN2R2M03[1]	2.2 µH, 3.2 A	1	muRata™ unshielded or shielded coil
	EM0540M-2R2Y[2]	2.2 µH		Panasonic
	MPA7030-2R2-R[3]	2.2 µH		Cooper Bussmann Coiltronics
Capacitor	C3225X7R1E106M	10 µF, 25 V	2	TDK high capacitance ceramic SMD - connect to VDD near the inductor
Capacitor	C3225X7R1E106M	10 µF, 25 V[4]	2	TDK high capacitance ceramic SMD - connect near the drain of the NMOS FET (the source voltage for VDD)
Capacitor	C3225X7R1E225K	2.2 µF, 25 V	2	TDK capacitance ceramic SMD - connect to VDD near the MCU
Capacitor	—	100 nF, 2 V	6	Ceramic
Resistor	—	20 KΩ	1	Pull down on the gate of the NMOS FET

1. This component is not Automotive qualified and does not meet the same temperature as the MPC567xF/MPC5676R.
2. In development.
3. Automotive qualified.
4. A single 22 µF capacitor can optionally be used instead of two 10 µF capacitors.

3.5.2.2.3 Switch mode supply layout guidelines

The layout of the switch mode regulator circuit is critical to the proper operation and performance of the regulator.

- The input power supply capacitor (two times 10µF at the source of the NMOS, connected to VDDREG), the output capacitor (two times 10µF at the inductor output), and inductor shown should be located very close to the power MOS-Schottky diode.
- The output capacitor (two times 10µF, connected to the inductor) should be connected close to the inductor to the MCU ground.
- The common power ground for nodes with high switching currents should be separated from nodes with low switching currents.
- Minimize the inductance between the switching supply node and the decoupling/filtering capacitor, so that decoupling is effective and minimum energy is radiated.
- Star-connect all grounds to the ground plane below the MOS-Schottky device.
- Keep the gate control signal REGCTL far away from any other switching signals on the board, shield with VSS,

- Place the smaller EMI/bypass capacitors underneath the microcontroller.
- Use the 5 V power trace exclusively as power to the source of the power MOS by means of star connection to the global 5 V power supply.

3.6 Using internal and external supplies

An external 3.3 V supply can be used while still using the internal 1.2 V linear regulator. The SMPS regulator controller cannot be used when an external 3.3 V supply is being used with the device and V_{DDREG} is connected to an external 3.3 V supply. In this configuration, V_{DDREG}, V_{DDSYN}, and V_{DD33} must be shorted together and powered by the same 3.3 V supply. The figure below shows this configuration. However, it does not show all of the external 1.2 V circuitry. See the section on the 1.2 V linear regulator controller for the complete requirements (see Linear 1.2 V regulator controller).

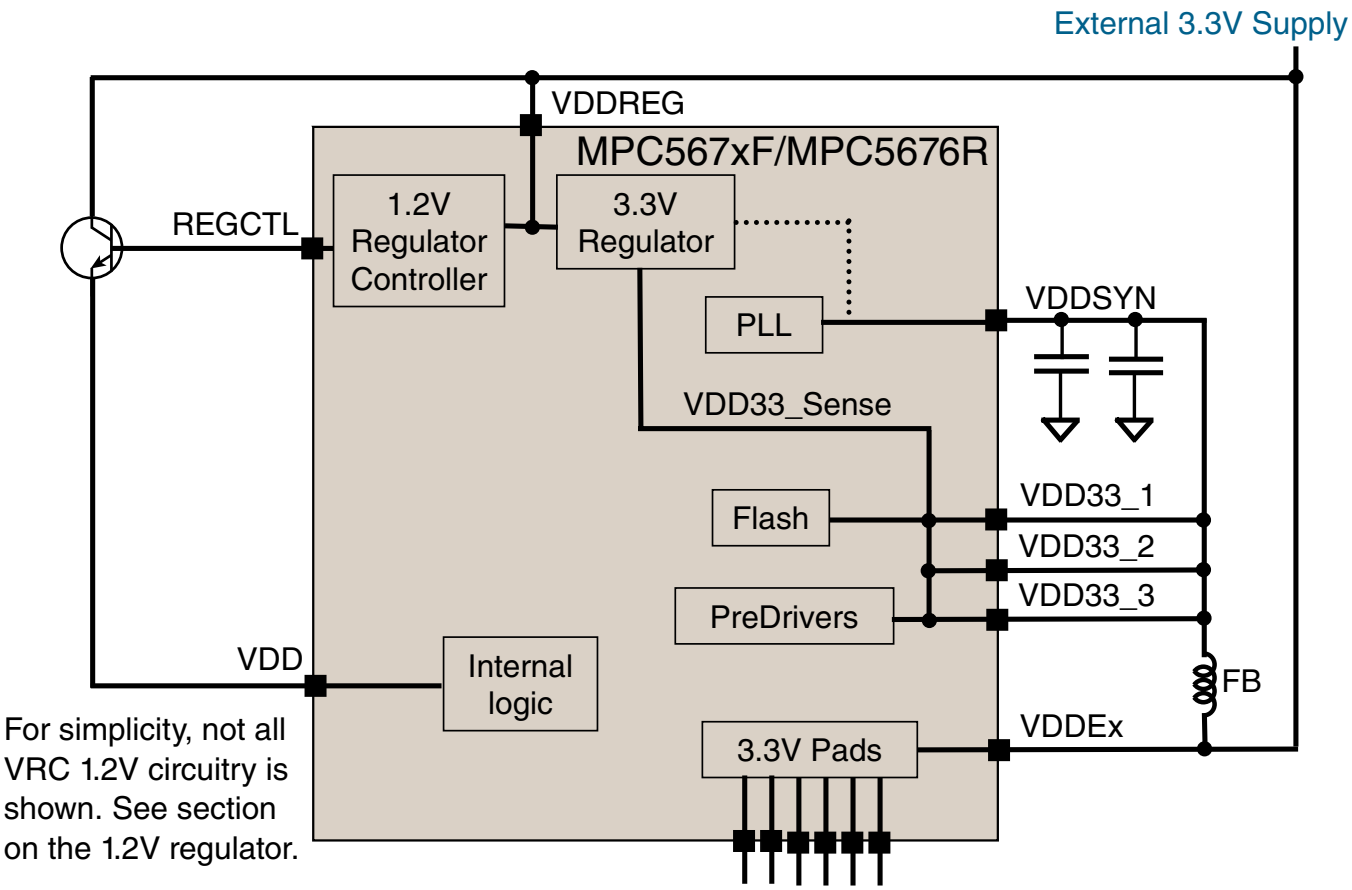


Figure 9. Internal 1.2V regulator with an external (only) 3.3V supply

NOTE

It is highly recommended that even when using an external 3.3 V supply for the VDDEx supplies, that the internal 3.3 V regulator still be used. See Using the internal regulator and regulator controller.

3.7 Using external supplies

The MPC567xF and MPC5676R can be powered by external supplies. The 3.3 V internal regulator is disabled by connecting V_{DDREG} to a voltage less than approximately 4.0 V. V_{DDREG}, V_{DDSYN}, and V_{DD33}**must be** connected together if the internal 3.3 V regulator is not used. Typically, V_{DDREG} is connected to 3.3 V if the internal 3.3 V regulator is not used. This does allow the 1.2 V linear regulator controller to be used if desired. If an external 1.2 V supply will also be used, REGCTL should be left open.

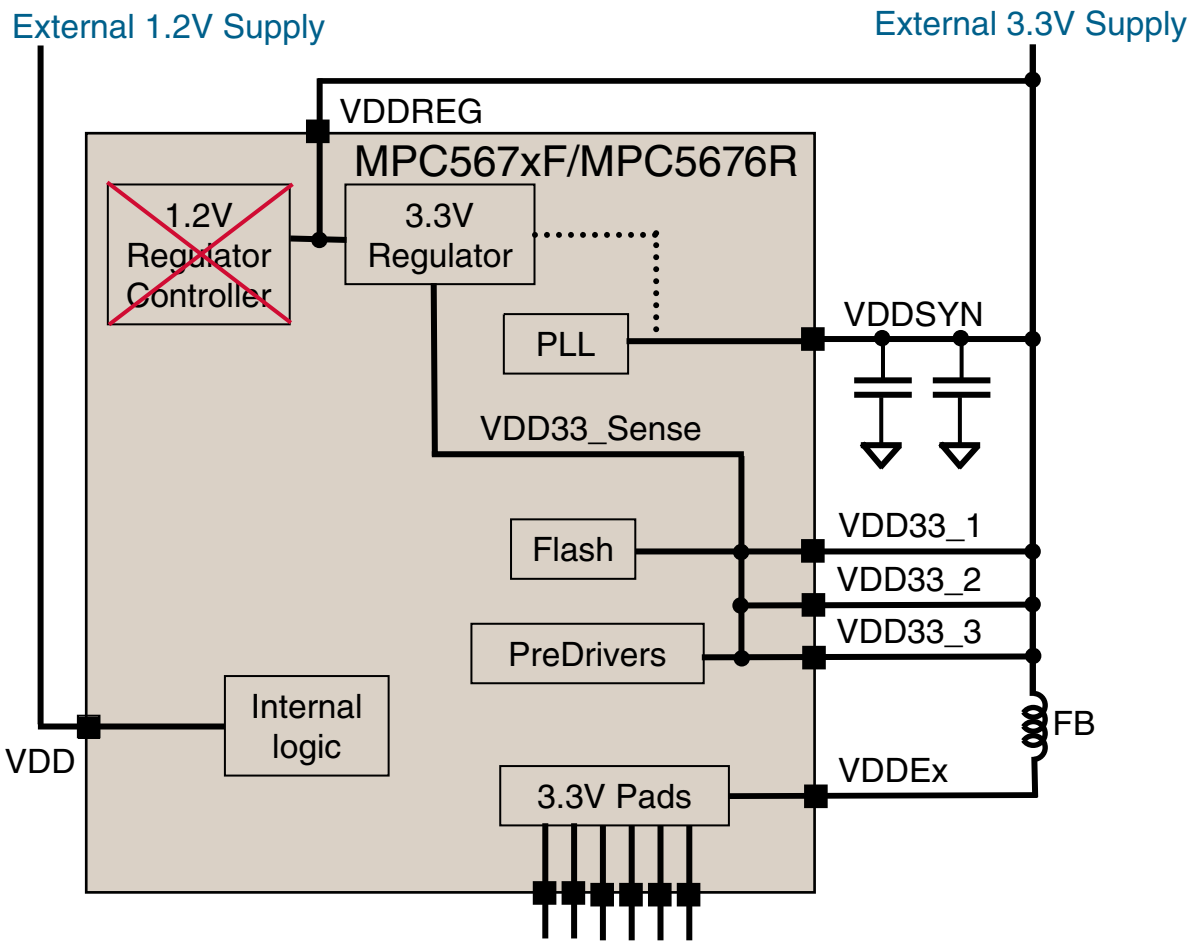
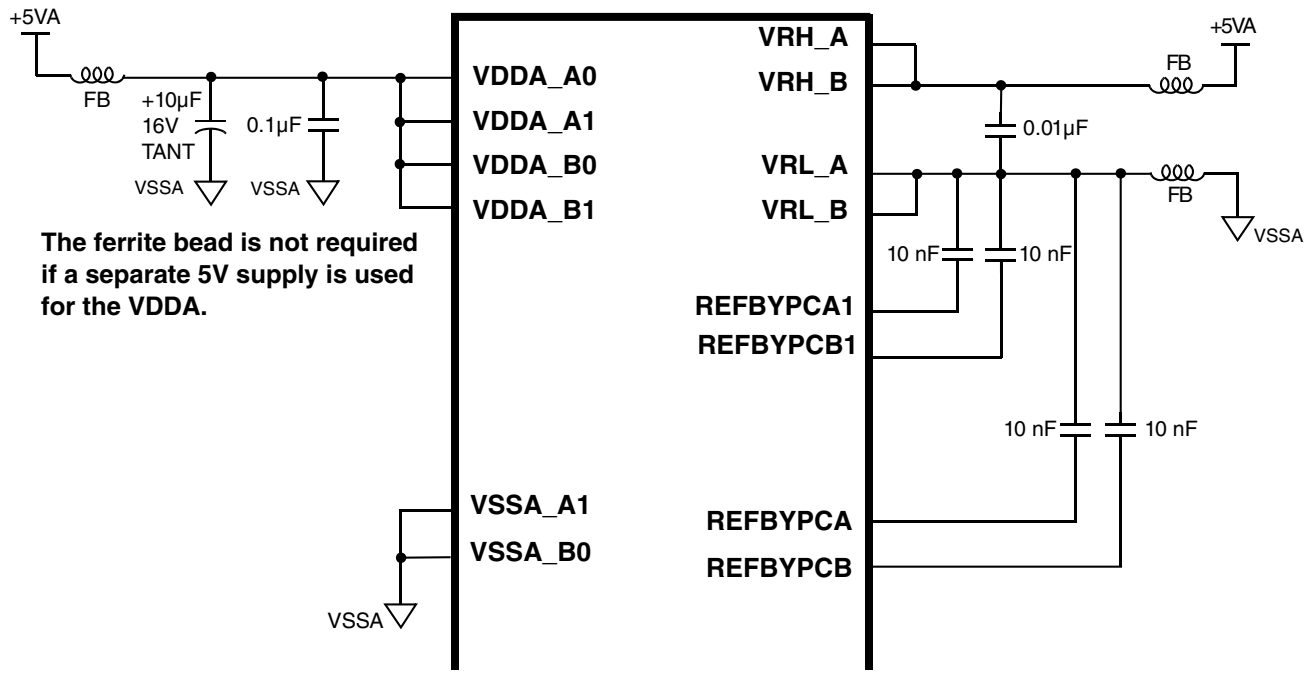


Figure 10. External power supply configuration

When using an external 3.3 V supply, VDDSYN should be connected directly to VDDREG. The VDDEx supplies should be isolated from VDDSYN/VDDREG with a ferrite bead to reduce noise on VDDSYN.

3.8 eQADC (analog) power supply connections

To obtain the best analog performance, it is essential to use correct bypassing and configuration of the eQADC power supply and reference pins. The overall analog performance can directly be linked to noise on either the analog power supplies and/or the reference voltages (VRH and VRL).



This circuit applies to the MPC5676R and revision 2 or later of the MPC567xF. It does not apply to revision 1 of the MPC5674F.

Figure 11. eQADC supply and reference circuitry

The reference bypass capacitor pin (REFBYPC) requires a capacitor to reduce noise on the internal 75% reference used by the ADC. This capacitor may be as high as 100 nF, however, this requires additional settling time on start up of the ADC module but may provide a more stable internal reference in some systems. Some devices (such as the MPC567xF and the MPC5676R) include a second reference bypass (REFBYPCx1) on the internal 25% reference. This should be treated in a similar manner to the 75% bypass capacitor.

VSSA should always be connected directly to the ground plane of the board.

For slightly lower analog performance in low-cost systems, the ferrite bead isolation can be removed from the 5V analog VDDA supply. In addition, the ferrite bead on VRL can and should be removed if the system has a good (solid) ground plane. The ferrite bead on VRH is always recommended.

For the best analog performance, good layout techniques should be used for all signals connected to the analog inputs. It is important that the return path of each analog signal not be interrupted with discontinuities in the return path (either ground or power). Crossing "slots" in the return path will affect the signal integrity.

3.9 SRAM standby supply

The MPC567xF and the MPC5676R include a power supply option for maintaining the contents of a portion of the internal SRAM when power to the rest of the device is off. If the SRAM standby feature is not required in the system, the best option is to connect the SRAM standby pin (VSTBY) to ground. This completely disables the standby SRAM function. It is also possible to connect VSTBY to either an external 3.3 V supply or to the 5 V supply that powers the rest of the device.

Table 17. VSTBY Options

	VSTBY connection	VSTBY voltage
Standby SRAM operation required	Nominal 1.0 V supply that remains powered when all other supplies are off.	0.95 V to 1.2 V

Table continues on the next page...

Table 17. VSTBY Options (continued)

	VSTBY connection	VSTBY voltage
	Nominal 3.3 V or 5 V supply that remains powered when all other supplies are powered off.	2.0 V to 6.0 V
Standby SRAM operation is not required	Ground reference.	0 V
	An external nominal 3.3 V supply that is turned on and off with the device.	3.0 V to 3.6 V
	An external nominal 5 V supply that is turned on and off with the device power.	4.75 V to 5.25 V

There are two options for the VSTBY power supply to provide power to the SRAM when the main device power supplies are turned off. The VSTBY supply can either be between 0.95 V and 1.2 V or it can be between 2.0 V and 6.0 V. When the VSTBY pin is between 0.95 V and 1.2 V, this voltage directly powers the SRAM when VDD is powered off. If VSTBY is between 2.0 V and 6.0 V, an internal standby regulator is enabled and this supply provides power to the SRAM when VDD is off. The table below shows the electrical specifications for VSTBY; however, the latest version of the device data sheet should be consulted.

Table 18. Standby power supply specifications

Characteristic	Minimum	Maximum	Units
No SRAM standby operation	0	0.2	Volts
Illegal VSTBY voltage range	0.2	0.95	Volts
SRAM standby voltage, standby regulator disabled	0.95	1.2	Volts
Illegal VSTBY voltage range	1.2	2.0	Volts
SRAM standby voltage, standby regulator enabled	2.0	6.0	Volts

If the proper voltage is on VSTBY, then VSTBY will provide power to the SRAM anytime the device is in power-on reset (POR). POR is an internal signal that is asserted if any of the monitored supplies are lower than their specified values.

NOTE

VSTBY must not be left floating. If VSTBY is left floating and floats to a voltage greater than 1.2 V, but less than 2.0 V, access to the SRAM will be disabled. If the voltage floats to above 2.0 V, it is likely that insufficient current will be available to power the internal standby regulator which could cause supply to the standby supply to float to a level that will disable access to the SRAM. The assumption in the device is that if the standby voltage to the SRAM is the same or higher than the VDD supply voltage, the VDD supply voltage must be powering down and therefore the SRAM should be disabled to prevent corruption of the SRAM data.

4 Hardware system requirements for oscillator

The most important aspects of an accurate clock source require that some care be taken in the layout and design of the circuitry around the crystal and FMPLL power supplies. Any noise in these circuits can affect the accuracy of the clock source to the FMPLL. The figure below shows the typical connections required for the PLL power supply and the crystal connections. The power supply for the FMPLL is VDDSYN, which is also the output of the internal 3.3 V regulator (if

enabled). If the internal regulator is disabled and an external 3.3 V supply will be used, then noise isolation circuitry is recommended between the system 3.3 V supply and VDDSYN. Any noise on VDDSYN can affect the accuracy and jitter performance of the PLL.

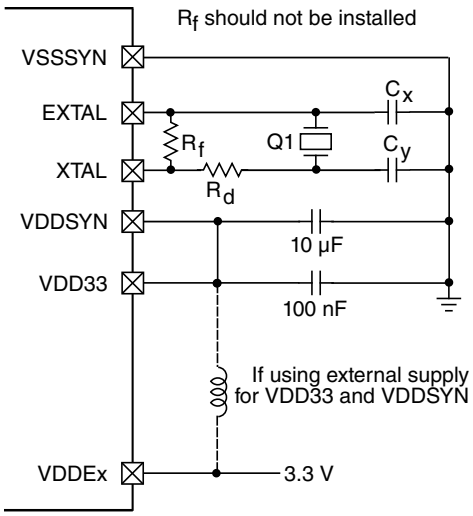


Figure 12. Oscillator and VDDPLL supply connections

In the figure above, R_f should not be installed with any current devices or crystals, as there is an internal feedback resistor. Room should be left in the layout in case a resistor is needed in the future for new types of crystals. Since the layout of the module/board can affect the component values required, customers should have their board characterized by their crystal vendor to recommend values for R_d, C_x, and C_y. The values shown in this document should be used as a starting point. These should be re-characterized for any change to the oscillator circuit layout, including routing changes of other circuitry near the crystal circuit.

NOTE

The oscillator circuit should be placed as close as possible to the MCU. In order to minimize signal degradation, the circuitry should be placed entirely on only one PCB layer, avoiding unnecessary vias where possible. The schematic also illustrates the recommended layout; the VSSSYN trace should be used as a shield around the crystal components and then connected to the ground plane. The bypass capacitor to VDDSYN should also be connected at this ground connection point.

NOTE

Do not allow any signals to cross the crystal connections to the device. **Absolutely no high current or high speed signals should be run near any of the crystal components.**

NOTE

Other than the connections shown in the above schematics, no other connections should be made to the crystal or EXTAL and XTAL device pins. Do not use XTAL to drive any other circuitry than shown.

The recommendations from the crystal manufacturer will include not only a series resistor value but also the load capacitance required for the crystal (the total crystal load capacitance is usually specified in the crystal data sheet). Keep in mind that the load capacitance is the sum of

- Physical capacitors (C_x and C_y)
- Capacitance of the MCU
- Capacitive loading of the board (C_{PCB})
- Pin capacitance (C_{MCU_PIN}) of the MCU EXTAL and XTAL balls (BGA balls are specified as 7 pF maximum)

The requirement for the crystal vendor to measure the customer board is due to the board capacitance effect on the crystal load capacitors.

Generally, the method to calculate the capacitors values to use for C_x and C_y is given by the following:

$C_A = C_B = 2 \times C_L$
$C_A = C_X + C_{MCU\_PIN} + C_{BOARD}$
$C_B = C_Y + C_{MCU\_PIN} + C_{BOARD}$

C_L should come from the crystal specifications (requirements). C_{BOARD} should also include any socket capacitance if a socket is used. This is listed in the device data sheet as the discrete load capacitance to connect to EXTAL and XTAL:

$C_{L\_EXTAL} = (2 \times C_L) - C_{SOCKET\_EXTAL} - C_{PCB\_EXTAL}$
$C_{L\_XTAL} = (2 \times C_L) - C_{SOCKET\_XTAL} - C_{PCB\_XTAL}$

In some cases, the crystal vendor may recommend different values for C_X and C_Y (not equal).

VDDSYN should be isolated from the rest of the system's 3.3 V supply. Ideally, this should be a ferrite bead. However, in very cost-sensitive applications a resistor could be used. The resistor value needs to be low enough that the voltage drop does not allow the voltage to go below the minimum operating voltage of the device. Factored into the this resistor value is the maximum current of the VDDSYN supply (currently, this is specified as less than 10 mA on the devices covered by this application note, but the latest data sheet should be checked for any updates to this specification).

4.1 Oscillator and predivider circuitry

The MPC56xx[4] devices can use either the on-chip oscillator with an external crystal or an external reference clock as the reference clock to the device. This reference is qualified in multiple manners before the PLL will begin lock operation. The "pre" FMPLL circuitry consists of an automatic level-controlled amplifier, a comparator, a loss of clock detector, and a predivider.

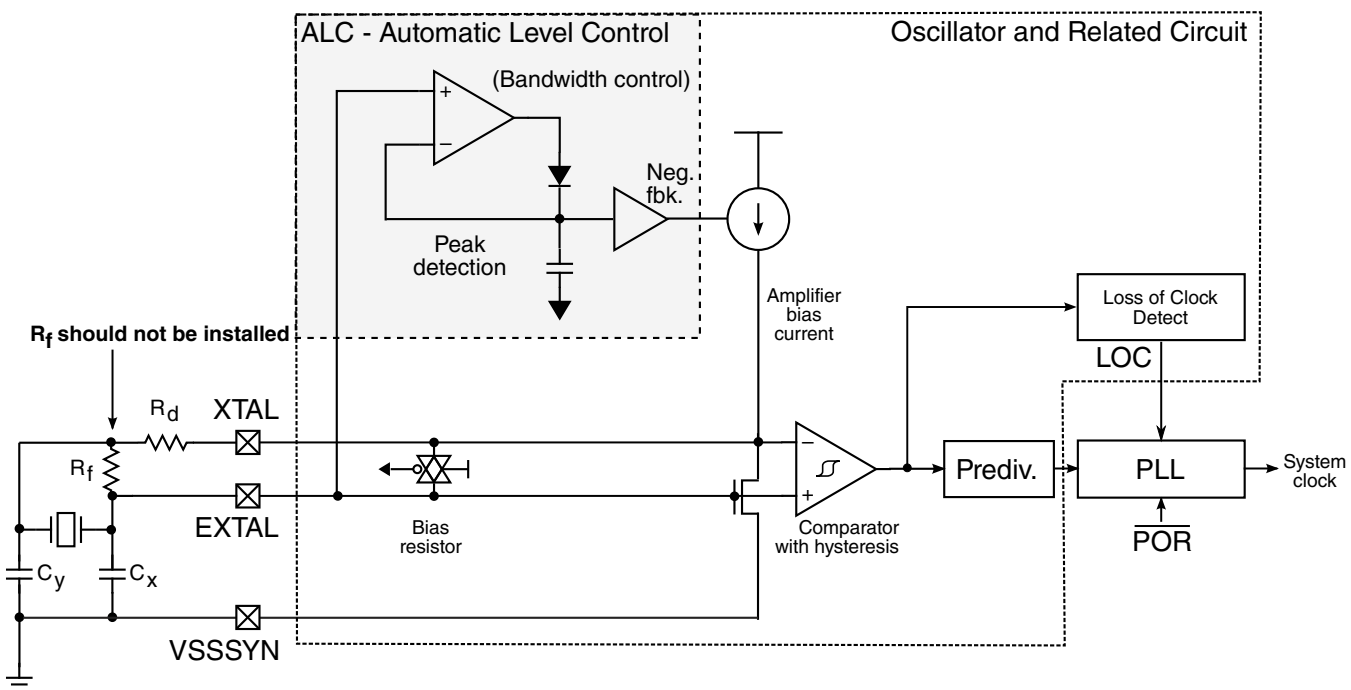


Figure 13. Pre-FMPLL circuitry (oscillator, comparator, and loss-of-clock circuits)

4. including the MPC567xF and MPC5676R

5 Device reset configuration

The basic configuration of the FMPLL, boot location, and timer pull values are set during reset. The states of the control pins for these features are latched four clocks prior to the negation of the RSTOUT input of the device. The following table shows all of the reset configuration pins.

NOTE

The MPC5676R powers up operating with an internal RC oscillator and therefore does not require the PLL[0:1] pins. Software should set the proper values of the multiplier (EMFD) and the dividers (EPREDIV, ERFD) to the desired frequency prior to switching the MCU to the Phase Lock Loop (PLL) output[5].

Table 19. Device reset configuration pins and modes

Configuration	Configuration pins	Description
Boot configuration	BOOTCFG[0:1][1]	The BOOTCFG[0:1] pins control the boot configuration of the device - booting from internal memory, external memory, or serial boot.
FMPLL configuration	PLLCFG[0:2][2]	Sets the operating mode of the FMPLL, including clock source type (crystal or external clock), and the default FMPLL settings.
Timer pin default pull configuration	WKPCFG	WKPCFG selects the pull direction (either up or down) for the timer pins of the device. The timer pins are defined as the device pins that have a primary intended use of eTPU and eMIOS functions.

1. BOOTCFG[0] is not available in all packages. For packages without a BOOTCFG[0] pin is sampled as zero.
2. The PLLCFG functions are not required for the MCP5676R.

Since multiple external devices could assert the MCU RESET signal (power supply reset out, debugger, external independent watchdog), all devices connected to RESET should be configured for open drain (or open collector depending on the technology) with a strong pull-up (less than 4.7 K Ω) resistor installed in the system on the RESET signal.

5.1 Boot configuration

The BOOTCFG pins select the boot operating mode of the device. The following table shows the boot options.

Table 20. BOOTCFG configuration

BOOTCFG[0]	BOOTCFG[1]	Description
0	0	Boot from internal flash memory (default)[1]
	1	Boot from FlexCAN or eSCI interface

Table continues on the next page...

5. Multiple steps may be desirable to limit sudden changes in operating current.

Table 20. BOOTCFG configuration (continued)

BOOTCFG[0]	BOOTCFG[1]	Description
1[2]	0	Boot from external memory (no bus arbitration)
	1	Boot from external memory (with external bus arbitration)[3]

1. If no valid boot configuration exists in the internal flash, the device will then go into serial boot mode.
2. BOOTCFG[0] is not available in all package options and defaults to zero. In other words, external boot is not supported in packages that do not have a BOOTCFG[0] pin (324 and 416 PBGA).
3. Bus arbitration is not supported on this device. Therefore, a setting of 0b11 is illegal.

In the normal boot process, the Boot Assist Module looks for a valid Reset Configuration Half-Word (RCHW) in the internal flash at the various possible boot locations. If a valid RCHW is not found, then serial boot mode is entered.

Serial boot mode allows the device to boot over either the eSCI (a simple, standard RS-232D type interface) or via the FlexCAN module. Both interfaces are monitored until activity is seen on one interface. Once an initial activity is seen on an interface, that interface becomes the boot interface. The boot protocol allows software to be downloaded into the device via the serial interface. Control will be passed to that software once loaded into memory. See the documentation for each device for additional information on the serial boot process.

5.2 PLL configuration

NOTE

Since the MPC5676R begins operation using an internal RC oscillator, the PLLCFG signals are not required; all settings of the PLL can be controlled by software, including selection of the crystal reference oscillator or external reference.

The default configuration of the PLL is set by the PLL configuration pins of the device (PLLCFG[0:2]). PLLCFG[0:1] set the basic operating mode as shown in the table below.

Table 21. FMPLL Mode Configuration Selections

PLLCFG[0]	PLLCFG[1]	Clock Mode
0	0	PLL off mode
0	1	Normal mode with external reference
1	0	Normal mode with crystal reference
1	1	Reserved

PLLCFG[2] sets the range of the input frequency. When PLLCFG[2] = 0, then the default predivider is set to divide by two and is reflected in the Enhanced Predivider field (EPREDIV) of the FMPLL Enhanced Synthesizer Control Register 1 (ESYNCR1). Setting PLLCFG[2] = 1 selects the upper range of crystal frequencies and sets the default divider to divide by four.

Table 22. FMPLL Input Frequency Range Select

PLLCFG[2]	Clock input frequency	FMPLL predivider default value (ESYNCR1[EPREDIV]
0	8 to 20 MHz	Divide by 2 (0b0001)
1	16 to 40 MHz	Divide by 4 (0b0011)

The input frequency from the PLL predivider to the PLL must be between 4 and 10 MHz. These default settings ensure that this is true in all cases.

NOTE

Setting the PLLCFG[2] pin high allows the use of either a 16 to 20 MHz crystal (for slightly lower power dissipation) or a 40 MHz crystal to protect for the option of using FlexRay. For the MPC567xF and the MPC5676R, FlexRay requires the use of a 40 MHz crystal (or external reference) to meet the timing requirements of the FlexRay communication network. A 16 or 20 MHz crystal can be used and the FlexRay components can be left out of the module. Or, the crystal could be changed to 40 MHz and the FlexRay driver circuitry can be populated to support FlexRay at a later time without having to change the setting of the PLLCFG[2] pin with a layout change or pull option resistor.

5.3 Weak pull configuration

The default configuration of the pull devices connected to the timer pins of the device can be controlled with the state of the Weak Pull Configuration pin (WKPCFG) during reset. The value of this signal is latched by the device four clocks prior to the negation of $\overline{\text{RSTOUT}}$ (low to high transition). The pull device can either be a pull-up or a pull-down. This default value remains in effect until disabled in the Pad Configuration Register (PCR) for the signal.

Table 23. WKPCFG Configuration

WKPCFG state	Description
0	The pins controlled by the WKPCFG, by default, will have pull-down devices enabled.
1	The pins controlled by the WKPCFG, by default, will have pull-up devices enabled.

The timer pins consist of all the pins for which the primary intended use is either eTPU functions or the eMIOS module. The signals section of the device reference manual or data sheet lists the pins that are controlled by the WKPCFG pin.

NOTE

In some cases where the eTPU or eMIOS function is not the primary intended use of the signal, the WKPCFG does not affect the direction of the pull device. Pins may exist for which eTPU or eMIOS are the primary functions, but are not affected by the state of the WKPCFG pin. Check the device documentation to be sure.

5.4 Minimum reset configuration example

By default, the PLLCFG and WKPCFG external signals have internal weak pull-up devices enabled during and after reset. The BOOTCFG external signals have internal weak pull-down devices enabled. The figure below shows the absolute minimum configuration required to configure the FMPLL to use an external 8 to 20 MHz crystal and to boot from the internal flash. An option to allow selection between internal flash boot and serial boot can be added with a jumper on the BOOTCFG[1] external signal. If the system requires that the timer channels (eTPU and eMIOS) be configured with the internal weak pull-down devices by default, the resistor on the WKPCFG should be installed.

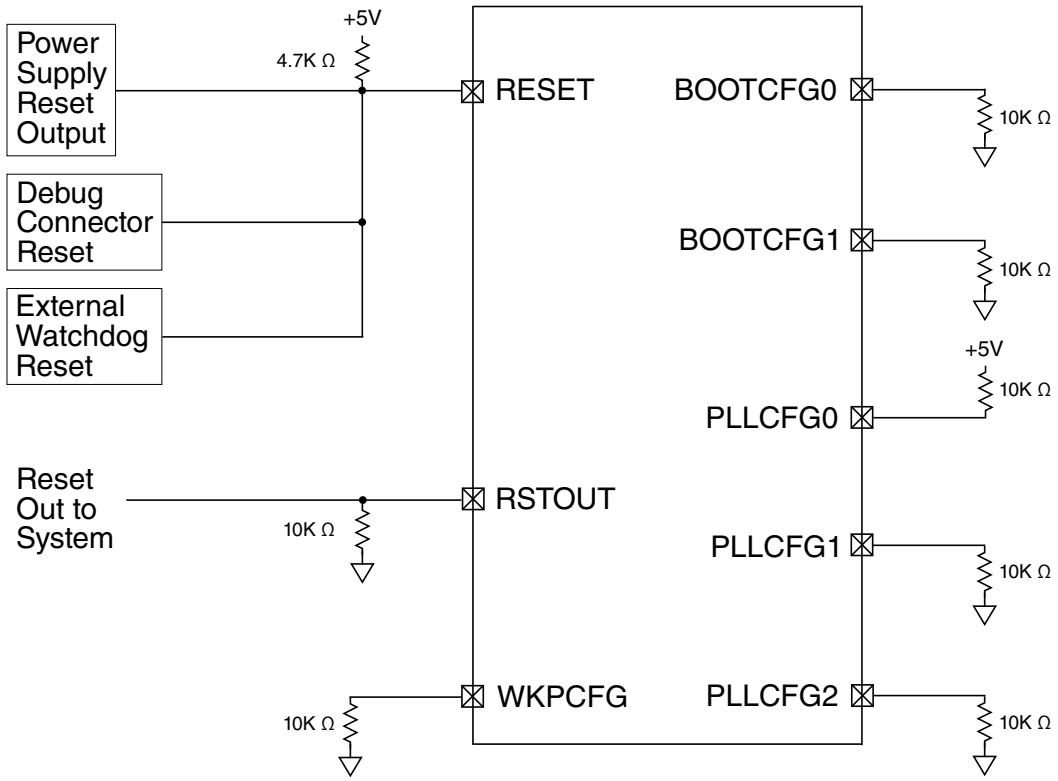


Figure 14. Minimum reset configuration for an 8 to 20 MHz crystal example

The absolute minimum configuration required to configure the FMPLL to use an external 16 to 40 MHz crystal and to boot from the internal flash for the device is shown in the figure below. This configuration is normally used when using a 40 MHz crystal for FlexRay. (FlexRay requires a 40 MHz crystal or external clock source.) This configuration also allows a 16 MHz crystal (for slightly lower current consumption and lower crystal emissions), while providing an option for later conversion to a 40 MHz crystal for using FlexRay.

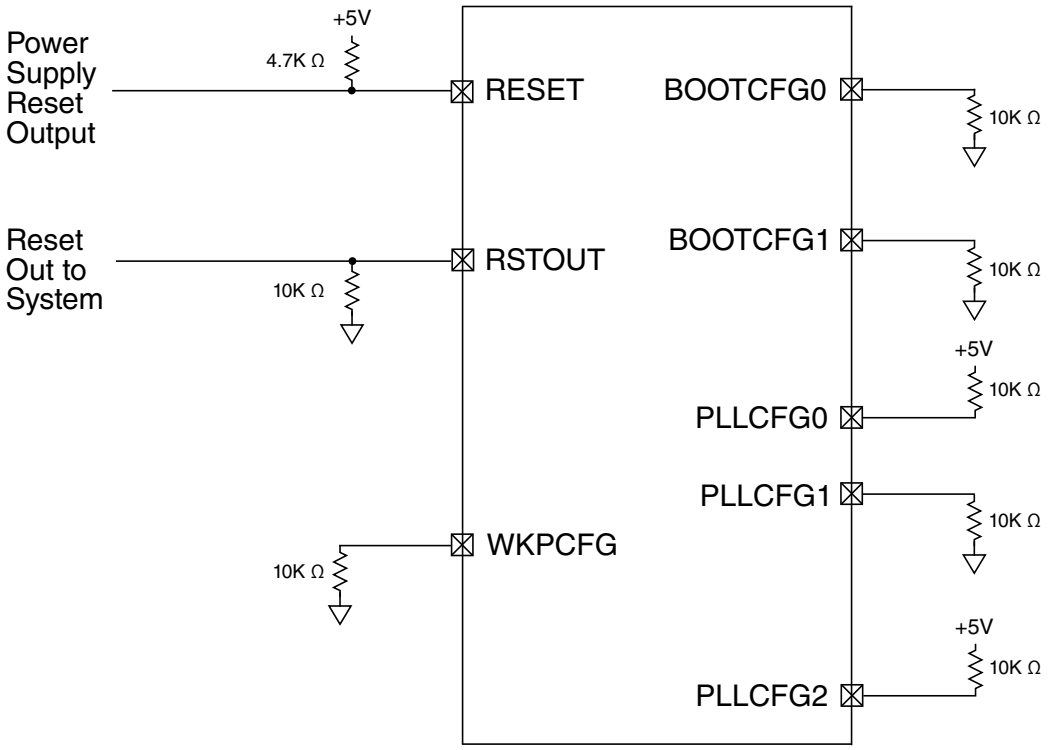


Figure 15. Minimum reset configuration for a 16 to 40 MHz crystal example

5.5 Fully selectable reset configuration example

In some cases (such as an initial prototype/evaluation board/module), a fully selectable option is helpful so as to be able to set any configuration of the PLL options (PLLCFG[0:1]) , boot options (BOOTCFG[0:1]), and timer pins pull default state (WKPCFG). The figure below shows a circuit example.

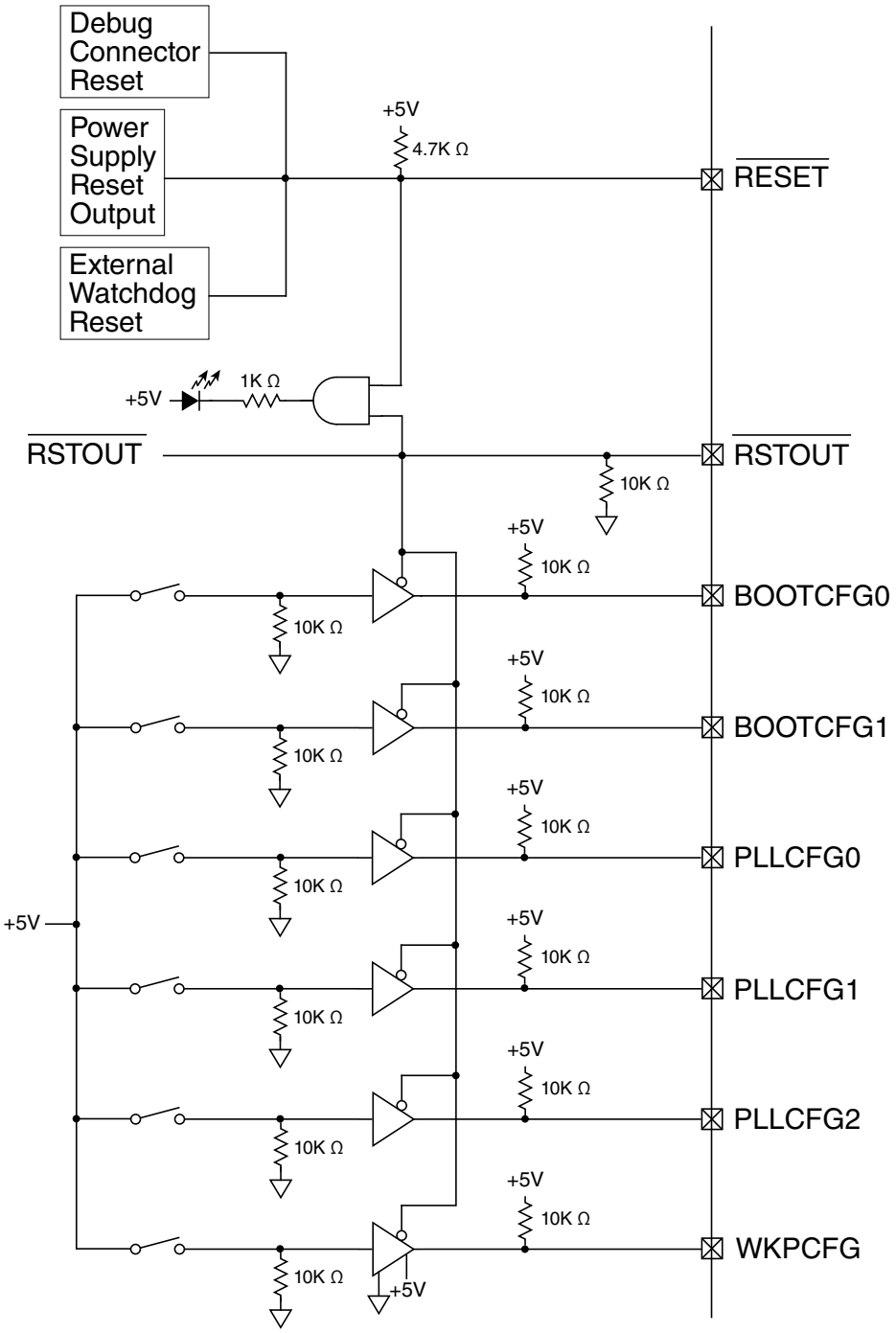


Figure 16. Schematic of fully configurable reset configuration example

5.6 Using the configuration pins for I/O

In some systems, it is a requirement to use the configuration pins (balls) for either input or output functions after the MCU exits reset. During reset the configuration pins need to be in the proper state for configuring the device. Therefore a tristate buffer can be used that is enabled while $\overline{\text{RSTOUT}}$ is asserted (low). After reset, another set of buffers that are enabled when

RSTOUT is negated (high) can be used to either drive the pin or enabled to drive an external signal. When used as an output, the state of the signal during reset should be set by an external resistor. This resistor should be strong enough to overcome any internal resistor on the device that this tristate buffer is driving.

The figure below shows an example circuit that can be used to isolate the configuration pins during and after reset.

NOTE

The tristate buffers used during reset assertion are active low and the buffers used after reset are active high.

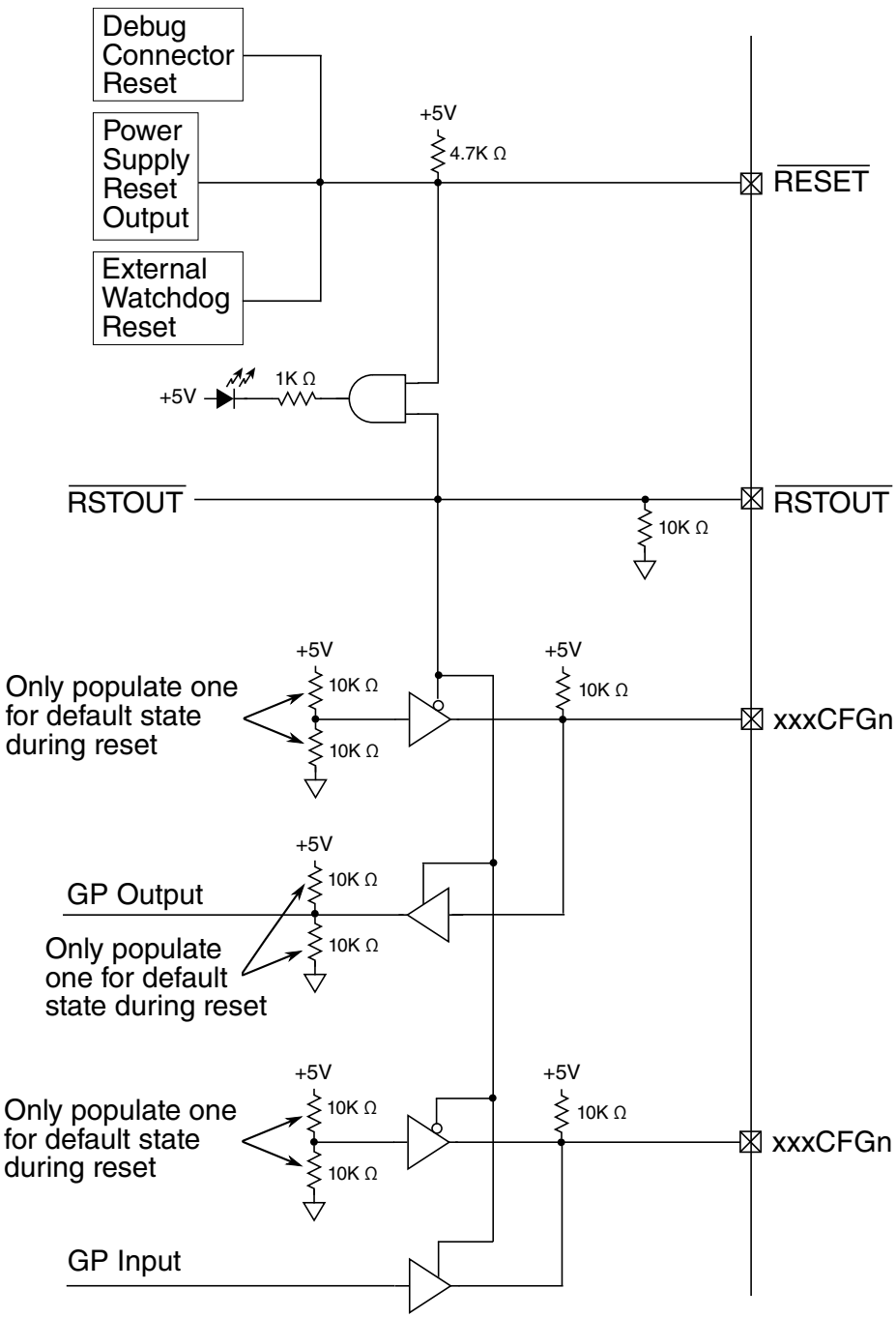


Figure 17. Typical I/O circuitry for configuration signals

6 Recommended debug connectors and connector pin out definitions

The table below shows the recommended connectors for different applications for the MPC567xF and MPC567xR.

Table 24. Recommended connectors

Connector style	Target system part number	Connector type
14-pin BERG JTAG only	3M 2514-6002UB	JTAG-only configuration
25-position (2 × 25, 50-pin) Samtec	Samtec ASP-148422-01	Full Nexus configuration
38-pin MICTOR[1]	Tyco 767054-1[2]	Full Nexus configuration

1. Recommended for backward compatibility only. Not recommended for 16-bit MDO support. The Lauterbach LA-7631 Mictor adapter has four solder pad options for connecting MDO[12:15]. Older interfaces do not support the 16-bit wide mode. Not shown in this document. See AN3968.
2. Other compatible part numbers are 2-5767004-2 (RoHS compliant), 2-767004-2, 767061-1, and 767044-1.

NOTE

Whichever connector is chosen, "keep-out" areas may be required by some tools. Consult the preferred tool vendor to determine any area that must remain clear around the debug connector. Some tool vendors may include an extension cable to minimize "keep-out" areas, but use of an extension will degrade the signal. In many cases, this degradation will be insignificant, but the amount of degradation depends on many factors, including clock frequency and target board layout.

For additional information on the MPC567xF and MPC5676R debug connector options and signal descriptions, see Application Note AN3968, "Nexus Interface Connector for the MPC567xF and MPC5676R."

6.1 MPC5600 JTAG connector

The figure below shows the pin-out of the recommended JTAG connector to support the MPC5600 devices. If there is enough room allowed in the target system, a full Nexus connector is preferred over the simple 14-pin JTAG connector since it allows a higher degree of debug capability. It can be used as a minimum debug access or for BSDL board testing.

The recommended connector for the target system is the Tyco part number 2514-6002UB and the pin-out is shown in the following table.

NOTE

This pin-out is similar to the Freescale MCORE and DSP JTAG/OnCE connector definitions.

Table 25. Recommended JTAG connector pinout

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
$\overline{\text{EVTI}}$[1]	7	8	—
$\overline{\text{RESET}}$	9	10	TMS

Table continues on the next page...

Table 25. Recommended JTAG connector pinout (continued)

Description	Pin	Pin	Description
VREF	11	12	GND
$\overline{\text{RDY}}$[2]	13	14	JCOMP

1. $\overline{\text{EVTI}}$ is optional and was not included in the original (very early) definitions of the JTAG-only connector.
2. The $\overline{\text{RDY}}$ signal is not available on all packages or on all devices. Check the device pinout specification. In general it is not available in packages with 208 signals or less.

NOTE

Freescale recommends that a full Nexus connector be used for all tool debug connections, regardless of whether Nexus trace information is needed. Adapters for a JTAG class 1 14-pin connector (tool side) to the full Nexus MICTOR connectors (board side) are available from P&E Microcomputer Systems (http://www.pemicro.com), part number PE1906, and from Lauterbach (http://www.lauterbach.com), order number LA-3723 (CON-JTAG14-MICTOR). Lauterbach also has an adapter that will connect a MICTOR connector (tool side) to a 14-pin JTAG connector (board side). This adapter is order number LA-3725 (CON-MIC38-J14-5500).

6.2 MPC56xx high-speed parallel trace connector

For high speed trace applications, the MICTOR-38 connector is not optimized for best signal integrity when using more than eight Message Data Out signals (MDO). Twelve MDO pins push the capability of the connector from a signal integrity standpoint. When moving to devices that support the full 16-bit MDO, a Samtec ERF8 series connector is highly recommended. The part number of the Samtec connector is shown in the following table.

Table 26. Recommended high-speed parallel trace connector part number

Connector	Part number (Samtec)	Style	Description
HP50	ASP-148422-01	Samtec ERF8 Series, 25 position by 2 row	Vertical mount for MCU module

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of twenty-five contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity.

The following picture is courtesy of Samtec U.S.A (http://www.samtec.com/search/NEXUS.aspx).

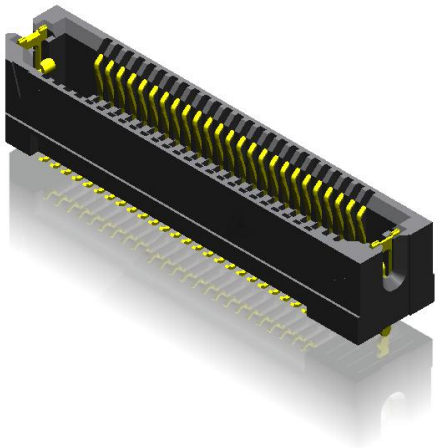


Figure 18. HP50 (ASP-148422-01) connector

The table below shows the recommended pinout for the Samtec connector.

Table 27. MPC56xx high-speed parallel trace connector

Position	Signal	Direction	Pin number	Pin number	Direction[1]	Signal	IEEE-5001-2011 GEN_IO signal name
	GND					GND[2]	
1	MSEO0	Out	1	2	Out[3]	VREF	
2	MSEO1	Out	3	4	In	TCK	
3	GND		5	6	In	TMS	
4	MDO0	Out	7	8	In	TDI	
5	MDO1	Out	9	10	Out	TDO	
6	GND		11	12	In	JCOMP	
7	MDO2	Out	13	14	Out	RDY	
8	MDO3	Out	15	16	In	EVTI	
9	GND		17	18	Out	EVTO	
10	MCKO	Out	19	20	In	RESET	
11	MDO4	Out	21	22	Out	RSTOUT	GEN_IO0
12	GND		23	24		GND	
13	MDO5	Out	25	26	Out	CLKOUT	
14	MDO6	Out	27	28	In/Out	TD/WDT	GEN_IO1
15	GND		29	30		GND	
16	MDO7	Out	31	32	In/Out	DAI1	GEN_IO2
17	MDO8	Out	33	34	In/Out	DAI2	GEN_IO3
18	GND		35	36		GND	
19	MDO9	Out	37	38		ARBREQ	GEN_IO4
20	MDO10	Out	39	40		ARBGRT	GEN_IO5
21	GND		41	42		GND	

Table continues on the next page...

Table 27. MPC56xx high-speed parallel trace connector (continued)

Position	Signal	Direction	Pin number	Pin number	Direction[1]	Signal	IEEE-5001-2011 GEN_IO signal name
22	MDO11	Out	43	44	Out	MDO13	
23	MDO12	Out	45	46	Out	MDO14	
24	GND		47	48		GND	
25	MDO15	Out	49	50		N/C[4]	
	GND[2]					GND[2]	

1. Viewed from the MCU.
2. The connector locking mechanism provides additional ground connections on each end of the connector.
3. This is an output from the connector standpoint. It may or may not be from the MCU.
4. No connection — should be left open. Reserved for MDO16 on devices with more than sixteen MDO signals (future compatibility). In some applications this may be used as an SRAM voltage detect to determine when voltage for a standby SRAM is disconnected.

6.3 Minimum debug external circuitry

In general, other than the connector, no additional circuitry is required for the Nexus/JTAG debug circuitry. The MPC5600 devices include internal pull devices that ensure the pins remain in a safe state. However, if there is additional circuitry connected to the Nexus/JTAG pins, or the signals have long traces, a minimum number of external pull resistors can be added to ensure proper operation under all conditions. Long traces could be affected by other signals, due to crosstalk from high-current or high-speed signals. The recommended external resistors are shown in the following table.

Table 28. Optional minimum debug port external resistors

Nexus/JTAG signal	Resistor direction and value	Description
JCOMP	10 kΩ pulldown	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU.
$\overline{\text{RESET}}$	4.7 kΩ pullup	The $\overline{\text{RESET}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU.
TD/WDT[1]	10 kΩ pulldown	With no tool attached, this signal should be held low and may or may not be connected to a pin of the MCU, depending on the system definition.
$\overline{\text{EVTI}}$	10 kΩ pullup	A pull-up resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. **NOTE:** In almost all situations, a resistor is not required on this signal.
TCK	series isolation resistor	A termination resistor or an isolation (0Ω) resistor may be required in systems that use a debug connector on the VertiCal connector since the TCK signal may have multiple endpoints that can cause reflections.

1. This is an optional signal and is not actually required for the MCU.

In addition to the pull-up and pull-down resistors, some systems may want to use buffers between the Nexus/JTAG connector inputs and the MCU. This will prevent over-voltage conditions from causing damage to the MCU pins. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit to use is the Texas Instruments SN74CBTLV3861[6]. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

NOTE

It is recommended that at least the reduced port configuration Nexus signals be made available (somewhere) on production boards. This facilitates debugging of new boards and analysis of errors in software, even on boards that have restricted space and normally provide a JTAG-only connection. If the Nexus signals are available on the production board, an adapter could be built to provide a Nexus connection on boards that do not have a complete footprint for one of the standard Nexus connectors. Likewise, the JTAG connector does not have to be populated on production boards and could even utilize a smaller connector footprint that could be used with an adapter to the standard debug connections.

In systems that use a VertiCal mounted debug connector and have a JTAG connector/footprint in the target system, termination may be required on the JTAG Test Clock (TCK) to avoid ringing due to the multiple signal endpoints.

7 Monitoring internal analog signals

Many of the PMC reference and output voltages can be monitored by the on-chip analog-to-digital converter (eQADC). These can be monitored by the application software. Some of these signals can be converted by only one of the on-chip ADCs. The available PMC signal channels are shown in the following table.

Table 29. Power supply ADC monitor channels

ADC Channel	ADC	Description
128	ADC0, ADC1 of eQADC_A	Temperature sensor
145	ADC0 of eQADC_A	PMC band gap voltage (0.62 V)
146	ADC0 of eQADC_A	VDD 1.2 V analog supply
147	ADC0 of eQADC_A	1.2 V Output output / 2.045
162	ADC0 of eQADC_A	VDDEH1 50%
163	ADC0 of eQADC_A	VDDEH3 50%
164	ADC0 of eQADC_A	VDDEH4 50%
165	ADC0 of eQADC_A	VDDEH5 50%
166	ADC0 of eQADC_A	VDDEH6 50%
167	ADC0 of eQADC_A	VDDEH7 50%
180	ADC0 of eQADC_A	1.2 V supply low voltage detect voltage / 1.774
181	ADC0 of eQADC_A	3.3 V supply / 5.460

Table continues on the next page...

6. SN74CBTLV3861-Q1 is automotive qualified if required.

Table 29. Power supply ADC monitor channels (continued)

ADC Channel	ADC	Description
182	ADC0 of eQADC_A	VDDSYN 3.3 V supply low voltage detect / 4.758
183	ADC0 of eQADC_A	VDDREG low voltage detect / 4.758 when the 1.2 V regulator is in linear mode, VDDREG low voltage detect / 7.032 when the 1.2 V regulator controller is in switched mode
196	ADC1 of eQADC_A	VDDA low voltage detect voltage / 3.8934

8 eQADC overview

The MPC567xF and MPC567xR each include two separate enhanced Queued Analog-to-Digital Converters (eQADC). Each eQADC module contains two actual analog-to-digital converters (ADC). The ADC supports both single-ended and differential analog inputs. In addition, on the differential channels the eQADC modules support programmable pull-up and pull-down resistors to allow for on-chip biasing of the external differential signals. These internal resistors can be independently controlled to allow diagnostics to be performed on the analog channels to check for shorts to ground, shorts to 12 V, and open circuits (no sensor) by switching the different resistors in and out and by performing single-ended conversions of both halves of the differential channel pair. In addition, the differential channels provide a programmable gain stage that allows a unity gain, gain of two, or gain of four. Any output value from the ADC can be routed to a separate decimation filter that provides either decimation only, a filtered result through a 16-bit fourth-order IIR (Infinite Impulse Response) filter, or an eighth-order FIR (Finite Impulse Response) filter.

The block diagram below of the eQADCs shows the four (total) ADCs. The majority of the analog inputs are connected to either eQADC_A or to eQADC_B. However, there are some channels that are shared between the two modules. This is also shown in the figure below. A more detailed input model is shown in MPC567xF and MPC5676R ADC Input Model (Appendix B).

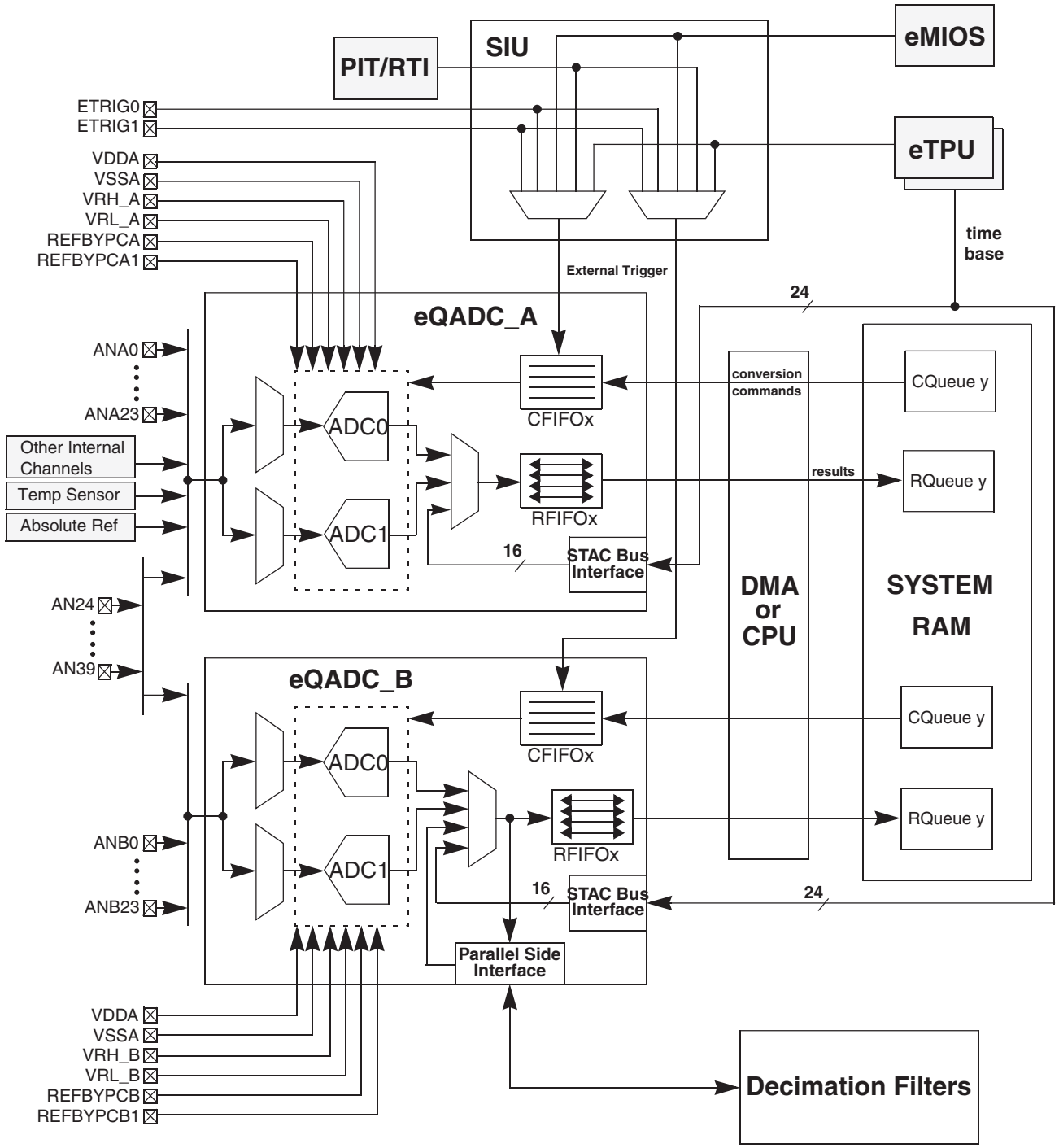


Figure 19. MPC567xF and MPC567xR ADC Sub-system

Internal to the device package, there are separate connections to the die for the analog power (VDDA_AN) and the digital power (VDDA_DIG) supplies to the eQADC module. These are connected inside the package for a single VDDA pin (or ball). Likewise, the analog (VSS_AN) and digital (VSS_DIG) grounds are isolated internal to the package.

Each eQADC can have up to four differential analog channels. There are sixteen channels that are shared between both eQADC modules.

Table 30. Number of external ADC channels

Module	Channel type	Total channels when using the maximum differential channels	Total channels when no differential channels are used
eQADC_A	Differential channels	4	8
	Dedicated single channels	16	16
eQADC_A and eQADC_B	Shared A and B single-ended channels	16	16
eQADC_B	Differential channels	4	8
	Dedicated single channels	16	16
Total ADC channels		56[1]	64[2]

1. Of these 56 channels, 8 are differential channels.
2. No differential channels.

The eQADC provides the capability of expanding the number of analog inputs by using external multiplexers. Up to eight external multiplexers can be used. The external multiplexers require three digital pins that are used as multiplexer address select signals. An external multiplexer can only be used with one of the eQADC modules, either eQADC_A or eQADC_B. This is selectable by software. The external multiplexers feed the analog signals into eight ADC channels. This allows up to fifty-six additional channels (sixty-four externally multiplexed analog signals minus the eight channels that are lost for the multiplexed inputs).

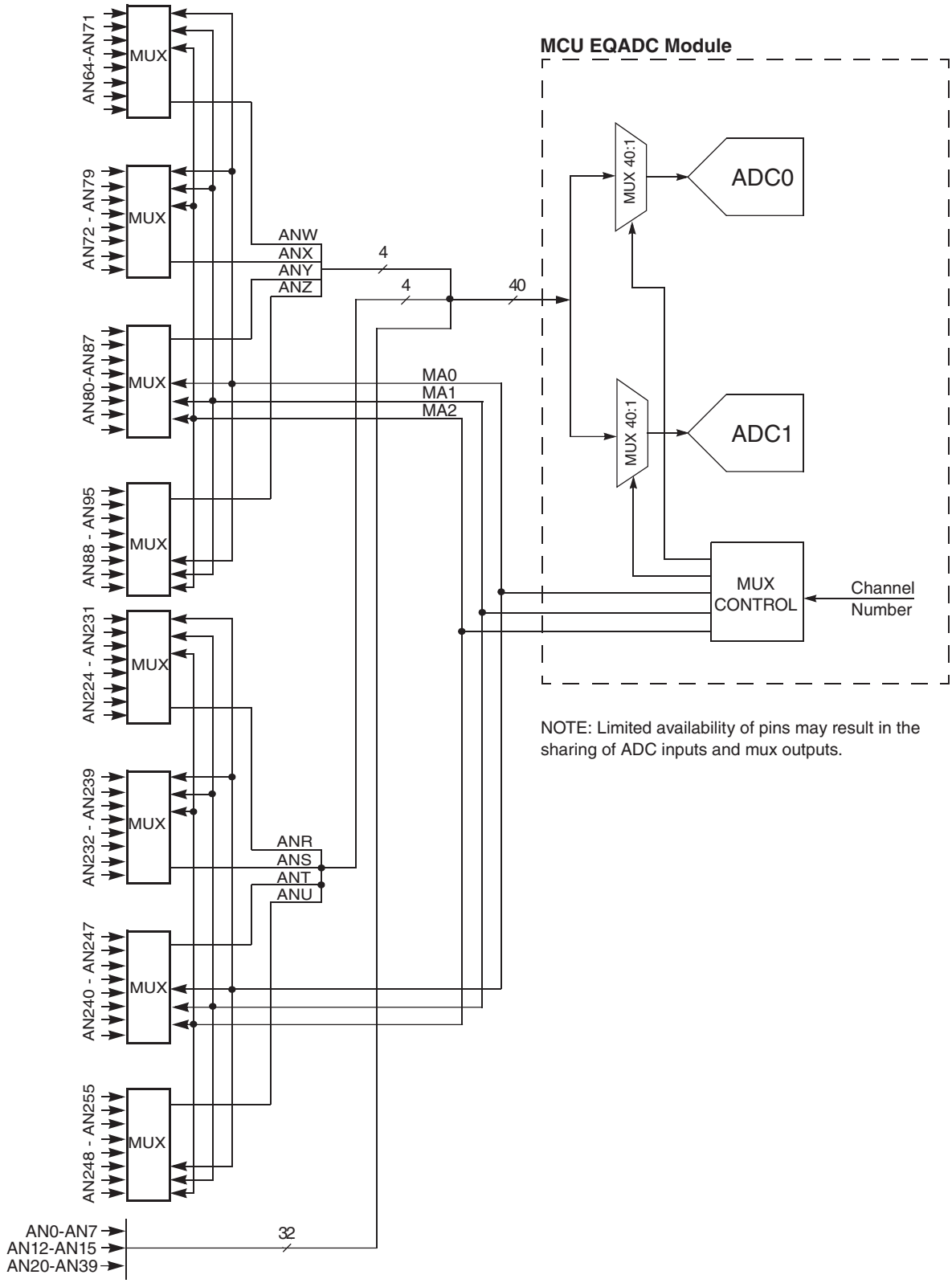


Figure 20. External multiplexer options

NOTE

Not all devices support the ANR, ANS, ANT, and ANU inputs.

In addition, the following board schematic and layout guidelines should be followed:

- Isolate the analog power supplies (VDDA) from digital power supplies (see eQADC (analog) power supply connections).
- Isolate analog traces from digital high-frequency traces
- Incorporate robust bypassing of power supplies (analog and digital supplies) to ensure lowest possible voltage ripple on the power supplies (see the bypassing guidelines eQADC (analog) power supply connections)
- Use linear power supplies when possible, or minimize or isolate the switching noise when using a switching power supply
- Incorporate low-pass filter on ADC inputs to remove unwanted higher frequency components as shown in the following sections

The eQADC requires calibration before it can be used. See AN2989 "Design, Accuracy, and Calibration of Analog to Digital Converters on the MPC5500 Family" for information on calibrating the eQADC.

8.1 eQADC single-ended analog input example

The figure below shows a typical single-ended analog input circuit. The resistor and capacitor values will vary depending on the circuitry connected to the analog input. The values shown may not be appropriate for all types of signal input. There are several criteria required for selecting this circuitry that depend on the source impedance, the maximum voltage allowed (including under error conditions), the required accuracy (including resolution), and the actual specifications of the ADC of the MCU (input impedance, and injection current limits). Care should be taken (by sizing the series resistor) to keep the currents within the injection limits of the device (see the device data sheet). In addition, in some environments. additional protection may be needed. However, the resistors and capacitors shown provide some protection, along with the MCU on-chip ESD protection diodes, for over current and over voltage conditions. See Injection Current section later in this document.

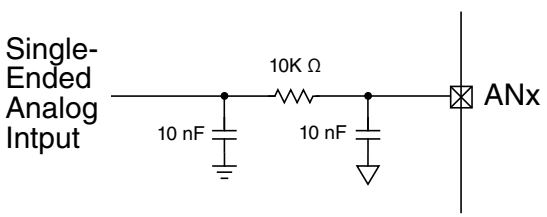


Figure 21. Typical single-ended analog input

The approximate filter cut off frequency is shown in the following equations. For the equations, the following definitions apply:

- R is the series resistor value (ohms)
- C is the capacitor value (farads)

$$\text{Filter\_Cut\_Off\_Frequency} = \frac{1}{2(\pi)(R)(C)}$$

Figure 22. RC filter frequency calculation

$$\text{Filter\_Cut\_Off\_Frequency} = \frac{1}{2(\pi)(10K)(10\text{nF})} = \frac{1}{2(3.14)(0.0001)} = 1.592\text{KHertz}$$

Figure 23. Example filter frequency

In addition, if the incoming signal is being measured at a repetitive sample rate without other channels being converted, compensation may be required as the ADC sampling capacitor may begin to appear as a resistive component and therefore create a resistor divider. For the following equation, the follow definitions apply:

- C_s is the internal ADC sample capacitance, this is approximately 0.5 pF for the eQADC in the MPC5600 family process (farads).
- F_s is the sample rate (repetitive rate, not the clock frequency of the ADC itself). In this example 200 thousand samples per second is used (Hertz).

$$\text{Filter\_Sample\_Rate\_Equivalent\_Resistance} = \frac{1}{(Cs)(Fs)} = \frac{1}{(0.5\text{pF})(200K\text{samples/sec})} = \frac{1}{1x10^{-7}} = 10M$$

Figure 24. Sample rate equivalent resistance

Taking this equivalent resistance in to account results in a slight reduction in the voltage that is actually seen by the ADC.

- R is the external series filter resistor (ohms)
- R_s is the internal routing resistance (ohms)
- R_{equ} is the equivalent resistance due the switched capacitor effect of the internal sample capacitor (ohms).
- V_{in} is the input voltage into the filter network (volts).

$$\text{ADC\_Actual\_Equivalent\_Voltage} = \frac{\text{Requ}}{(R+\text{Rs}+\text{Requ})}(\text{Vin}) = \frac{10M}{(10K+8K+10M)}(\text{Vin}) = \frac{10M}{10.028\text{M}} = 99.7\,\%\,(\text{Vin})$$

Figure 25. Actual ADC voltage

8.2 eQADC differential analog input example

The figure below shows a typical differential analog input circuit.

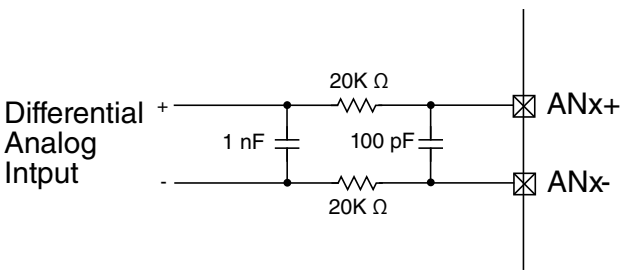


Figure 26. Typical differential analog input

The differential inputs are limited to a maximum differential amplitude of 2.5 V. The signal should be biased around the mid supply of the references = (VRH - VRL)/2. See the device data sheet for the allowable differential offset voltage from the mid-point, however, it is typically ± 5% of (VRH-VRL). This is shown in the following figure.

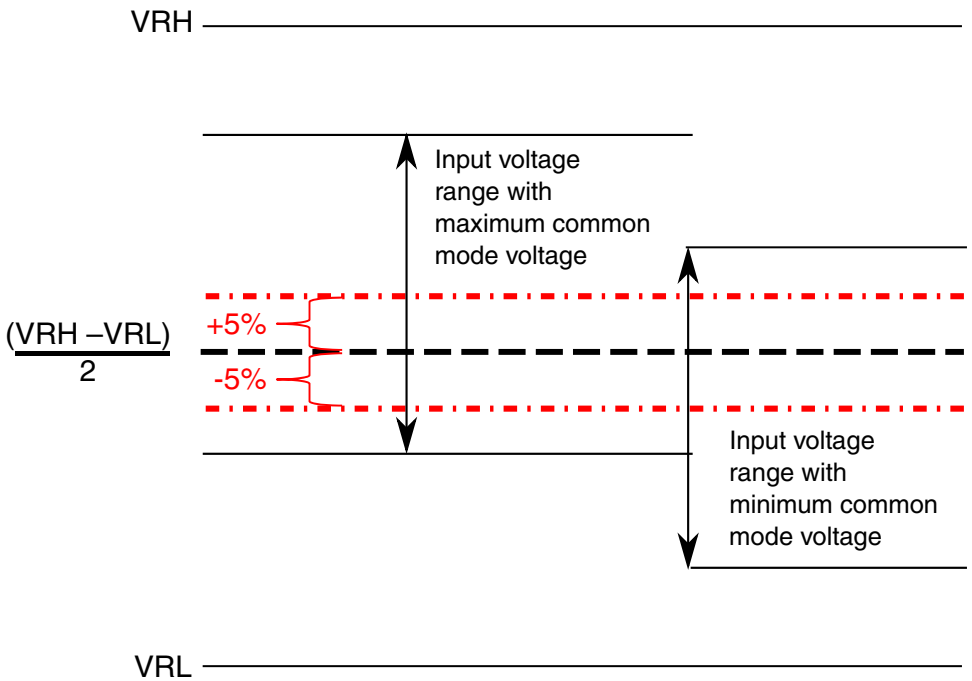


Figure 27. Differential voltage range (Gain = x1)

Another feature of the differential inputs of the eQADC is a variable gain amplifier[7]. This "amplifier" can be enabled in the ADC conversion command and can be set to a gain of two (x2) or a gain of four (x4) (normally the gain is set to one). It should be noted that when the x2 or x4 gain is enabled, the maximum input voltage level of the ADC is reduced. See the following table.

Table 31. Maximum differential input voltage for the different gain settings

Gain Setting	Maximum Differential Voltage[1]
x1	±2.5V
x2	±1.25V
x4	±0.625V

1. Although the eQADC cannot accurately convert voltages greater than a differential voltage 2.5V (x1 gain), 1.25V (x2), or 0.625V (x4), the inputs will not be damaged by voltages that are within the range of VRL to VRH.

An additional feature available on the differential inputs is bias resistors. Three values of pull-up and pull-down resistors are available on each of the differential pins. In addition to providing a DC bias voltage for AC signals, these resistors can be used to perform some diagnostic tests by enabling different combinations and determining the effect on the input voltages.

7. This gain stage is actually not implemented as a traditional op-amp and therefore does not have the normal amplifier specifications. The gain is implemented by the controlling the references to the ADC. However, the performance of the "amplifier" stage is included in the integral nonlinearity (INL) and differential nonlinearity (DNL) specifications of the ADC.

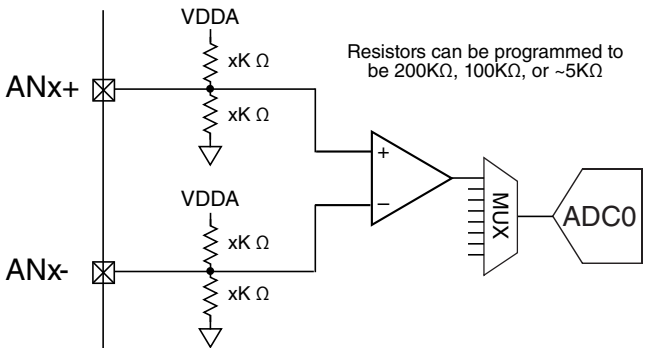


Figure 28. Differential ADC input pull up and pull down resistors

NOTE

Some documentation shows that the pull-up and pull-down resistors are connected to VDDE, this is due to the generic designation that VDDE stood for an external power supply. The pull-up resistors are connected to the external analog power supply (VDDA) on devices.

The following table shows the specifications of the bias resistors (from the MPC567xF Data Sheet, revision 8). In addition to the value specifications, there is an additional specification on the 100KΩ and 200KΩ resistors, matching. The ratio of the pull up and pull down resistors match within 2.5%. This specification does not apply to the ~5KΩ resistor.

Table 32. ADC pull-up and pull-down resistor specifications

Description		Minimum	Maximum	Units
Weak pull-up/pull down resistance 200KΩ selected		130	280	KΩ
Weak pull-up/pull down resistance 100KΩ selected		65	140	KΩ
Weak pull-up/pull down resistance 5KΩ selected	MPC567xF	1.4	7.5	KΩ
	MPC576R	1.4	5.2	KΩ
Pull-up/down matching ratio (100K and 200K resistors only)		-2.5%	2.5%	—

8.3 Decimation Filter

Some devices include one or more Decimation Filters. The Decimation Filter block implements a multiply-accumulate (MAC) unit capable of implementing a 16-bit, 4th order IIR or 8th order FIR filter. On devices with multiple decimation filter blocks, the blocks can be cascaded to form higher order filters. In addition, the output data can be decimated (reduce the number of samples) at a programmable rate from 1 to 16. Optionally, a 32-bit integrator can be included to sum a series of signed or absolute value filter outputs. The Integrator can select-ably be placed before or after the decimator. The integrator can be operated in multiple modes: windowed, continuous mode, or controlled mode. In controlled mode, signals from the eTPU can be used to start, stop, reset, or read the output of the integrator.

Table 33. Device Decimation Filter implementations

Device	Number of Decimation Filter blocks	Integrator	Integrator trigger sources	Accessibility
MPC567xF	8	Yes	eTPUA, eTPUB	eQADC B only
MPC5676R	12	Yes	eTPUA, eTPUB, eTPUC	eQADC A and B

A block diagram of the Decimation filter is shown in the following figure.

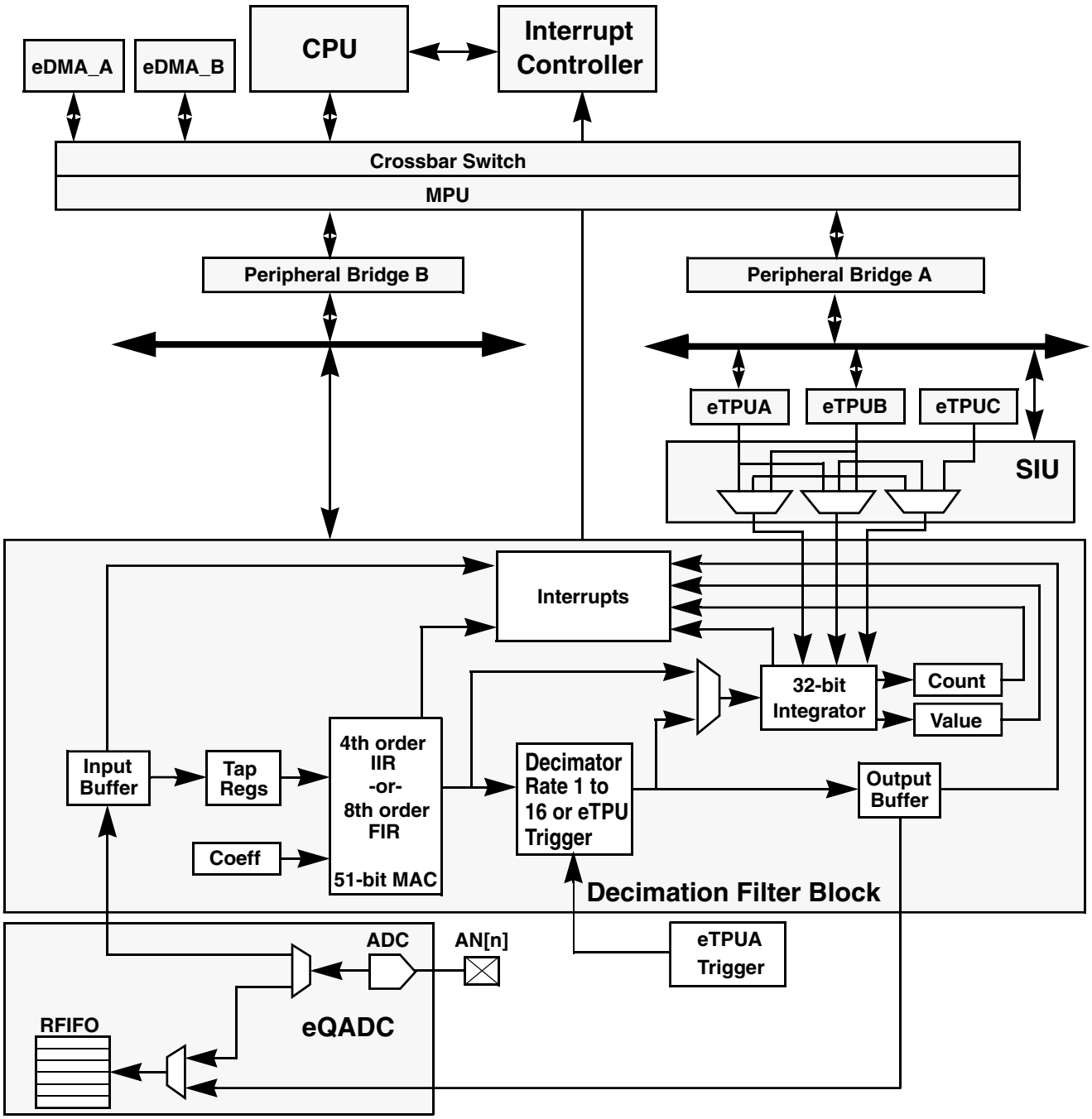


Figure 29. MPC5676R Decimation Filter block diagram with device integration details

9 Example communication peripheral connections

There are a wide range of peripheral pins available on the MCUs. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as LIN, CAN, FlexRay, and RS-232 communication interfaces.

The table below summarizes the maximum communication speed and general overview information of the different types of interfaces.

Table 34. Communication module comparison

Common name	Standard	Distributed timebase	Speed (maximum Kbits/second)	Channels	Time triggered	Arbitration
RS-232D	EIA RS-232 revision D	No	115.2	Single	No	None (optional flow control)
K Line	ISO 9141	No	150[1]	Single	No	None
LIN	LIN 1.0, LIN 2.0, and LIN 2.1[2]	No	100[3]	Single	No	None (master/ slave)
CAN	Bosch 2.0B ISO11898	No	1,000[4]	Single	No (additional function)	CSMA[5]
FlexRay	FlexRay	Yes	10,000	Dual	Yes	TDMA[6]

1. Typical speed is 10.4Kbits/s.
2. Many Freescale devices only support the LIN 1.0 and 2.0 standards. LIN2.1 requires a different sampling scheme covered by an erratum to the LIN standard..
3. Typical speed is 10 or 20 Kbits/s, but supports a fast mode of 100 Kbits/s.
4. Two different speed classes are supported by CAN, a fast (250K to 1Mbits/s) and a low speed CAN (5K to 125Kbits/s).
5. Carrier Sense Multiple Access
6. Time Division Multiple Access

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system. The below figure shows a typical protection circuit.

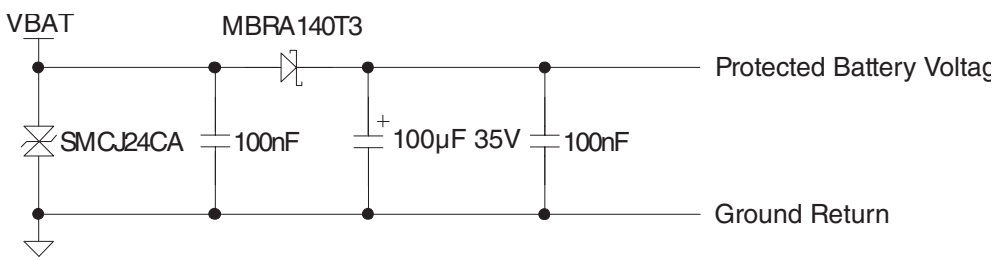


Figure 30. Typical protection circuit

9.1 Example LIN interface for eSCI

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

On many of the Freescale automotive MCUs, the enhanced Serial Communication Interface (eSCI) module implements Local Interconnect Network (LIN) interface. This same module (eSCI) also supports the standard Universal Asynchronous Receiver/Transmitter (UART) functions (with a different physical layer device).

The following figure shows a typical interface implemented using the Freescale MC33661 LIN transceiver.

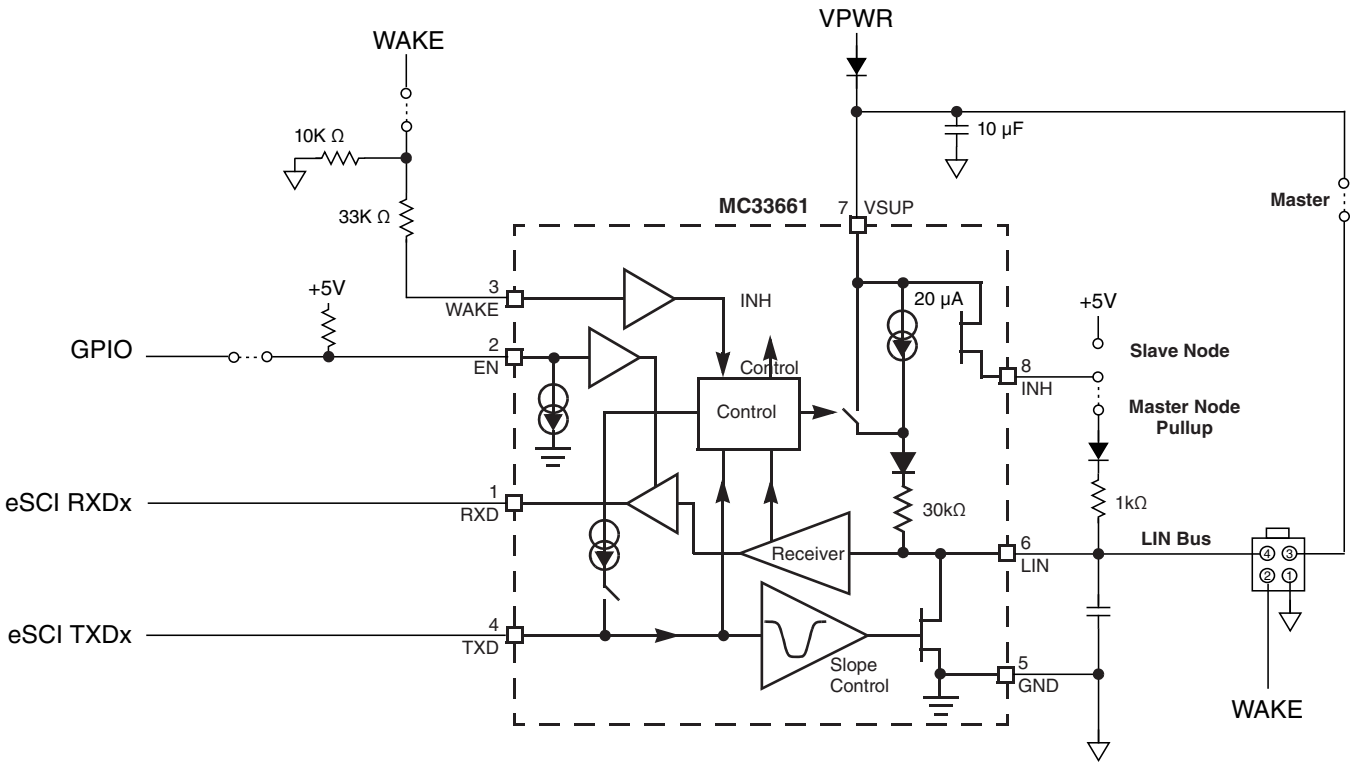


Figure 31. Typical eSCI to LIN connections

The table below shows the pins of the MC33661 and their typical connections to an MCU.

Table 35. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN Receive Data Output to the MCU.
2	EN	Input	Enable Control	MCU GPIO	Enables operation of the device.
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Wake enables the devices out of sleep mode.
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN Transmit Data Input from the MCU.
5	GND	Input	Ground	System Ground Reference	Device ground reference.
6	LIN	Input/Output	LIN Bus	LIN bus	Bidirectional pin that represents the single-wire transmit and receiver.
7	VSUP	Input	Power Supply	Protected battery voltage	This is the power supply for the device and is typically connected to a nominal 12 V.

Table continues on the next page...

Table 35. MC33661 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
8	INH	Output	Inhibit Output	LIN Bus (if master)	The Inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus on master nodes.

1. Wake is an optional signal on the LIN connector, but may come directly from a switch.

There is no standard industry-defined LIN connector. Freescale uses a 4-pin Molex that allows for the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. The Freescale Molex connector definition is shown in the following table.

Table 36. LIN connector pin-out recommendation

Function	Pin number	Pin number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN Bus - This is the single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.
- VPWR - This connector input can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- Wake - The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, turn on the MCU that controls a function inside the vehicle, such as power a smart dome light or enable the controls of a smart seat.
- Ground - Ground reference for the module.

Part numbers for the 4-pin Molex Mini-Fit Jr.™ connector are shown in the table below.

Table 37. Recommended 4-pin Molex Mini-Fit Jr.™ connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-30-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts, latch	39-29-5043

Table continues on the next page...

Table 37. Recommended 4-pin Molex Mini-Fit Jr.™ connector part numbers (continued)

Description	Manufacturer part number (Molex)
Mating connector with latch for cable assemblies	39-01-2040
Female terminal for mating cable assembly	39-00-0077

9.2 Example RS-232 interface for eSCI

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that was once available on nearly all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals though other interfaces, such as USB. RS-232 was intended to be a very low-cost, low-performance interface. This interface was originally specified with signal voltages of +12 V and -12 V typically. However, this has been lowered to a typical minimum voltage of +5 V and -5 V in recent years.

On many of the Freescale automotive MCUs, the enhanced Serial Communication Interface (eSCI) module implements the standard Universal Asynchronous Receiver/Transmitter (UART) functions. This same module (eSCI) also supports the Local Interconnect Network (LIN) interface (with a different physical layer device).

The figure below shows the typical connections between the serial port of an MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments (http://www.ti.com/). The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature range of -40 to +125° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore the commercial device can be used for prototyping purposes. TI does offer a device option with an operating temperature range of -40 to +85° C. TI has an enhanced version of the device, MAX3232-EP, which is intended for aerospace, medical, and defense applications. This version is available with an operating temperature range of -55 to +125° C.

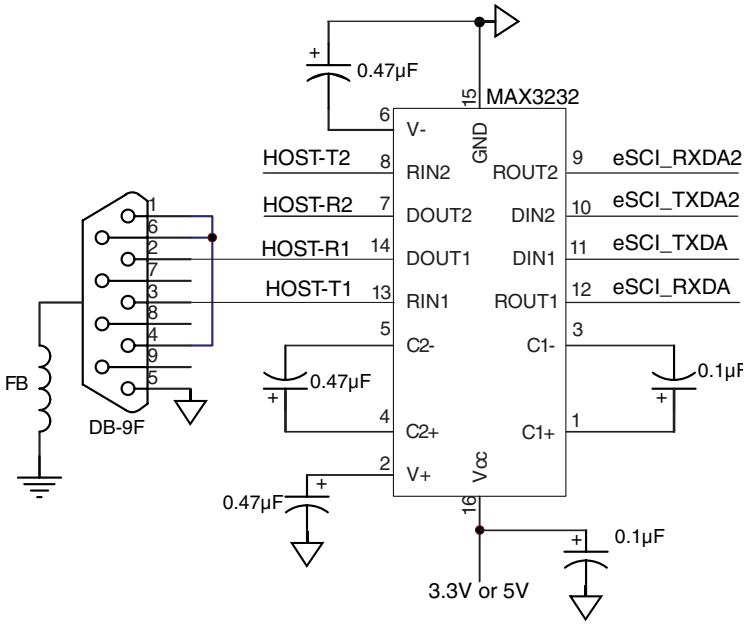


Figure 32. Typical eSCI to RS-232D circuit

The following table shows the standard connection of the RS-232 connector, as used on the Freescale evaluation boards.

Table 38. Typical RS-232D Connector Definition

6 Connect to pin 1 and 4	**1** Connect to pin 4 and 6
7 N/C	**2** RS-232 TX (Transmit)
8 N/C	**3** RS-232 RX (Receive)
9	**4** Connect to pin 1 and 6
	5 GND

NOTE

N/C pins are not connected.

Shell of connector should be connected through a ferrite bead to ground.

9.3 Example K LINE interface for eSCI

ISO9141, also known as K Line, is a low-speed diagnostic interface that provides a bi-directional half-duplex single-wire communication channel. A K Line interface can be implemented with a standard UART type function, such as is implemented in the eSCI module of the devices in Freescale's MPC5500 and MPC5600 families. The K Line interface is used primarily for a low cost on-board diagnostic interface.

The MC33200 implements a K line interface in an 8-pin SOICN package. Features of the MC33290 are:

- Operation over wide supply voltage of 8.0 V to 18 V
- Operating temperature of -40 to 125 °C
- Interface directly to standard CMOS microprocessors
- ISO K Line pin protected against shorts to ground
- Thermal shutdown with hysteresis
- ISO K Line pin capable of high currents
- ISO K Line can be driven with up to 10 nF of parasitic capacitance

- 8.0 kV ESD protection attainable with few additional components
- Standby mode: no battery current drain with VDD at 5.0 V
- Low current drain during operation with VDD at 5.0 V

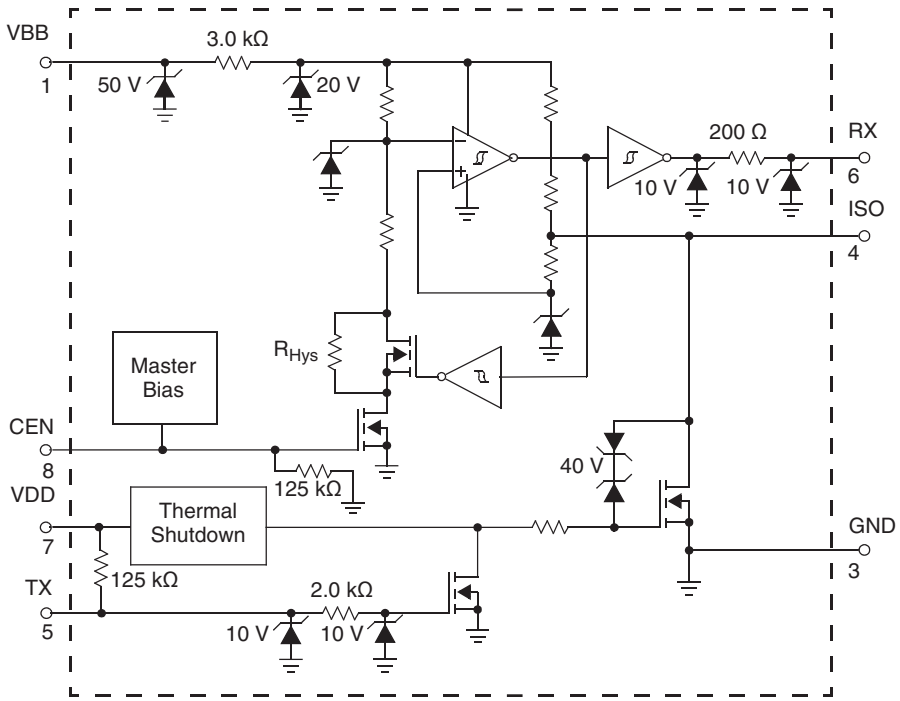


Figure 33. MC33290 block diagram

The following figure shows a typical interface between the MCU and the MC33290.

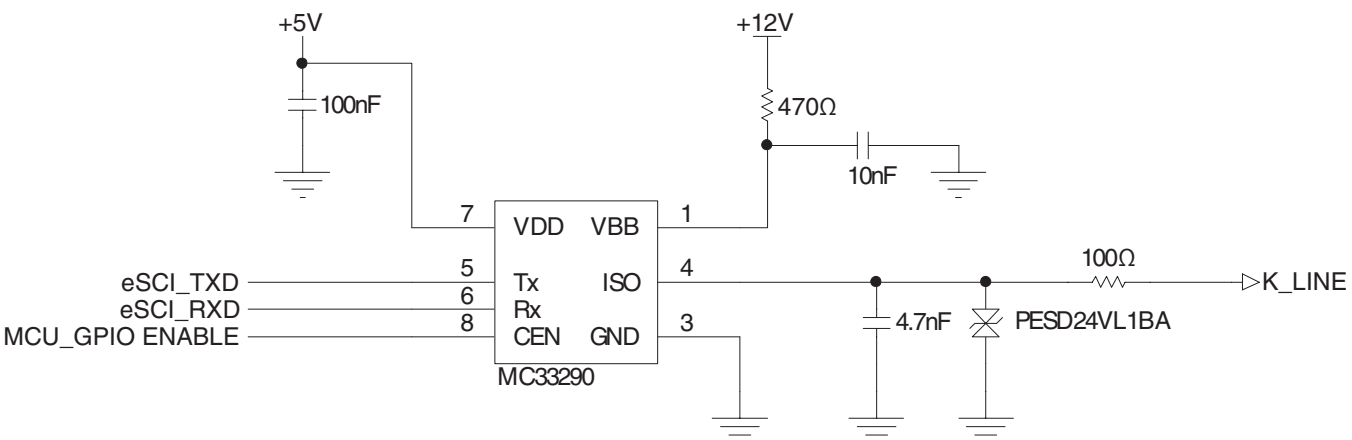


Figure 34. Typical eSCI to K Line connections

The following table shows the pins of the MC33290 and the typical connection in a target system.

Table 39. MC33290 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	VBB	Input	Battery Voltage	Protected battery voltage	VBB is the protected battery voltage supply for the device. It should have a reverse bias

Table continues on the next page...

Table 39. MC33290 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
					protection diode and a series resistor to the over-voltage protected battery.
2	NC	—	—	None	This pin should have no connection in the system.
3	GND	Input	Ground	Ground	Ground reference and power return for the device.
4	ISO	Input/Output	ISO9141 bus	K-Line connector	ISO9141 bus connection.
5	TX	Input	Transmit data input	eSCI TXD	Input data to be transmitted on the ISO bus.
6	RX	Output	Receive Data Output	eSCI RXD	Output of the data received on the ISO bus.
7	VDD	Input	Digital Interface logic supply	5 V supply	Logic power source.
8	CEN	Input	Chip Enable	MCU GPIO (output)	Chip enable for the MC33290.

NOTE

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system.

Typically Freescale does not include a K Line connector; therefore no standard connector is defined.

9.4 CAN interface circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The number of CAN modules on-chip varies from device to device. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pullup resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed.

Freescale CAN modules conform to CAN protocol specification version 2.0 B, and the transceivers shown in this application note comply with ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 Kbit/s to 125 Kbit/s) or a high speed (250 Kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

Freescale has a high-speed standalone CAN physical interface device with built-in diagnostic capabilities (MC33902), as well as CAN transceivers integrated with other functions[8]. Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 40. NXP CAN transceiver comparison

	TJA1050	TJA1054	TJA1040	TJA1041
Bitrate (Kbit/s)	1000	125	1000	1000
Modes of operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep

9.4.1 High-speed CAN with diagnostics: MC33902 interface

For target systems that require full diagnostics of the CAN interface, the Freescale MC33902 high-speed CAN transceiver is available. Features of this device are:

- High-speed CAN interface for baud rates of 40 Kbit/s to 1.0 Mbit/s
- Compatible with ISO 11898 standard
- Single supply from battery
- I/O compatible from 2.75 V to 5.5 V via a dedicated input terminal (3.3 V or 5.0 V logic compatible)
- Low-power mode with remote CAN wakeup and local wake-up recognition and reporting
- CAN bus failure diagnostics and TXD/RXD pin monitoring, cold start detection, and wake-up sources reported through the ERR pin
- Enhanced diagnostics for bus, TXD, RXD, and supply pins available through pseudo-SPI via existing terminals EN, STBY, and ERR
- Split terminal for bus recessive level stabilization
- INH output to control external voltage regulator

A block diagram of this transceiver is shown below.

8. An example device is the MC33905 that includes a 5 V power supply controller, a CAN transceiver physical interface, and a LIN transceiver physical interface.

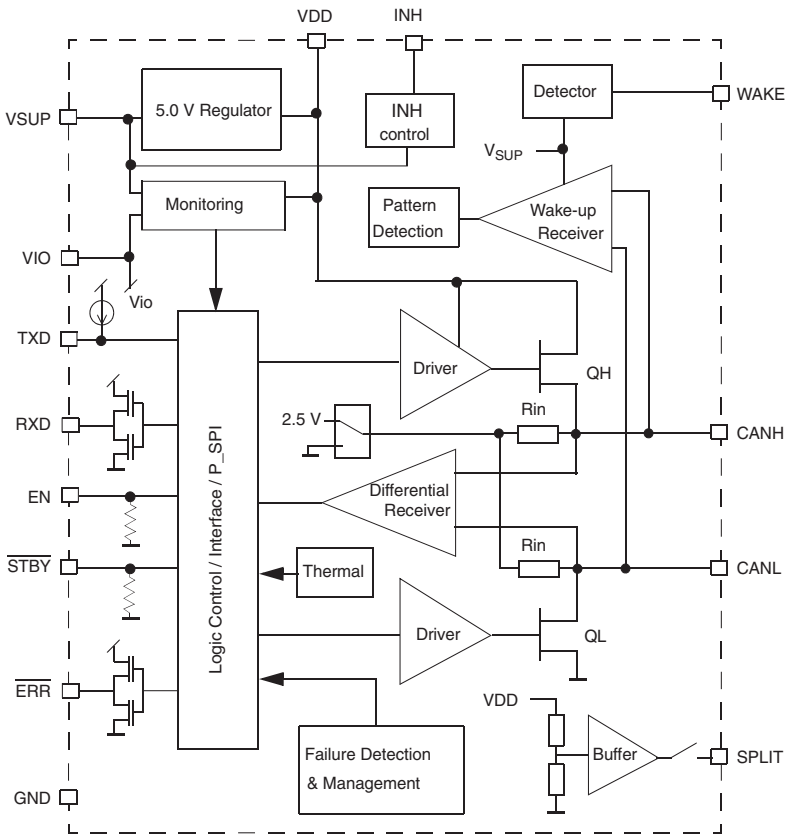


Figure 35. MC33902 block diagram

While a full SPI interface is not available for the diagnostic information, a quasi-SPI interface is available to communicate to the MCU. This interface is referred to as the P_SPI interface in the MC33902 data sheet.

The figure below shows an example schematic using the MC33902.

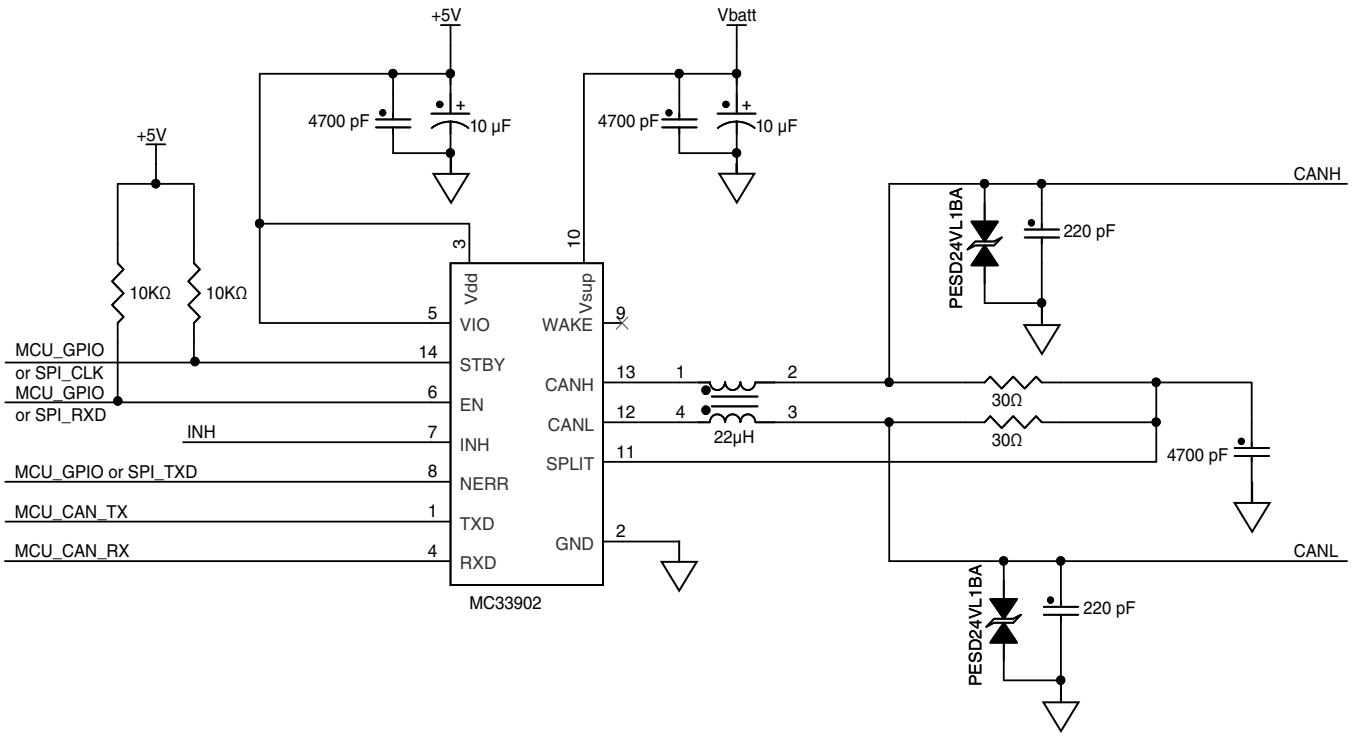


Figure 36. Typical high-speed CAN circuit using the MC33902

NOTE

- Decoupling and Bus protection shown as an example only.

The table below shows the pins of the MC33902 and the possible connections to a MCU and the target system.

Table 41. MC33902 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground termination
3	VDD	Output	VDD Internal Regulator Output	Bypass capacitors only	5 V power supply output. Requires external bypass capacitors.
4	RXD	Output	Receive Data	MCU CAN TXD	CAN receive data output to the MCU
5	VIO	Input	Voltage Supply for IO	3.3 V or 5 V	Supply voltage input for the digital input and output pins. This should be matched to the IO voltage supply of the MCU. Most typically, this is 5 V, but could also be 3.3 V.
6	EN	Input	Enable	MCU GPIO or SPI transmit data output	This is the enable input for the device in static mode control. This is the master output/slave input when used in SPI mode, and the MOSI (master out, slave in) during SPI operation.

Table continues on the next page...

Table 41. MC33902 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
7	INH	Output	Inhibit	Use depends on intended operation (see text below)	Inhibit output for control of an external power supply regulator
8	$\overline{\text{ERR}}$	Output	Active Low Error	MCU GPIO or SPI receive data input	Pin for static error and wakeup flag reporting MISO (master in, slave out) during SPI operation
9	WAKE	Input	Wake	MCU GPIO (output)	Wake input
10	VSUP	Input	Voltage Supply	Battery voltage	Battery supply pin, nominally 12 V
11	SPLIT	Output	Split	CAN termination midpoint	Output for connection of the CAN bus termination middle point
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
14	$\overline{\text{NTSB}}$	Input	Standby	MCU GPIO or SPI Clock output	Standby input for device static mode control. CLK (Clock) during P_SPI operation

The use of the Inhibit pin (INH) is dependent on the selected target system operation. INH can turn an external power supply on and therefore wake a connected MCU for operation to save power when MCU operation is not required. In MPC5500 and MPC5600 automotive power train applications (engine control), INH is typically not used. However, in automotive body and chassis applications, it may be used.

9.4.2 High-speed CAN TJA1050 interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

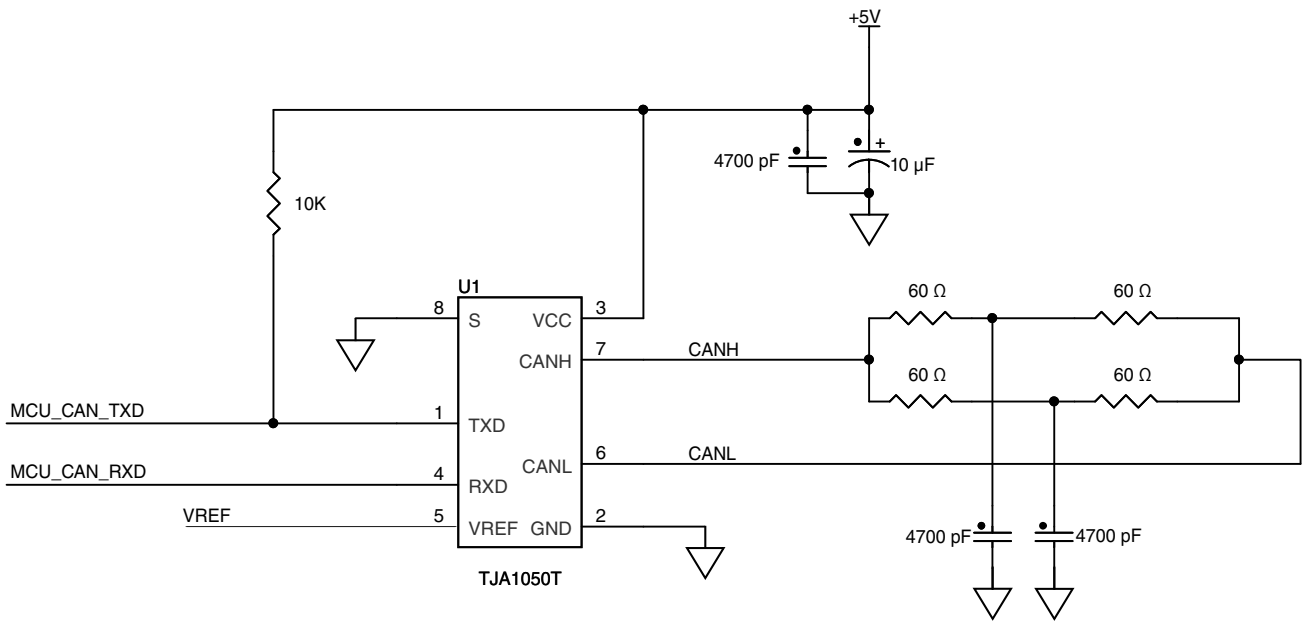


Figure 37. Typical high-speed CAN circuit using TJA1050

NOTE

- Decoupling shown as an example only.
- TXD/RXD pullup/pulldown may be required, depending on device implementation.

The table below describes the TJA1050 pin and system connections.

Table 42. TJA1050 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground return termination
3	VCC	Input	—	5 V	Voltage supply input (5 V)
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
5	VREF	Output	Reference voltage Output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
7	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
8	S	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in case of an error condition.

9.4.3 Low-speed CAN TJA1054 interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

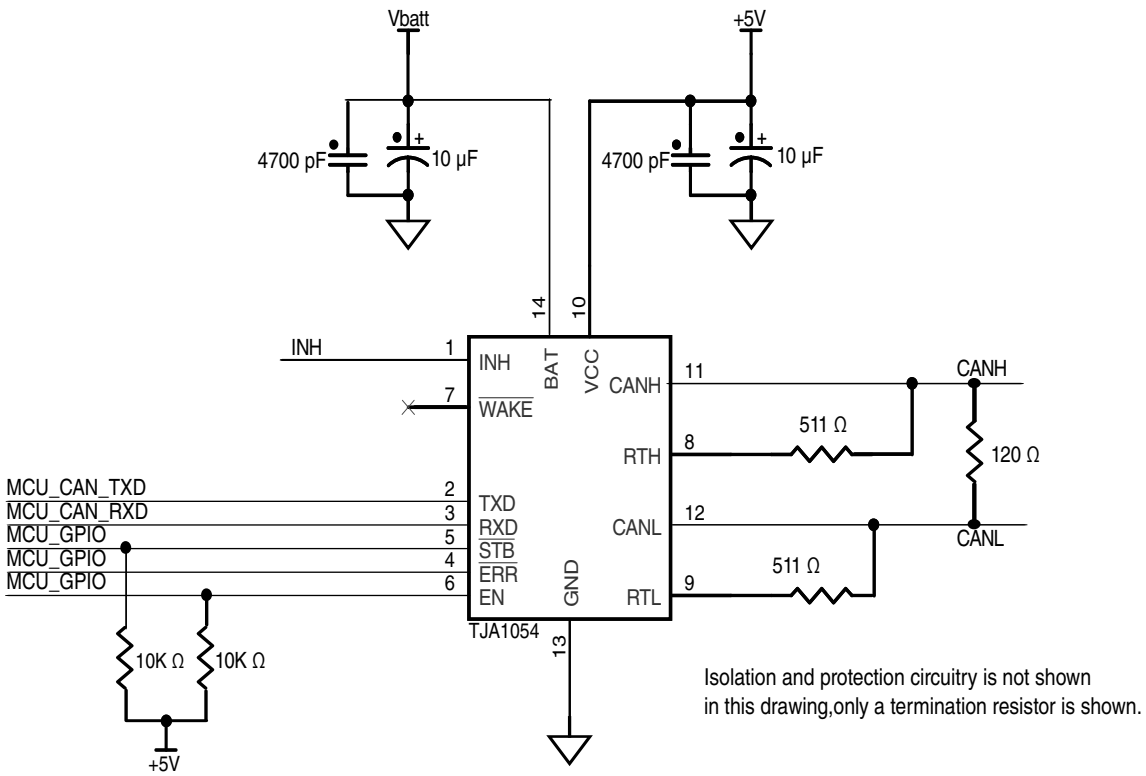


Figure 38. Typical low-speed CAN circuit using TJA1054

NOTE

- Decoupling shown as an example only.
- $\overline{\text{STB}}$ and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 43. TJA1054 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH	Input	Inhibit	Typically not connected	Inhibit output for control of an external power supply regulator if a wake up occurs
2	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU

Table continues on the next page...

Table 43. TJA1054 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
4	$\overline{\text{ERR}}$	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake-up is detected in Standby or Sleep modes.
5	$\overline{\text{STB}}$	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	$\overline{\text{WAKE}}$	Input	Wake	Typically not connected	Wake input (active low), both falling and rising edges are detected
8	RTH	Input	Termination Resistor High	Resistor to CANH	Termination resistor for the CAN bus high[1]
9	RTL	Input	Termination Resistor Low	Resistor to CANL	Termination resistor for the CAN bus low[1]
10	VCC	Input	Voltage Supply	5 V	Digital IO supply voltage, 5 V
11	CANH	Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V

1. This allows the transceiver to control the CAN bus impedance under an error condition.

9.4.4 Recommended CAN connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket is used on the evaluation board and a cable with a connector connects with it.

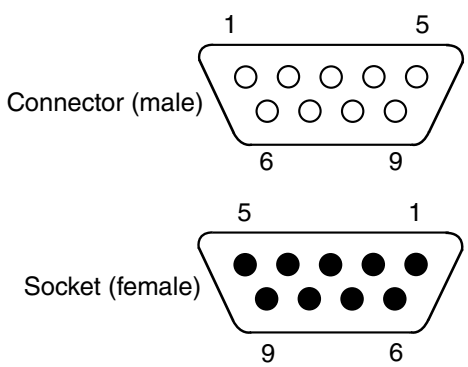


Figure 39. DB-9 connector and socket

The table below shows the typical connector pin-out definition.

Table 44. DB-9 pin signal mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHIELD (OPTIONAL)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (OPTIONAL)

NOTE

The metal shell of the socket should be connected through a ferrite bead to the chassis ground.

9.5 FlexRay interface circuitry using TJA1080A

FlexRay is an automotive fault-tolerant 2-wire communications interface. FlexRay is generally used at 10,000 Kbits/s (10 Mbit/s).

Freescale FlexRay devices implement a bus driver interface compliant with Communications System Electrical Physical Layer Specification, Version 2.1 Rev A.

Typically, FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s are supported and although the logic portions of the interface are implemented in the device, an external physical interface device is required to allow multiple FlexRay modules to be connected together.

The NXP™ (http://www.nxp.com) TJA1080A device is typically used as the FlexRay transceiver, although others are available. One transceiver is required for each FlexRay channel. The figure below shows the typical connections using the TJA1080A.

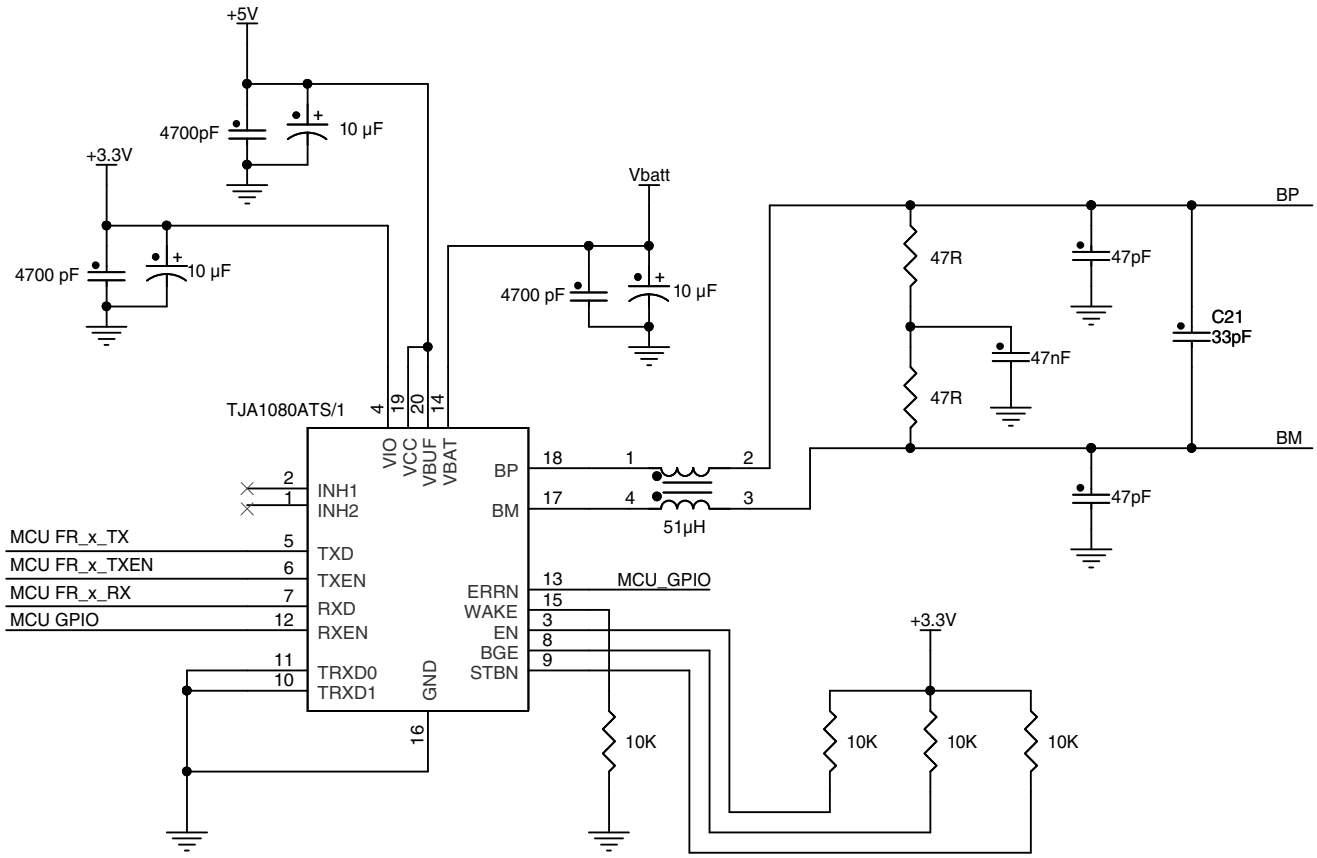


Figure 40. Typical FlexRay circuit

NOTE

- Decoupling shown as an example only
- TRXD0/TRXD1 is pulled to ground to enable the transceiver as a node device (not star configuration)
- In this configuration, only Normal mode is available. Further control is required to support Low-power mode.

MCU and system connections to the TJA1080A are shown in the following table.

Table 45. TJA1080 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH2	Output	Inhibit 2 Output	None	Inhibit output to enable/disable external power supply
2	INH1	Output	Inhibit 1 Output	None	Inhibit output to enable/disable external power supply
3	EN	Input	Enable Input	Pull up to 3.3 V or connect to a spare	Enable input (for mode selection (along with the

Table continues on the next page...

Table 45. TJA1080 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
				MCU GPIO (output to MCU)	STBN pin). Internal pull-down (transmitter disabled, but allows reception, listen only mode)
4	V_{IO}	Input (power)	IO Power Supply	3.3 V	Power supply input for the MCU I/O signals
5	TXD	Input	Transmit Data	MCU FR_x_TX[1]	Transmit data from the MCU for transmitting on the FlexRay bus. Internal pullup
6	TXEN	Input	Transmit Enable	MCU FR_x_TXEN[1]	Transmit enable. A high level disables the transmitter. Internal pullup
7	RXD	Output	Receive Data	MCU FR_x_RX[1]	Receive data from the FlexRay bus to the MCU
8	BGE	Input	Bus Guardian Enable	Pull up to 3.3 V	The bus guardian input disables the transmitter. This feature is currently not supported
9	STBN	Input	Standby Input	Pull up to 3.3 V or connect to a spare MCU GPIO	Standby mode enable input (low to enter low power mode). Internal pull-down
10	TRXD1	Input/Output	Data Bus Line 1	Tie low	Data bus signal 1 for an inner star connection
11	TRXD0	Input/Output	Data Bus Line 0	Tie low	Data bus signal 0 for an inner star connection
12	RXEN	Output	Receive Enable	MCU GPIO (input to MCU)	Receive data enable indicates data is available from the bus (low during activity)
13	ERRN	Output	Error Output	MCU GPIO (input to MCU)	The error diagnostic output drives low upon an error
14	V_{BAT}	Input (power)	Battery Supply Voltage	Protected battery voltage	Battery supply voltage

Table continues on the next page...

Table 45. TJA1080 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
15	WAKE	Input	Local Wake Up Input	Tie low or connect to switch or MCU GPIO	The local wakeup input forces
16	GND	Input	Ground	Ground	Ground, power supply return reference
17	BM	Input/Output	Bus Line Minus	To FlexRay Connector	FlexRay bus minus signal
18	BP	Input/Output	Bus Line Plus	To FlexRay Connector	FlexRay bus plus signal
19	V_{CC}	Input (power)	Supply Voltage	5 V	Supply voltage for internal logic
20	V_{BUF}	Input (power)	Buffer Supply Voltage	5 V	Supply voltage for the FlexRay bus minus/plus signals

1. x can be A or B depending on the channel requirements in the system.

To support the requirements of different worldwide OEMs, two connector types for FlexRay are used on evaluation boards:

- One socket DB-9 for both FlexRay channels
- Two Molex (Mini Fit Jr.™) headers, one for each FlexRay channel

However, there are various connectors used for production hardware. Figure 41 and Table 46 shows example pin-outs for both connector types. The DB-9 connector allows for two channels on a single connector. The dual channels allow for redundant wiring for increased reliability. The dual channel capability is built into the FlexRay standard.

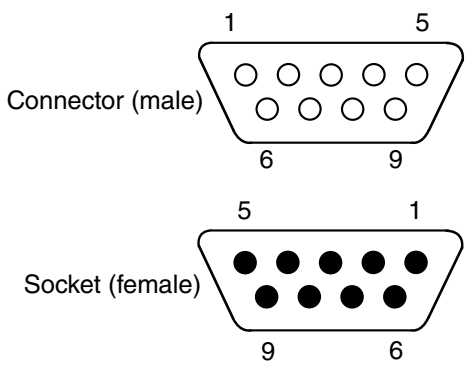


Figure 41. DB-9 connector and socket

Table 46. DB-9 pin-signal mapping

Pin Number	Signal Name	Full Name/Description
1	N/C	No connection
2	BM_A	Bus Minus Channel A
3	GND	No connection
4	BM_B	Bus Minus Channel B
5	SHIELD (OPTIONAL)	Optional Shield (if required)

Table continues on the next page...

Table 46. DB-9 pin-signal mapping (continued)

Pin Number	Signal Name	Full Name/Description
6	N/C	No connection
7	BP_A	Bus Plus Channel A
8	BP_B	Bus Plus Channel B
9	N/C	No connection

NOTE

- A socket is used on the evaluation board and a cable with a connector connects with this.
- The metal shell of the socket should be connected through a ferrite bead to GND.

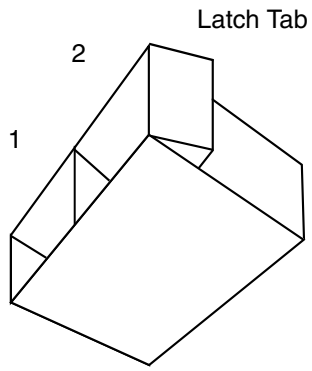


Figure 42. Molex connector picture

Table 47. Molex pin-signal mapping

Pin Number	Signal Name
1	BP
2	BM

NOTE

A connector is used on the evaluation board and a cable with a socket connects with this.

The Molex connectors are available in two types, one with pegs for mounting to the board and one without. The part numbers are shown in the following table.

Table 48. Recommended Molex Mini-Fit Jr. connector part numbers

Description	Manufacturer Part Number (Molex)
2-pin vertical connector with pegs for target system, tin contacts, latch	39-29-9022
2-pin vertical connector without pegs for target system, tin contacts, latch	39-28-8020
2-pin right-angle connector with pegs for target system, tin contacts, latch	39-30-0020

Table continues on the next page...

Table 48. Recommended Molex Mini-Fit Jr. connector part numbers (continued)

Description	Manufacturer Part Number (Molex)
2-pin right-angle connector with flange for target system, tin contacts, latch	39-29-1028
Mating connector with latch for cable assemblies	39-01-2020
Female terminal for mating cable assembly	39-00-0077

10 Pin Overview

Since there are many different requirements for the input and output signals of the MCUs, several types of pin types are used. The following table summarizes the types of pins/pads available on the MCUs. Information on the pad types and signal multiplexing is available in the device Reference Manual and the device Data Sheet. This section helps interpret this information.

NOTE

This document uses the terms pins, balls, and pads interchangeably when referencing the external signals of the device.

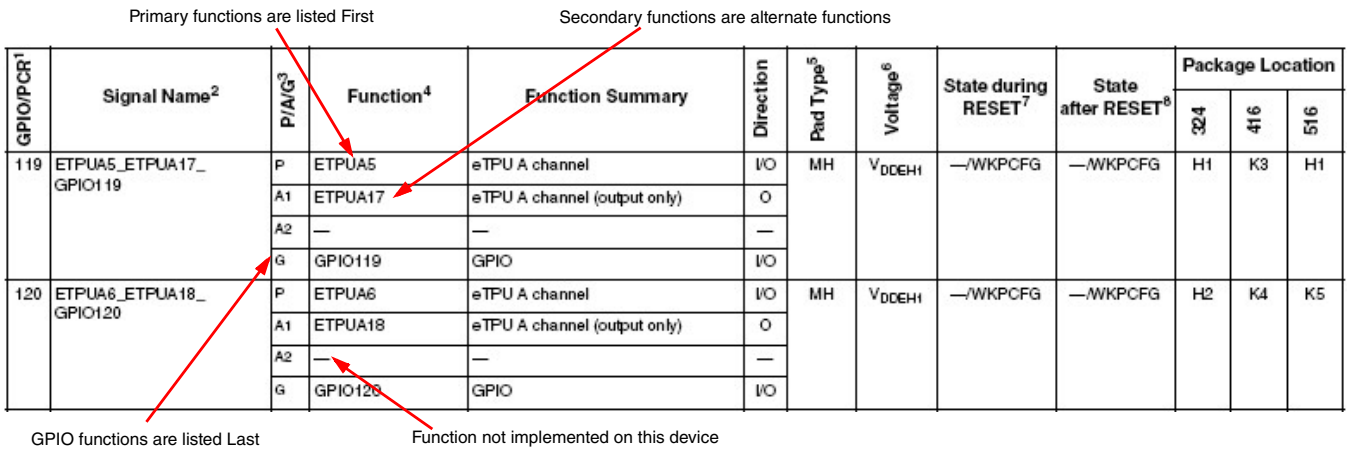
Table 49. Pad Types

Pad type	Abbreviation	Description
Medium Speed pads	MH or Medium	Most of the peripheral signals are medium (or medium if available depending on the device definition) speed pads, such as the eMIOS, and the eTPU. The Medium speed pads have slew rate control and may implement digital input circuitry, digital output circuitry or both. Medium pads can be powered by 3.3 V or 5.0 V.
Medium Speed pads with LVDS	MH+LVDS	MH+LVDS are Medium Speed pads that also support being used as part of a Low Voltage Differential Signalling pair.
Analog pads	AE or Analog	The Analog pads are low leakage and have no digital input or output circuitry. Some Analog pins (analog pads that support being used as a differential analog signal) also contain pull up and pull down resistors incorporated into the pad that can be independently selected.
Fast pads	F or Fast	The fast pads are digital pads that allow high speed signals. Generally, these are used for the external bus interface.
Fast pads with Slew Rate control	FS	Fast digital pins that also implement slew rate control. In general, these are used for the FlexRay signals.

Each of these pad types have programmable features that are controlled in a pin or pad configuration register (PCR). All pins, except single purpose pins without special properties that need to be controlled, on the device have a PCR. In a few cases, some signals are grouped together and a PCR controls multiple pins. The PCR is identified by the GPIO number. The PCR controls the pin function, direction, and other capabilities of the pin.

10.1 Understanding pin multiplexing

A majority of the Input/Output pins[9] on the MCU have multiple functions that are selectable by software[10]. The figure below shows a typical excerpt from the MPC567xF data sheet, but other devices have similar table, for the ball multiplexing of the different functions. This table shows the different functions that are available on each pin.



GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H1	K3	H1
		A1	ETPUA17	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO119	GPIO	I/O							
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H2	K4	K5
		A1	ETPUA18	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO120	GPIO	I/O							

Figure 43. Typical Device Pin Multiplexing

The first example shown above shows the ETPUA5_ETPUA17_GPIO pin. It can function as either enhanced Timing Processing Unit instantiation A (eTPU A) channel 5, eTPU A channel 17, or as a General Purpose Input/Output. In this particular case, the GPIO and the eTPU A Channel 5 can be used either as an input to the eTPU or GPIO, or can be used as an output. However, if the eTPU A Channel 17 function is selected, it can only be used as an output.

NOTE

In some cases, whether a channel can be an input or an output depends on the individual device definition. These should be checked carefully when designing a board. Although the internal signal to the eTPU A for channel 17 can either be input or an output, this particular pin can only support channel 17 being an output in this example. Other modules such as enhanced Modular Input/Output Subsystem (eMIOS) may also have this restriction. In particular, even though the eMIOS, channels are all orthogonal[11] on the MPC567xF and MPC5676R, the input of some channels can only come from the Deserial/Serial Peripheral Interface (DSPI) and cannot be defined to come directly from a pin. This functionality of each pin needs to be reviewed with the particular device Reference Manual and Data Sheet.

Other information is shown in the above table extract is important when designing a board. These other fields are:

9. Ball grid array (BGA) packages have balls instead of pins. Pins are used on packages that have pins for signals. Pads refers to the bonding pad on the physical die that is contained inside the package. These terms are typically used interchangeably. The actual correct term depends on the package type.
10. In some cases, hardware overrides the software settings. Consult the device reference manual and data sheet.
11. On some devices, the eMIOS channels are orthogonal, that is every channel has the same functional capabilities. This is not true on all devices. Some devices (such as the MPC5634M) only support a subset of the eMIOS functions are supported on some channels.

- **Pad Type**: This column of the table contains the pad type of the ball/pin. This is required to understand the characteristics of the pin/ball.
- **Voltage**: The voltage column of the table lists the power supply that powers the pin. All of the pins are broken up into separate power segments such that the input and output voltages for the pins match the voltage of the circuits connected to the pins. On some devices that support more than one DSPI module, one of the DSPI can be set to operate at a different voltage level than the others. This allows one DSPI to handle 5 V peripheral devices and another DPSI to have 3.3 V peripheral devices.
- **State During Reset and State After Reset**: The columns for the state of the pin during and after reset could be important in the design of the system. The user needs to ensure that these states do not cause any issues with external circuitry, such as turning on a motor during reset.
- **Package Location:** These columns show the ball map location of the signal for each of the package types..

10.2 Injection Current

All pins implement protection diodes that protect against electrostatic discharge (ESD). In many cases, both digital and analog pins need to be connected to voltages that are higher than the operating voltage of the device pin. In addition to providing protection from ESD, these diode structures will also clamp the voltage to a diode drop above the supply of that pin segment. This is permissible, as long as the current injection is limited as defined in the device specification. Current can be limited by adding a series resistor on the signal. The input protection diodes will keep the voltage at the pin to a safe level (per the absolute maximum ratings of the device) as long as it is less than the maximum injection current specification.

Additional circuits on the pins can be enabled only by fast ESD transients. In normal operation, these circuits have no effect on the pin characteristics and are triggered by fast high voltage transients. To prevent turning on these circuits during normal power-up sequences, the ramp rate of the power supplies (all external supplies, 5V, and if the internal regulators are not used, 3.3V and 1.2V) should not exceed 25 V/ms.

Below is an extract from the MPC5674F Data Sheet revision 9 dated November 2011 and the MPC5676R Data sheet revision 3 dated September 2012. These specifications may change. Consult the latest revision of the data sheet to determine if there have been updates to these specifications.

Table 50. Injection currents allowed

Data Sheet Table	Pin type	Maximum inject current allowed
DC Electrical Specifications	DC Injection Current (per pin)	DC ±1 mA
Absolute Maximum Ratings	Maximum Digital Input Current, (per pin, applies to all digital pins)[1]	±3mA[2]
Absolute Maximum Ratings	Maximum Analog Input Current (per pin, applies to all analog pins)[3]	±3mA[2]

1. Total injection current for all pins must not exceed 25mA at maximum operating voltage.
2. Injection current of ±5mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25V maximum analog or V_{DDEH} supply when under this stress condition. Transitions within the absolute Maximum input current specification do not affect device reliability or cause permanent damage. Inputs must be current limited to the values shown.
3. Total injection current for all analog input pins must not exceed 15mA.

The figure below shows a typical digital pin and the protection diodes. Controls for all of the pad options are controlled in the Pad/Pin Configuration Register for the pin.

NOTE

The below diagram represents the production mask set versions of the MPC564xF and the MPC5676R. The pre-driver circuit was previously powered by VDD33 on some earlier mask sets (MPC567xF: fixed on 3M17W and later, MPC5676R: fixed on 2N23A, production mask set is 3N23A or later). The earlier versions had limitations on the differential voltage between the VDD33 internal power supply and the external 3.3V

VDDEx or VDDEHx power supplies when the VDDEx/VDDEHx power supplies are powered from an external supply. See the mask set errata.

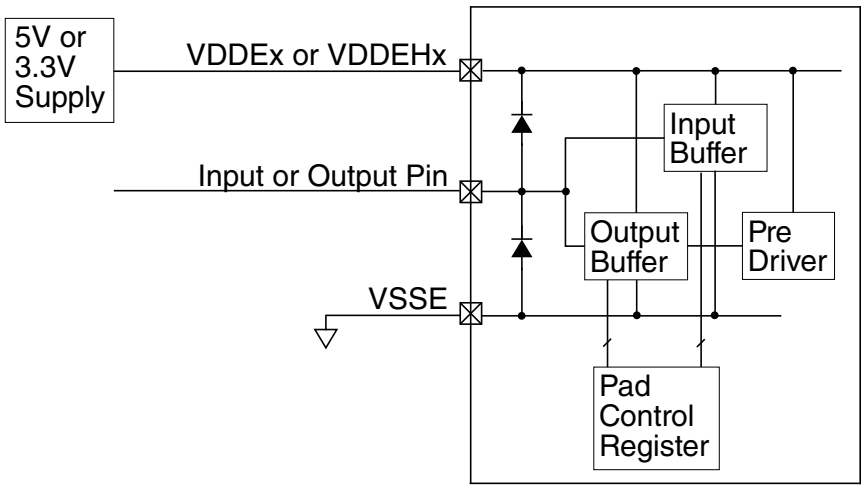


Figure 44. Typical input protection

The value of a series resistor to limit the injected current can be calculated simply. For a 1mA injection current limit, a 20KΩ resistor provides protection for a 20V DC injection current:

DC_{max} = 20kΩ/1mA = 20V

This voltage is sufficient for signals that are connected to a typical 12V battery.

In addition to the DC current, typically the data sheet includes a maximum accumulation specification for short periods of time over this DC level, such as 5mA for up to 60 hours over the entire life of the device.

$AC_{max\_current}$ = 20kΩ/5mA = 100V

If there are 5mS excursion events over the 1mA injection current limit of up to 5mA, then a total of 43.2K events can occur over the lifetime of the device.

$AC_{max\_duration}$ = 60 hours/5 ms per event = (60 hours x 60 minutes/hour x 60 seconds/minute) / 5ms = 43,200,000 events

10.3 Special Pins

There are a few pins on the device that should always be treated in the same manner. There are no options for how these pins are connected in a system.

- TEST - The Test pin should always be connected directly to ground.
- VSSFL - The VSSFL is a special ground signal for the flash. It must be tied directly to ground.

10.4 Handling unused pins

In some applications, not all pins of the device may be needed. Good CMOS handling practices state that all unused pins should be tied off and not left floating. On the MCU, unused digital pins can be left open in the target system. Almost all pins have internal pull devices (either pull-up or pull-down devices[12]). For unused digital pins, it is recommended that software disable both the input buffers and the output buffers of the pads in the Pad Control Register for the pins. In addition, the weak pull-down device should be enabled. This keeps the pad in a safe state under all conditions.

12. Technically, these devices are not resistors. They are active weak transistors that pull the input either up or down.

For analog pins, it is recommended that they be pulled down to VSSA (the analog return path to the MCU).

Appendix A Summary of recommended power supply bypass capacitors

The table below shows the recommended number and values of bypass capacitors for each of the digital power supply pins.

Table A-1. Recommended digital power supply bypass capacitors

Supply	Quantity	Value	Notes
VDDREG	1	4.7 µF	These capacitors should be placed near the collector of the external pass transistor and to the VDDREG pin.
	1	100 nF	
VDD	6	2.2 µF	Locate at the 4 corners and on 2 sides.
	7	10 nF[1]	
VDDSYN (3.3 V output)	1	10 µF / 16 V	VDDSYN should be shorted directly to VDD33 with a minimum of impedance.
VDD33 (3.3 V input)	1	100 nF[1]	
VDDE2	1	10 nF	Nexus/JTAG pin supply.
VDDE8 VDDE9 VDDE10	4	10 nF	External bus - 516 package only.
VDDEH1 VDDEH3 VDDEH4 VDDEH5 VDDEH6 VDDEH7	5	10 nF	Place near any five of the six supplies.
VSTBY	1	10 nF	

1. Low ESR capacitors should be used.

The table below shows the recommended bypass capacitors for the analog power supplies of the device.

Table A-2. Recommended analog power supply bypass capacitors

Supply	Quantity	Value	Notes
VDDA_A0	1	10 µF	For optimum analog performance, the VDDA supplies should be isolated/ filtered from the digital 5 V supplies. However, if analog injection current is allowed, no isolation should be used to prevent VDDA from rising due to injection current.
VDDA_A1 VDDA_B0 VDDA_B1	1	100 nF	
VRH_A VRH_B	1	10 nF	Connect to VRL. VRH and VRL should be isolated from VDDA and system ground.

Table continues on the next page...

Table A-2. Recommended analog power supply bypass capacitors (continued)

Supply	Quantity	Value	Notes
REFBYPCA	1	10 nF	Connect capacitor between each pin and VRL.
REFBYPCA1	1	10 nF	
REFBYPCB	1	10 nF	
REFBYPCAB1	1	10 nF	

Appendix B MPC567xF and MPC5676R ADC Input Model

In some cases, the internal topology of the eQADC model is required for some calculations, including sizing of the external capacitors, external resistors, and for setting the minimum sample time of the ADC. The figures below show a representative model of the eQADC inputs including the input multiplexers, internal node capacitances, and the actual sample capacitor of the ADC itself. The analog inputs that are accessible from both eQADC modules are also shown. For readability, the two eQADC modules (A and B) are shown separately.

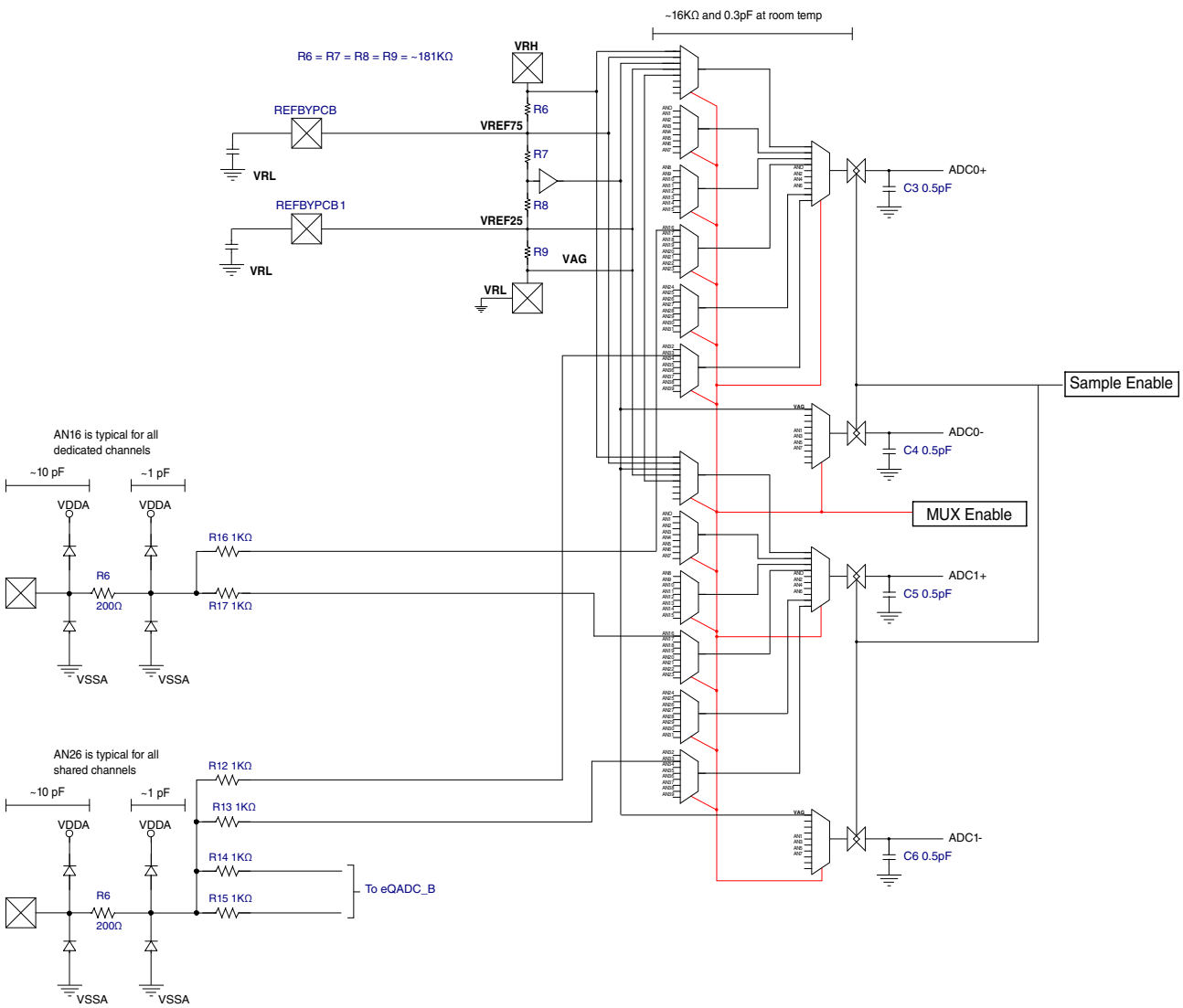


Figure B-1. MPC567xF and MPC5676R eQADC_A Input Model

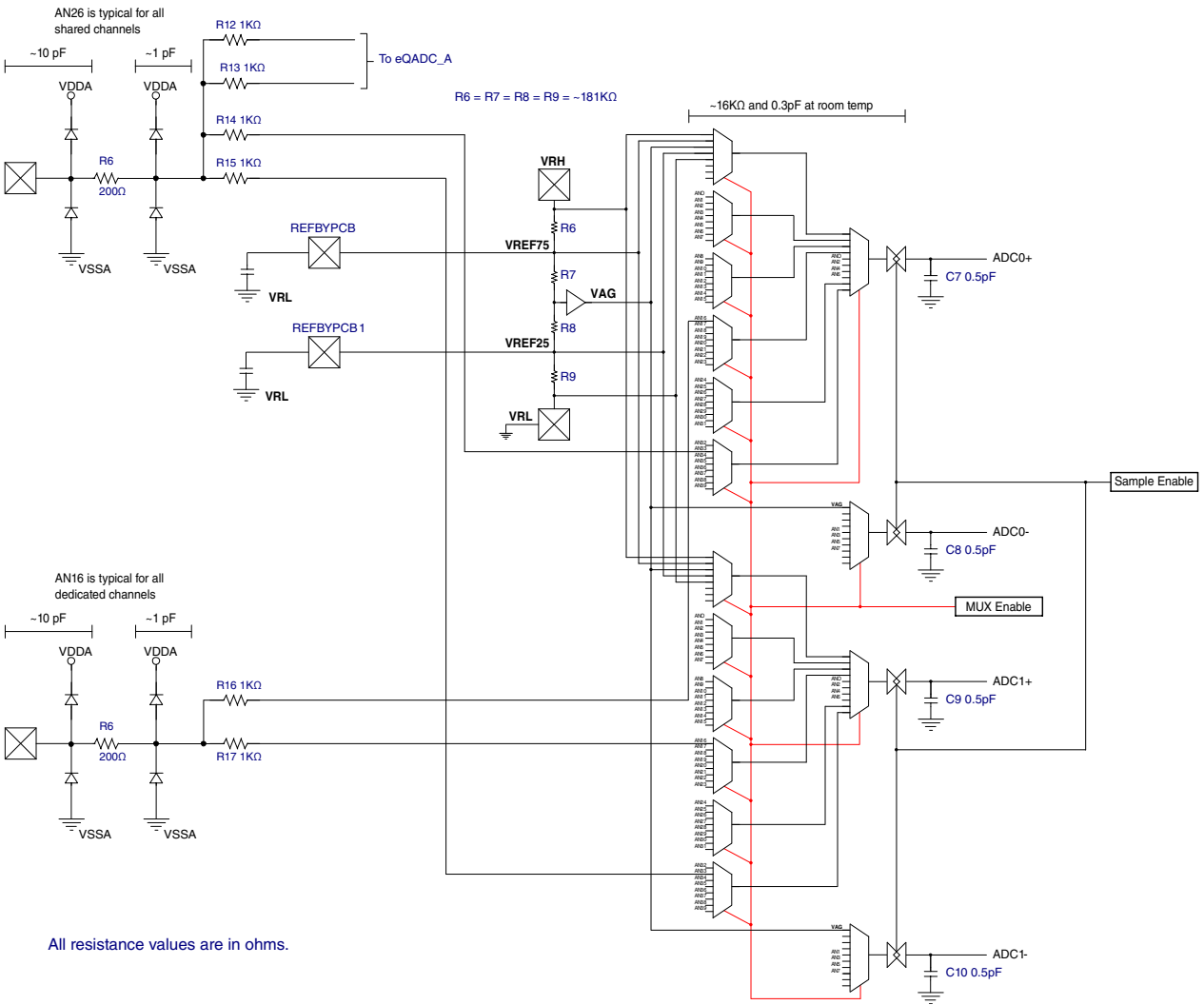


Figure B-2. MPC567xF and MPC5676R eQADC_B Input Model

Appendix C References

More information can be found in the documents listed in the table below. All of these documents are available on the Freescale web site (http://www.freescale.com).

Table C-1. References

Document	Title
MPC5674FRM	MPC5674F Microcontroller Reference Manual
MPC5676RRM	MPC5676R Microcontroller Reference Manual
MPC5674F	MPC5674F Data Sheet
MPC5676R	MPC5676R Data Sheet
e200z760RM	e200z760n3 Power Architecture Core Reference Manual
AN3968	Nexus Interface Connector for the MPC5674F/MPC5676R
AN2989	Design, Accuracy, and Calibration of Analog to Digital Converters on the MPC5500 Family
AN4731	Understanding Injection Current on Freescale Automotive Microcontrollers

Appendix D Revision History

Table D-1. Revision History

Revision	Release Date	Changes
0	13 August 2012	Initial customer release.
1	01 December 2014	Removed VDDREG connection to ground option. This option is not supported.
		Added External Supplies option with internal 3.3V also used. This is the preferred configuration even when using an external 3.3V supply.
		Added TCK isolation resistor option in the "Minimum debug external circuitry" section.
		Added comments that the eSCI module is used for LIN and UART functions.
		Added reference to AN4731 "Understanding Injection Current on Freescale Automotive Microcontrollers" to references.
2	06 January 2015	Added statements that VDDREG, VDDSYN, and VDD33 must be sorted together in multiple sections of the application note (Internal linear 3.3 V regulator, Using internal and external supplies, and Using external supplies)
		Minor clarifications in the Introduction about powering the ADC (5 V required) and that if pin segments are powered by 3.3 V, an external 3.3 V supply is required.
		Updated references in Injection Current to the latest versions of the device data sheets. Added table references column to table. Removed Disruptive Input Current for Analog pins from "Injection currents allowed" table.

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