



System Integration Unit Lite Pin Multiplexing

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1 Scope

This document explains the pin-multiplexed connections and portions of the programming model for the external pins that are controlled by the System Integration Unit Lite (SIUL).

2 Reference material

Current revision of Freescale document MPC560XPRM, *Qorivva MPC5604P Microcontroller Reference Manual*.

This application note refers specifically to the Qorivva MPC5604P device, but it is used only as an example — the information given here applies to the SIUL in all Freescale MPC56xx devices.

3 General

In this document and throughout the reference manual, the terms pins, pads, and ports are used interchangeably.

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The external package pins are attached to die pads. These pads are controlled by the Pad Configuration register (PCR).

4 Port control

Each pin is connected to port control logic. The Pad Configuration register controls the output pin multiplexer (output MULTIPLEX), the input and output enables, output configuration, slew rate control, pull up/down, and mode control.

For an output the user needs to select the module output driving the pad output buffer, which then drives the pin. For an input the user must select the pad input buffer, driving the module input. The multiplexing is always associated to the destination of the signal.

4.1 Pad Configuration register

Each pad is controlled by an associated Pad Configuration register. It configures the characteristics of the pin. Whether its an input, output, pull up or pull down, etc. There are nine characteristics controlled by each register. The figure below is taken from the reference manual.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
R		SMC	APC		PA[1:0]		OBE	IBE			ODE				SRC	WPE	WPS
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 1. Pad Configuration register (PCR)

This document will focus on the PA and IBE/OBE bits.

4.2 PA (Pad Output Assignment) bits

The PA bits select the signal assignment for the pin. Each pin has various possible alternate functions (ALTx). Each ALTx is determined by the PA bits: 00 is for ALT 0, 01 for ALT 1, 10 for ALT 2, and 11 for ALT 3.

4.3 IBE/OBE (Input Buffer Enable/Output Buffer Enable) bits

These bits control whether the signal is passed to the pin as an output or routed back in as an input, or both. In this case, the input can be used to monitor the output, or the input can be used to trigger an interrupt, etc.

4.4 Output

Each and every signal pin is capable of multiple signals. These signals are selected via an output multiplexer that is controlled by the PA bits of the PCR.

4.5 Input

Where the table indicates the signal is an I/O or I, these signals are routed to the functions as inputs. In most cases, when the IBE is set, the signal will be routed to the input of a particular module. However, if the module's input can be routed from two different pins, then the Pad Selection for Multiplexed Inputs register (PSMI) is used to select the pin routing for this pad.

4.6 Pad Selection for Multiplexed Inputs (PSMI) register

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PADSELO				0	0	0	0	PADSEL1			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	PADSEL2				0	0	0	0	PADSEL3			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 2. Pad Selection for Multiplexed Inputs register (PSMI0_3)

This register selects which pins are routed to specific input functions. Each multiplexed input has four bits in this set of registers. The user must program the bits based on which input will go to the module selected.

5 Real life example

Each pin has the ability to be selected to multiple module signal outputs. Some pins have the inputs routed to multiple module inputs. For instance, Port A[0] has a selection of three distinct input/outputs and one distinct input. Information in Table 1 is adapted from the MPC5604P reference manual.

These ports have been chosen to demonstrate the pin multiplexing, and to show that they share the clock line (SCK) for DSPI2 module. The DSPI clock can be an input or an output depending on whether the DSPI is setup as a master (output) or slave (input).

Since the DSPI clock is an I/O and is available on two separate pins, then the input pin multiplexing needs to be selected.

Table 1. Pin multiplexing

Pin port	PCR register	Alternate function	Functions	Peripheral	I/O Direction
A[0]	PCR[0]	ALT 0	GPIO[0]	SIU Lite	I/O
		ALT 1	ECT[0]	eTimer	I/O
		ALT 2	SCK	DSPI2	I/O
		ALT 3	F[0]	FCU0	O

Table 1. Pin multiplexing (continued)

Pin port	PCR register	Alternate function	Functions	Peripheral	I/O Direction
		—	EIRQ[0]	SIU Lite	I
A[11]	PCR[11]	ALT 0	GPIO[11]	SIU Lite	I/O
		ALT 1	SCK	DSPI2	I/O
		ALT 2	A[0]	FlexPWM0	O
		ALT 3	A[2]	FlexPWM0	O
		—	EIRQ[10]	DSPI2	I/O

5.1 Internal connection

The diagram below is a simplified diagram showing pin port A[0], based on the function chart above.

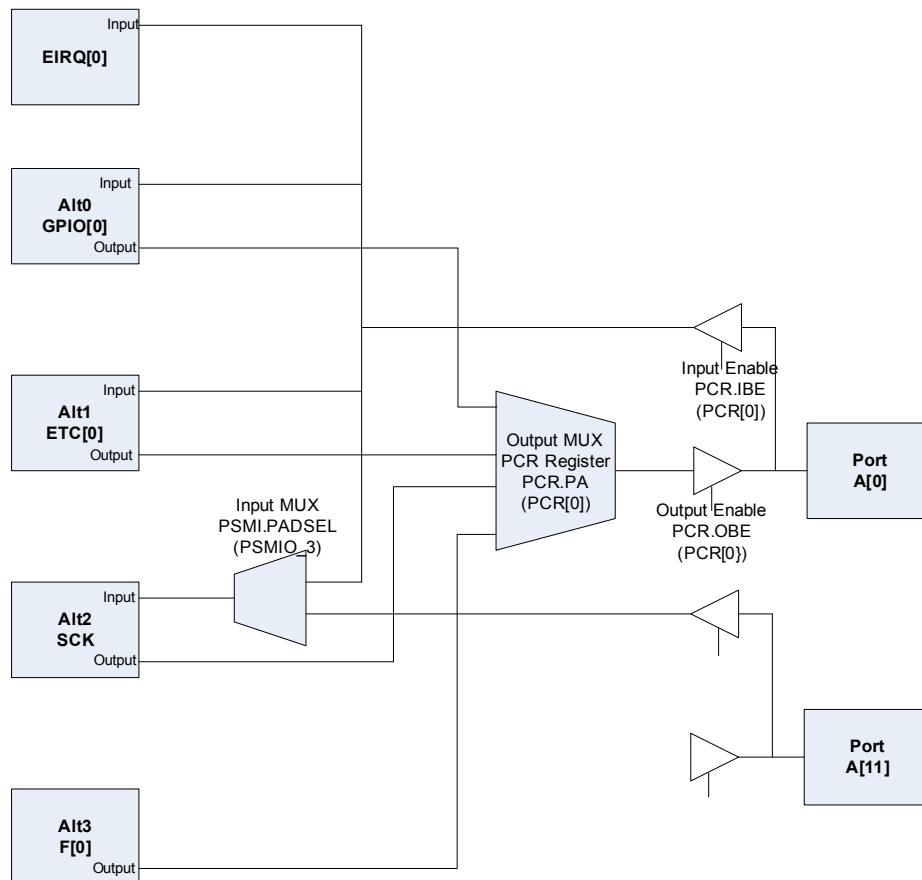


Figure 3. Block diagram of chip interconnects

To select a particular output function to this port/pin, the user would write to the Pad Configuration Register (PCR) and also enable the output using the PCR[OBE] (Pad Configuration Register[Output Bit Enable]). With this combination of data in the PCR, the function is set to this pin and the output is enabled.

For the input selection, there is an equivalent multiplex register, the Pad Selection for Multiplexed Inputs (PSMI). Writing this register configures the multiplexing from the pin to the appropriate functional block. The PCR[IBE] bit (PCR [Input Bit Enable]) must also be written to enable the input.

5.1.1 Input enable

In this case, once the input is enabled, the signal is routed to three inputs: EIRQ[0], GPIO, and the ETC[0]. For each of these modules, the signal can be used or ignored, based on the programming of the modules that have this input routed to it. If the input signal is capable of being routed to two pins, then the PADSEL bits in the appropriate PSMI register also need to be programmed. Please note that once the input is enabled, it is enabled for this entire port.

To determine if the PSMI register is required, you must read the pin multiplexing table for identical signal and peripheral names. In this case it is the DSPI2 clock (SCK).

NOTE

The PSMI register needs to be programmed only if an input signal can be assigned to multiple pins.

5.1.2 Software example

5.1.2.1 Simple GPIO Routing

Assume that the system requires port A[0] to be a simple output. This will require the PCR[PA] value to be programmed to 00, and the OBE to be set to one. So, for this nibble, the value would be 0010b. If the signal is needed to generate an interrupt, then the input would need to be enabled by setting the IBE to one. So now the nibble value will be 0011. At this point the input buffer is enabled and the signal will go to all the modules shown.

5.1.2.2 DSPI2 master mode

If the DSPI module is needed to act as the (clock) master, then the pin multiplexing must be set to ALT2, and the output buffer enabled. The nibble value must be 1010b. If you want to monitor the SCK signal via the GPIO module, then you must also enable the input buffer by setting the IBE to one, changing the nibble to 1011b.

5.1.2.3 DSPI2 slave mode

Now assume that the DSPI is set up in slave mode. This requires the clock to be sourced external to the chip — the pin now becomes an input. Another requirement is to use the Port A[0] as the input pin.

Since the DSPI2 SCK signal can come from two different pins, the PSMI selection is required. This results in a PSMI0_3[PADSEL1] nibble to be set to 0001. This selects the input multiplexing.

The value for PCR[PA] is a don't care. However, you must set the OBE to 0 and the IBE to 1. Care must be taken to not set the OBE when the signals will be generated from outside the chip, which can result in possible hardware damage.

6 Revision history

Table 2. Changes made April 2012¹

Section	Description
Front page	Add SafeAssure branding.
2	Add Qorivva branding.
Back page	Apply new back page format.

¹ No substantive changes were made to the content of this document; therefore the revision number was not incremented.

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Document Number: AN4035

Rev. 0

04/2011

