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Designing the V_{CORE} Compensation Network

For The MC33907/MC33908 System Basis Chips

1 Introduction

This application note explains how to design an effective compensation network for the V_{CORE} error amplifier of the MC33907 and MC33908. The V_{CORE} Regulator integrated inside these System Basis Chips is a non-synchronous voltage mode buck regulator. It generates the microcontroller core supply voltage. This voltage is adjusted using an external voltage divider in the range of 0.9V to 5V.

As with any switch-mode DC/DC converter, the V_{CORE} Regulator needs a compensation network for stabilizing the converter. It is necessary for compensating the gain and phase shift caused by the output filter of the buck regulator. Only with proper compensation can the buck converter react fast enough to load steps without falling into an unstable mode.

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2 Closed Loop System

Every buck converter has three main blocks: the modulator stage, the output filter and the compensation network (**Figure 1**).

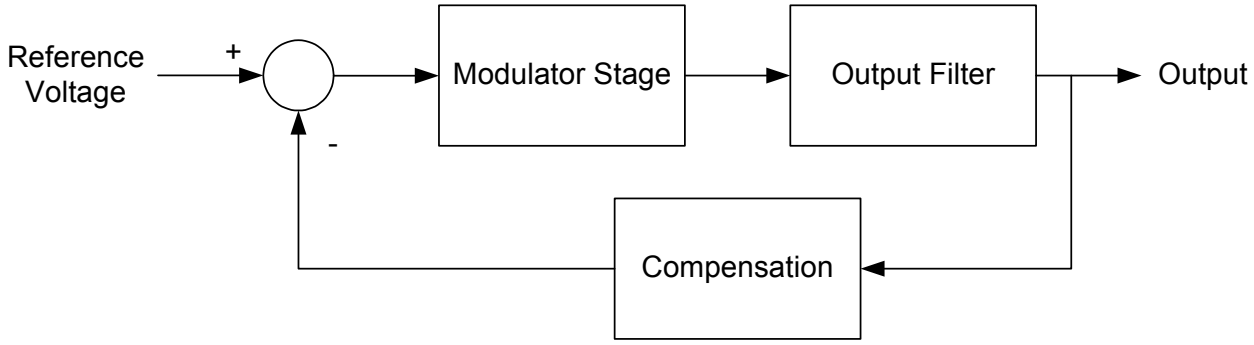

Figure 1. Buck Converter Functional Blocks

For the complete system the closed loop is expressed by

$$Gain_{loop}(s) = Gain_{Modulatorstage} \cdot Gain_{Filter}(s) \cdot Gain_{EA}(s)$$

Each of these stages has a specific transfer function. The characteristics of each block are shown in the next chapters.

3 Modulator Stage

The modulator stage is the part which modulates the pulse width of the switch mode converter. It compares the output signal of the error amplifier with the sawtooth voltage of the oscillator and adjusts the pulse width (**Figure 2**).

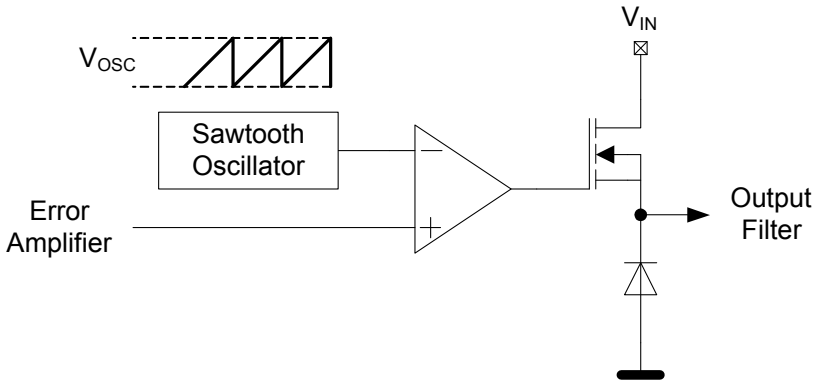

Figure 2. Pulse Width Modulation Stage

The gain of the modulator stage is defined by the quotient of input voltage V_{IN} and the oscillator peak-to-peak voltage V_{OSC}.

$$Gain_{Modulatorstage} = \frac{V_{IN}}{V_{OSC}}$$

In case of the MC33907 and MC33908 the input voltage for the core regulator is the output voltage of the pre-regulator, typically 6.5 V. The peak-to-peak oscillator voltage V_{OSC} is 1.45 for the devices. So the gain of the modulator stage is 4.48, or 13 dB respectively.

4 Output Filter

The output filter comprises the output inductor (L_{OUT}), its DC resistance (DCR), the output capacitor (C_{OUT}) and the equivalent series resistance of the output capacitor (ESR).

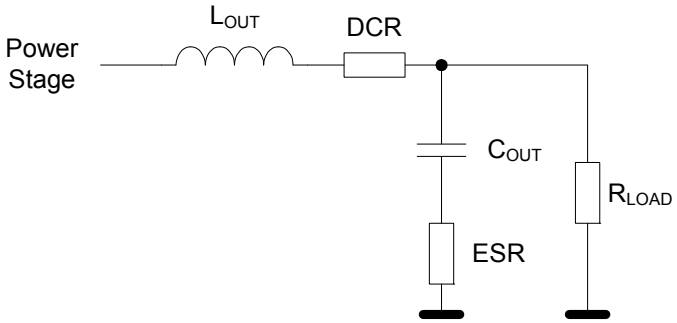

Figure 3. Output Filter

The transfer function for this stage is as follows:

$$Gain_{Filter}(s) = \frac{\frac{1}{sC_{OUT}} + ESR}{sL_{OUT} + DCR + \left[R_{LOAD} \parallel \left(\frac{1}{sC_{OUT}} + ESR\right)\right]}$$

With the assumption DCR = ESR ≈ 0, the equation can be simplified

$$Gain_{Filter}(s) = \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

with

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

$$\omega_0 = \frac{1}{\sqrt{LC_{OUT}}}$$

$$Q = R_{LOAD}\sqrt{\frac{C_{OUT}}{L}}$$

From these equations, it is obvious that the gain and the phase shift of the output filter are affected by a zero caused by the ESR and a double pole created by L_{OUT} and C_{OUT}.

Let's remember, a pole changes the slope of the gain by -20 dB/decade and the phase changes from 0 to -90° over the range from one decade below to one decade above the pole frequency. For the double-pole created by L_{OUT} and C_{OUT}, gain is therefore -40 dB/decade and phase is decreased by 180° with a very sharp roll off. For a zero the gain changes with +20 dB/decade and the phase changes from 0 to +90°, from one decade below to one decade above the zero frequency.

The graph below shows a Bode plot (gain and phase) for an output filter with low ESR ceramic capacitors. In this example the components have following values: L = 2.2 µH, C = 20 µF and ESR = 10 mΩ. This filter has a double pole ω_0 around 24 kHz and the zero ω_Z is around 795 kHz.

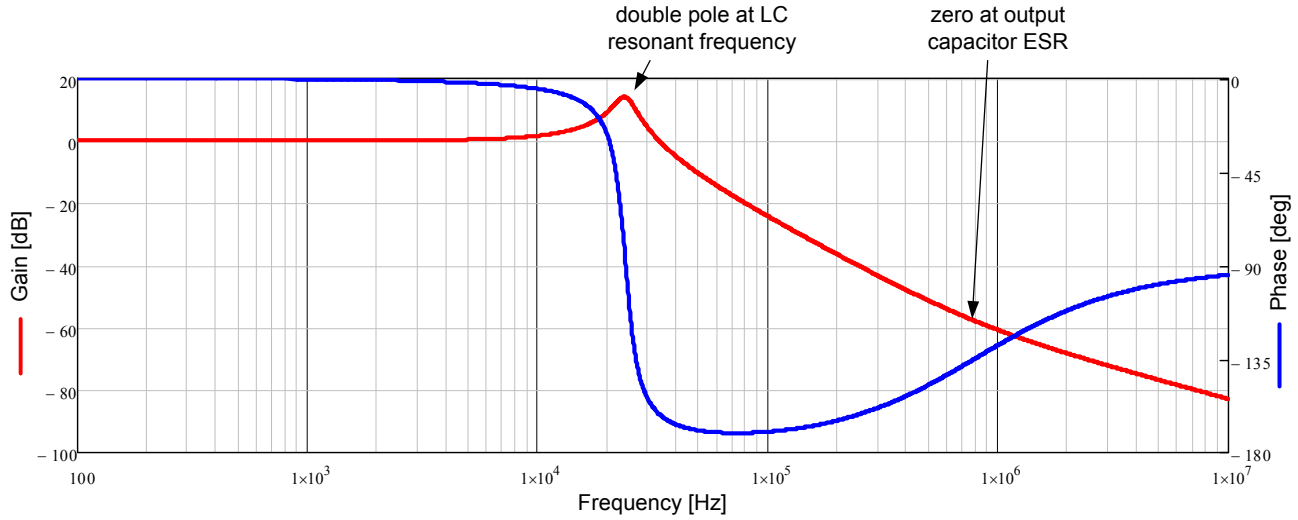

Figure 4. Frequency Response for Output Filter with Low ESR Capacitors

5 The Compensated System

To have a stable closed loop, the frequency response of the output filter and the gain of the modulator stage have to be compensated. Otherwise a load change could cause instabilities of the system. Compensation is done with the compensation network, which is connected to the error amplifier. A compensated system fulfills the following criteria:

- The gain crosses 0 dB at the desired bandwidth (f_C = crossover frequency)
- The gain rolls off with -20 dB/decade at the crossover frequency
- The phase margin is more than 45° below the crossover frequency

One common question is how to choose the right crossover frequency f_C. For a voltage mode buck converter, f_C should be at least three times above the double-pole frequency. On the other hand, the crossover frequency has to be less than half of the switching frequency (f_{SW}). With a higher crossover frequency, one can reach a faster load transient response, but circuits with high f_C are prone to pick up noise.

6 The Compensation Network

A compensation network is necessary to meet the above-mentioned criteria for the stability of the closed loop system. There are different compensation networks which set gain and phase differently. The voltage mode buck converter with the double pole needs a compensation network that creates a large phase boost. Such an amplifier circuit is the so called “type 3 amplifier compensation”. It gives a very good transient response to the circuit.

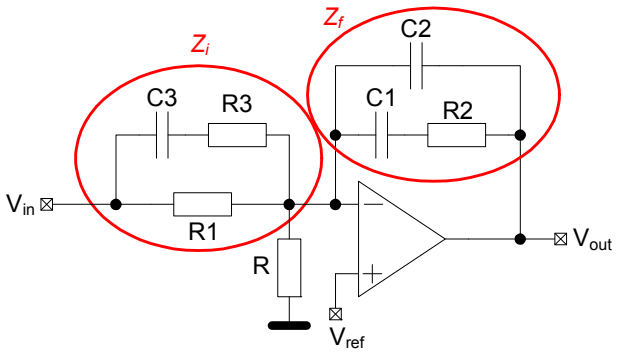

Figure 5. Compensation Network

The transfer function of the type 3 amplifier block is

$$Gain_{EA}(s) = \frac{Z_f}{Z_i} = \frac{\frac{1}{sC_2} \parallel \left(R_2 + \frac{1}{sC_1}\right)}{R_1 \parallel \left(R_3 + \frac{1}{sC_3}\right)}$$

Based on the transfer function, the poles and zeros of this circuit are:

$$\omega_{zero1} = \frac{1}{R_2 C_1}$$

$$\omega_{zero2} = \frac{1}{(R_1 + R_3)C_3}$$

$$\omega_{pole1} = \frac{C_1 + C_2}{R_2 C_1 C_2}$$

$$\omega_{pole2} = \frac{1}{R_3 C_3}$$

Figure 6 shows the gain and phase of an ideal type 3 amplifier, **Figure 7** provides a more realistic simulation result.

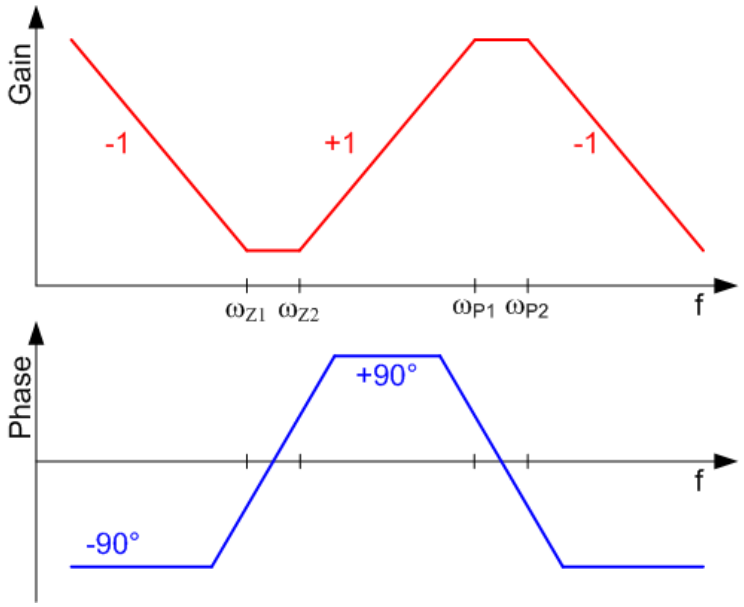

Figure 6. Frequency Response and Phase Margin for Ideal Type 3 Amplifier

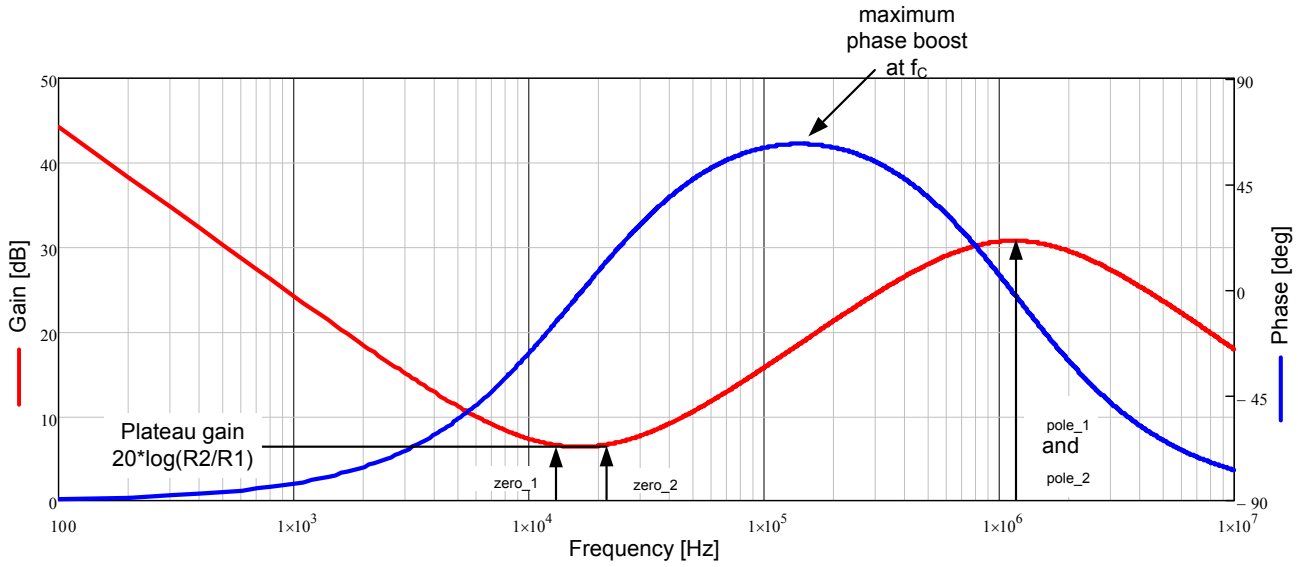

Figure 7. Type 3 Amplifier Simulated Frequency Response and Phase Margin

7 Calculation of the Compensation Network

As already mentioned, the LC filter with low ESR ceramic capacitors creates a phase shift close to -180°. On the contrary, the phase margin has to be at least 45° below the crossover frequency. This means the phase shift must not be below -135°. The type 3 amplifier gives the necessary phase boost.

The following example calculation is based on the filter parameter as used in the example above: L = 2.2 µH, C = 20 µF and ESR = 10 mΩ. The desired output voltage is 3.3 V.

At first, select a crossover frequency, for example f_C = 150 kHz. This is around six times the resonant frequency of the LC filter and below half of the switching frequency. The input voltage divider built using R_1 and R defines the output voltage of the V_{CORE} regulator. Therefore we already know R_1, which in our example is 24.9 kΩ.

In the next step, R_2 is calculated. The ratio R_2/R_1 defines the plateau gain and, therefore, the crossover frequency. At the crossover frequency f_C, the gain of the closed loop $G_{loop}(s)$ is 0 dB. “Plateau gain” is the gain of the compensation circuit at the second zero ω_{zero_2}. We will place this zero at the resonant frequency of the LC filter. As is already known, upwards from this zero, the gain is +20 dB / decade. From the Bode plot of the LC filter, one can read -31.5 dB at the crossover frequency. The required plateau gain (see also **Figure 7**) can now be calculated using

$$Gain_{plateau}(f_{zero2}) = Gain_{Filter}(f_C) + Gain_{Modulatorstage} + Gain_{slopez2}$$

with

$$Gain_{slopez2} = \frac{f_c}{f_{zero2}}$$

In our example,

$$Gain_{plateau}(f_{zero2}) = -31.5dB + 13dB + 20\log\left(\frac{f_c}{f_{zero2}}\right) = 2.5dB$$

This can be simplified to

$$R_2 = \frac{f_c}{f_{LC}} \cdot \frac{V_{OSC}}{V_{IN}} \cdot R_1$$

We get R_2 = 34.7 kΩ. The first zero of the compensation network ω_{zero_1} should be placed at half of the LC filter pole frequency (½ * ω_0). With this, C_1 can be calculated.

$$C_1 = \frac{2}{R_2\omega_0}$$

$$C_1 = 382pF$$

Next, the first pole ω_{pole_1} of the compensation network is calculated. Because the ESR zero, ω_Z, is far above the crossover frequency and does not play a role in the overall compensation, we can place this pole at half of the switching frequency of the V_{CORE} regulator.

$$C_2 = \frac{C_1}{f_{SW}\pi R_2 C_1 - 1}$$

With f_{SW} = 2.4 MHz, we calculate C_2 = 3.8 pF. This small capacitance is already included within the circuit due to parasitic elements. In addition, a lower C_2 boosts the phase at f_C a little bit, but has no influence on gain and phase below f_C. Therefore there is no need to insert this capacitor in the real circuit.

R3 and C3 define the second zero ω_{zero_2} and second pole ω_{pole_2} of the compensation network. The second zero is placed at the same frequency as the first zero, at half of the LC filter's double pole ω_0, whereas the second pole of the compensation is also placed at the same frequency as the first zero, at half of the switching frequency of the V_{CORE} regulator, so we now have a double pole at this frequency. With some modification, we get the following equations:

$$R_3 = \frac{R_1}{\frac{f_{SW}}{f_{LC}} - 1}$$

$$C_3 = \frac{1}{\pi f_{SW} R_3}$$

For the switching frequency f_{SW} = 2.4 MHz and the LC filter double pole frequency f_{LC} = 24 kHz, we calculate R_3 = 251 Ω and C_3 = 527 pF.

In order to meet the preferred component requirements list, the following values are selected:

C_1 = 390 pF R_1 = 24.9 kΩ R_3 = 249 Ω

C_3 = 560 pF R_2 = 34.8 kΩ

With the above selected values, we get the following zeros and poles for the compensation network:

$\omega_{zero\_1} \rightarrow$ 11.7 kHz $\omega_{pole\_1} \rightarrow$ 1.15 MHz

$\omega_{zero\_2} \rightarrow$ 11.3 kHz $\omega_{pole\_2} \rightarrow$ 1.15 MHz

The Bode diagram for the complete loop is shown in **Figure 8**. The gain rolls off with -20 db/decade at the selected crossover frequency of 150 kHz and the phase margin is always more than 45° for the range below the crossover frequency.

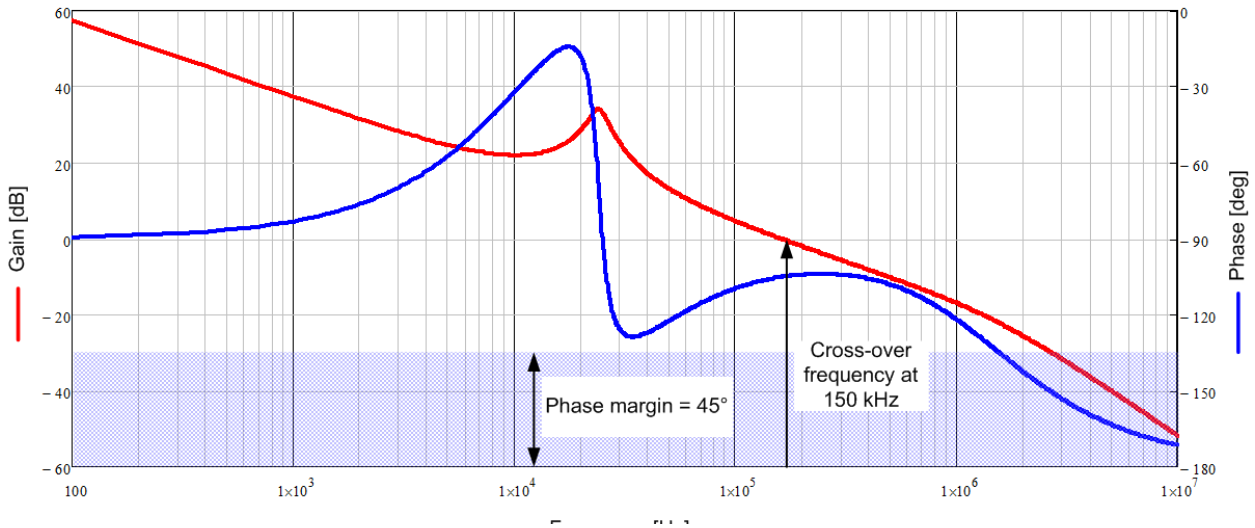

Figure 8. Frequency Response and Phase Margin for Complete System Loop

8 Conclusion

This application note shows how to design the proper compensation network for the V_{CORE} error amplifier of the MC33907 and MC33908. This compensation network has to be adjusted for different output voltages as well for different LC filters. The sharp phase lag caused by low ESR capacitors at the output always requires a type 3 compensation network.

Note: It is recommended to verify the calculated results with a tool like Spice or a mathematical program.

9 References

Author	Title, Publisher and Date
Pressmann, A., K. Billings and T. Morey	*Switching Power Supply Design*. New York: McGraw-Hill, 2009.

10 Revision History

Revision	Date	Description of Changes
1.0	10/2013	• Initial release

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