Parallel Configuration of H-Bridges

Featuring the MC33932 and MC34932 ICs

1   Introduction

Two or more H-bridges can be operated in parallel to increase the current handling capacity of the circuit. In this application note, paralleling of H-bridges has been exemplified using a dual H-bridge model MC33932/ MC34932. However, paralleling of H-bridges is not an easy task, as any offset or mismatch between the two MOSFETs can cause one of them to hit the overcurrent/temperature limit before the other, forcing very high-current through one of the H-bridges in parallel configuration, which may initiate device shutdown.

The objective of this application note is to present a method to obtain twice the current from a dual H-bridge by paralleling the dual H-bridges located on the same die. This document also presents the various methods to calculate the junction temperature, to ensure the device operates within the thermal limits specified in the data sheet.

Freescale analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

Contents

freescale

2 Background Information

Typically, the current carrying capacity of H-bridges are limited by power dissipation due to $I^2R_{DS(on)}$, switching losses, junction temperature, PCB temperature, ambient temperature, and thermal resistance across the various junctions in which the PC board structure plays a pivotal role. The IC packaging also plays a very important role in removing the heat from the die and keeping it away from the maximum temperature limits specified for the device.

The MC34932 and MC33932 are both monolithic dual H-bridge power integrated circuits, which have been embedded into a robust thermally enhanced package. They are designed for applications in automotive electronic throttle control, industrial motor and motion control, robotics, as well as aerospace applications. It can also be used for any low-voltage DC stepper motor control applications within the current, voltage, and frequency limits stated in the specifications.

In the MC34932/MC33932, each H-bridge is able to control inductive loads with currents up to a peak of 5.0 A. The RMS current capability is subject to the degree of heat-sinking provided to the device package. It has an internal peak current limiting (regulation), which gets activated at load currents above 6.5 A ± 1.5 A. Output loads can be pulse-width modulated (PWM-ed) at frequencies up to 11 kHz. A load current feedback feature provides a proportional (0.24% of the load current) current output suitable for monitoring by a microcontroller's A/D input. A Status flag output reports undervoltage, overcurrent, and overtemperature fault conditions. Two independent inputs provide polarity control of two half-bridge totem pole outputs. Two independent disable inputs are provided to force the H-bridge outputs to tri-state (high-impedance off state).
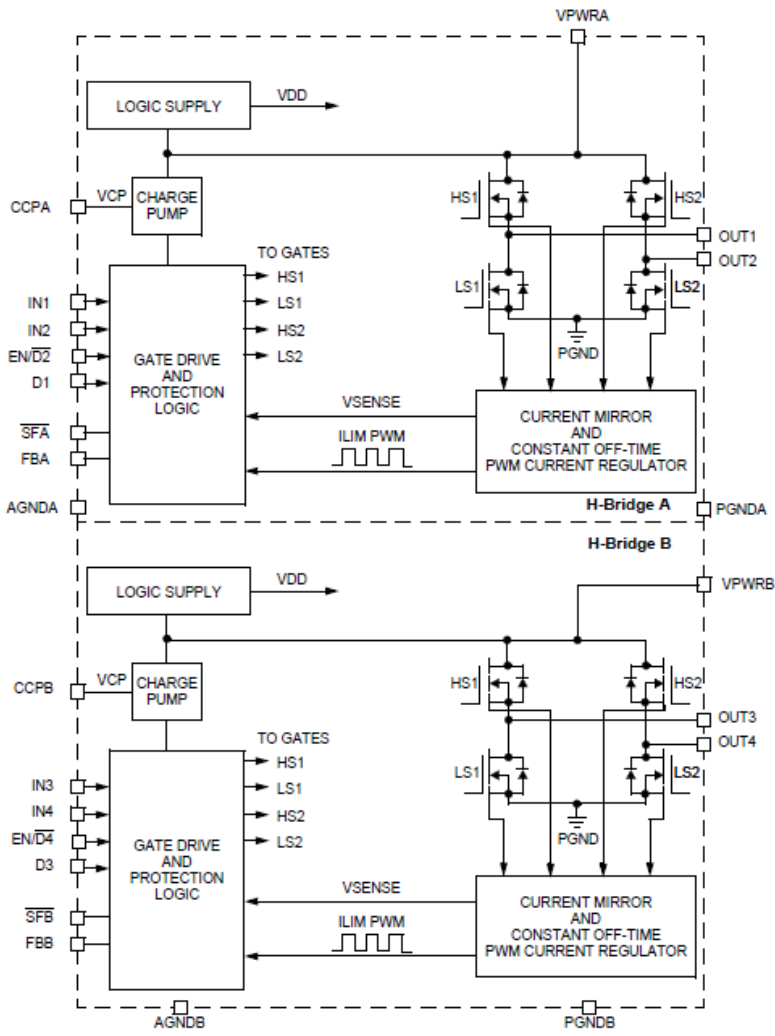

Figure 1. Block Diagram of the MC34932/MC33932

Figure 1 shows the internal block diagram of the dual H-bridge. It consists of two identical full H-bridges on same monolithic structure, with distinct gate drivers and current feedback outputs for external circuits enabling it to be used as stepper motor driver.

Paralleling two individual H-bridges in the MC34932/MC33932 can have two possible configurations. In the Figure 2 configuration, there is no doubling of current carrying capacity. Instead, the thermal performance of the device gets improved due to reduction of effective $R_{DS(on)}$. In the Figure 3 configuration, the current carrying capacity can be nearly doubled, when compared to a single H-bridge.

For this document, the parallel configuration of dual H-bridge is performed using evaluation boards with a 2s2p structure (part number KIT33932EKEVBE) consisting of the MC33932 in an SOIC-EP package.

A detailed description with theoretical analysis and explanation of each parallel H-bridge configuration are presented by the following.

3 Proposed Application Solution

In Figure 2, IN1, IN2, and OUT1, OUT2 are connected to form one input and output pair. Similarly, IN3, IN4, and OUT3, OUT4 are tied together to form another paralleled half H-bridge. As a result, the two power devices are now in parallel, due to the effective $R_{DS(on)}$, which reduces to half its original value, which in effect will cause 50% reduction in the power dissipation ($I^2R_{DS(on)}$) in the die. However, this configuration does not double the drive current of a single H-bridge, because the current limit is based on the sum of the currents through the low-side FETs, which remain unchanged. This configuration improves the overall thermal performance by reducing the power dissipation in the package.

The basic assumption is that the output stages are reasonably well matched, because they are part of the same monolithic structure. If two independent H-bridges are used (separate MC33926 or similar), the load sharing may not be quite as even, resulting in a reduction in the maximum drive capability. This configuration will latch any fault until the EN pin is toggled. Current limit will occur at the sum of the two low-side FET current mirrors. The same logic holds for overcurrent shutdown. The current feedback is properly scaled (the sum of the FET currents).
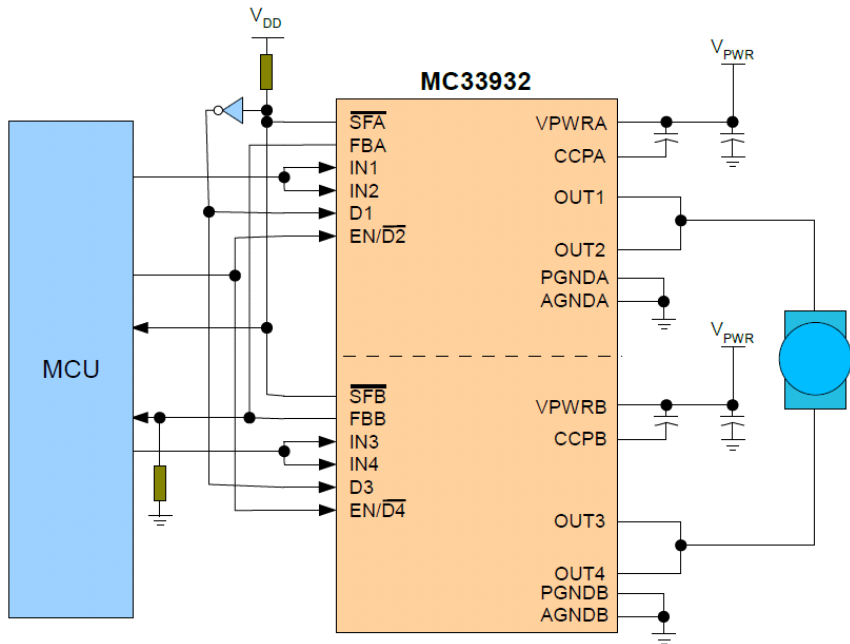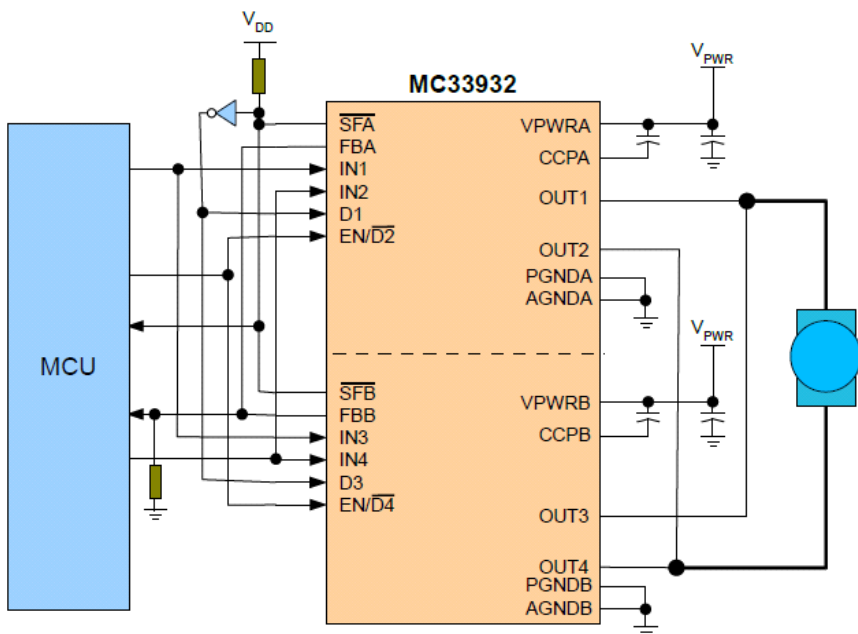

Figure 2. Configuration 1: Two H-bridges in Parallel

Figure 3. Configuration 2: Two H-bridges in Parallel

In the Figure 3 configuration, the high-side and low-side inputs are tied together and same is done for the outputs. In this case, the drive current of a single H-bridge can be doubled using the dual H-bridge part number MC34932/MC33932. The basic assumption is that the output stages are reasonably well matched, because they are part of the same monolithic structure. If two independent H-bridges are used (separate MC33926 or similar), the load sharing may not be quite as even, resulting in a reduction in maximum drive capability. This configuration will latch any fault until the EN pin is toggled.

Current limit will occur at the lowest of the two low-side FET current limit thresholds. Since both FETs are on the same die, they should be fairly well balanced, so the effective current limit would be approximately double the set point for a single device specified in the specification sheet of MC34932/MC33932. The same logic holds for overcurrent shutdown. With this configuration, about 10 A of peak current should be available to the load, as long as T_J is maintained below 150 °C. The current feedback is properly scaled (the sum of the FET currents).

4   Experimental Setup

The experimental setup consists of an evaluation board for the MC33932, which can be configured for parallel operation. A detailed schematic of the board is as follows.
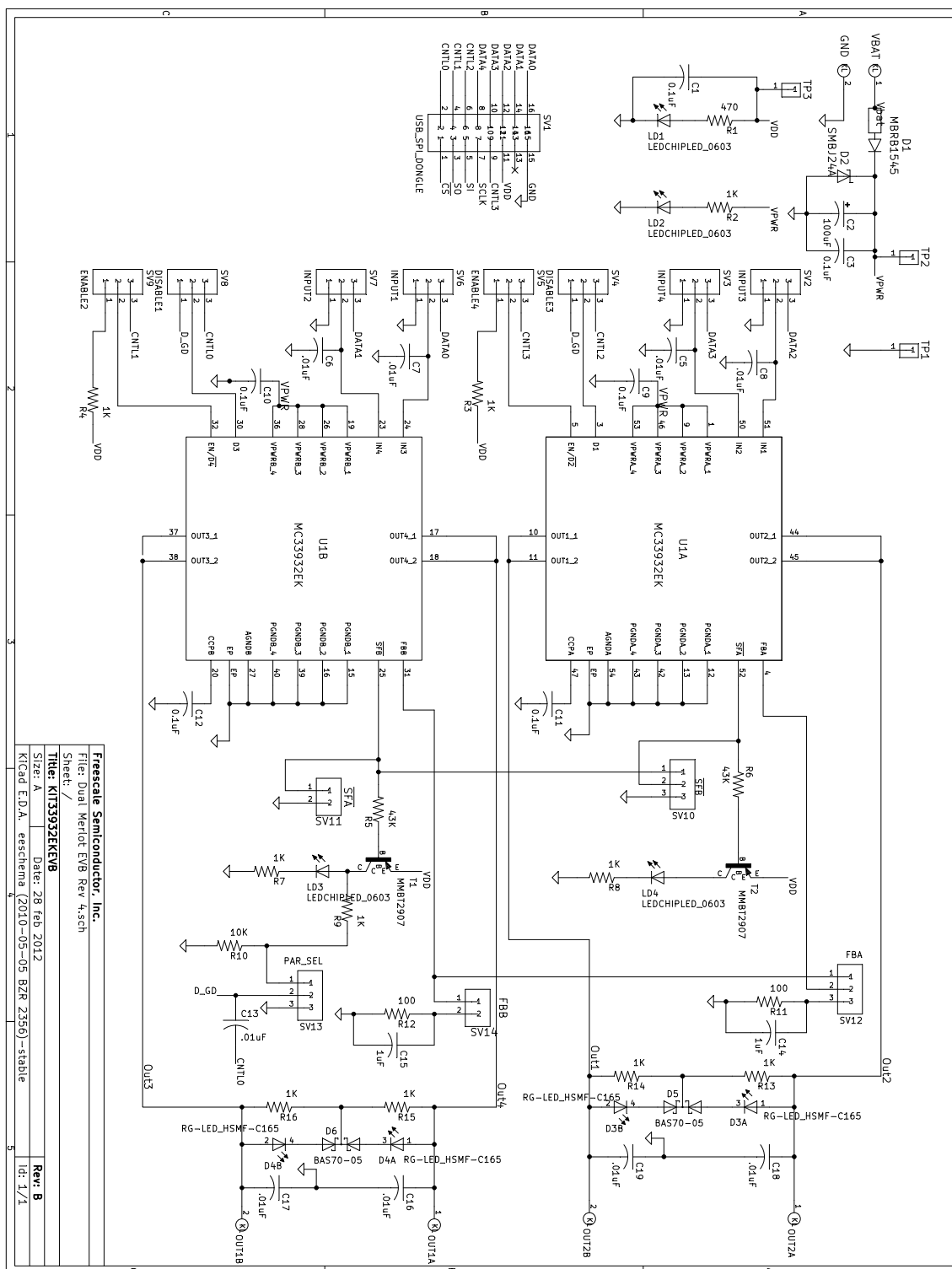

Figure 4. Block Diagram of the Physical Architecture

The jumpers on the evaluation board need to be configured as follows for parallel configuration. Note that the jumper PAR_SEL needs to have terminal 1 and 2 shorted together, as shown below for parallel operation. The H-bridge needs a 5.0 V pulse, which can be given by shorting the 5.0 V supply positive pin with the pin number 1 of SFA. Once the fault is cleared, the board starts functioning as two H-bridges in parallel.
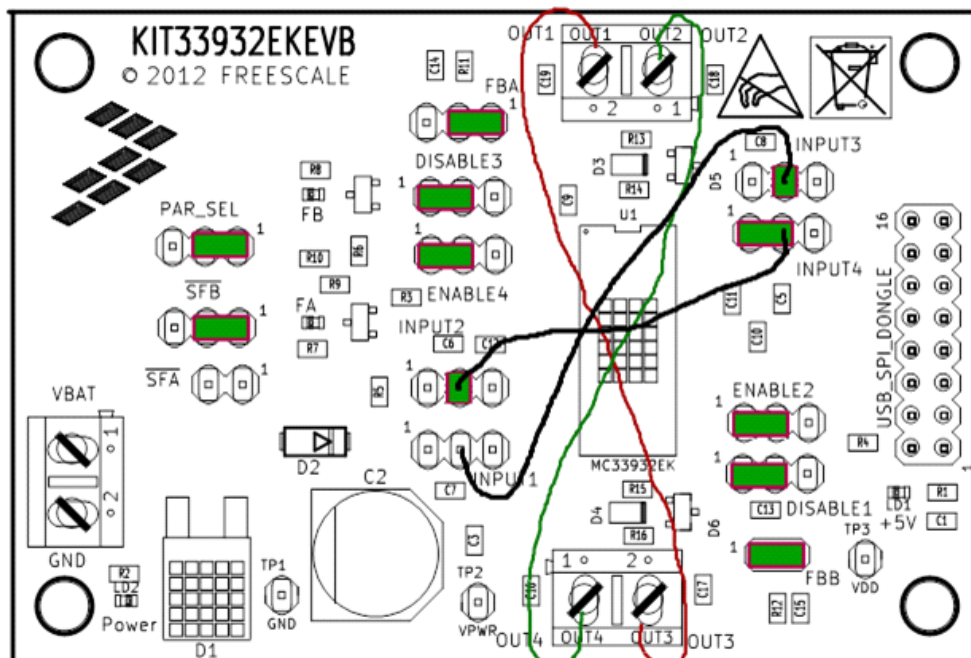

Figure 5. Jumper Settings and External Connections for Parallel Configuration of a Dual H-bridge MC3X932

While operating the two devices in parallel, it is important to consider and measure the junction temperature as if it exceeds the current foldback temperature value (T_{FB}) the internal PWM circuit starts to limit the output current. It is not possible to measure the junction temperature threshold (T_J) by direct measurement. However, based on the case and board temperatures, the junction temperature can be approximated using the thermal resistance values of junction to board and junction to package tops respectively, as specified in the data sheet. However, both methods require Watt calculations of power dissipated in the package. The power dissipation can be calculated, as shown in the following section.

4.1   Power Dissipation Calculation

In a motor driver IC, there are many sources of power dissipation. However, in steady state operation without any switching activity, the majority of power dissipation takes place at the on resistance ($R_{DS(on)}$) of the MOSFET device. Other sources such as standby power dissipation at the internal supplies and regulators and leakage power are typically negligible.

4.2 Power Dissipation Due to On-resistance ($R_{DS(on)}$)

When the drive is used in steady-state without any form of switching, is the biggest source of power dissipation in a motor driver IC. The power dissipated to the MOSFETs on the high-side (HS) and low-side (LS) in an H-bridge can be calculated as follows:
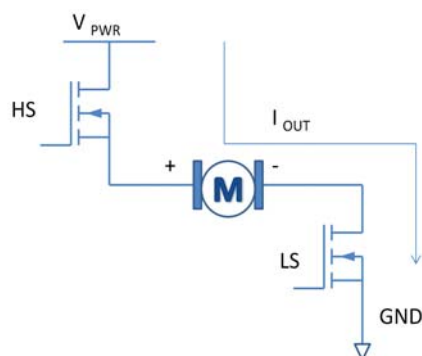

Figure 6. Evaluation Board Schematic

$$P\_R_{DS(on)} = I_{OUT}{}^2*(HS\_ R_{DS(on)}) + I_{OUT}{}^2*(LS\_ R_{DS(on)}) \qquad (1)$$

The HS_ $R_{DS(on)}$ and LS_ $R_{DS(on)}$ are the on resistances of high-side (HS) and low-side (LS) switches, respectively. I_{OUT} is the RMS value of output current. One important thing to note is that $R_{DS(on)}$ increases with junction temperature. Power calculations based on specified nominal values $R_{DS(on)}$ in the data sheet will lead to errors in calculations. To determine the correct value, the following setup in Figure 7 can be used.
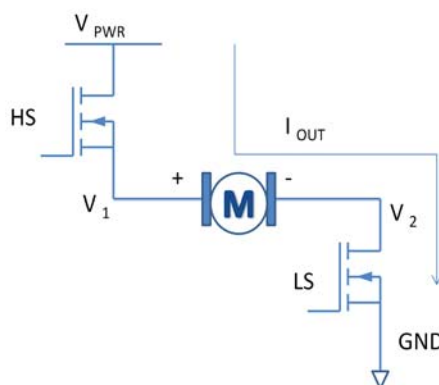

Figure 7. Setup to Calculate Power Dissipation H-Bridges

Since the current flowing through the device is constant throughout the circuit, the voltage drop across the HS_$R_{DS(on)}$ and LS_ $R_{DS(on)}$ will give the correct values of power dissipation. To calculate power dissipation, the following formula can be used.

Power dissipation at HS: $(V_{PWR} - V_1)*I_{OUT}$ $\qquad (2)$

Power dissipation at LS: V_2*I_{OUT} $\qquad (3)$

Total power dissipation due to $R_{DS(on)}$ = P_RDSon = $(V_{PWR} - V1)*I_{OUT} + V_2*I_{OUT}$ $\qquad (4)$

4.3 Power Dissipation Due to Internal Supply

The internal supplies and regulators consume some power due to operating supply current I_S. The power dissipated from the operating supply current due to the presence of V_{PWR} supply voltage in the IC is given by the following equation.

$$P_{IS} = V_{PWR}*I_S \qquad (5)$$

4.4 Power Dissipation Due to Switching

The input pins on the MC34932/MC33932 can be connected to the PWM signal to control the current at the output load up to 11 kHz. However, switching causes a lot of power dissipation, which accounts for the switching losses. These losses can be attributed to the output MOSFETs transitioning through the linear region, while switching causing more power dissipation. The switching losses are contingent upon the following factors:

- Switching frequency (f_{SW}).
- Rise time (t_R) while switching from low to high and fall time (t_F) during high to low transitions.
- Supply voltage (V_{PWR}).
- Output current (I_{OUT}).

From the previous factors, it is evident that any application requiring lot of switching, such as stepper motor drives will account for high switching losses. However, for non-switching applications, switching losses can be neglected. The power dissipated while switching may be estimated using the following equations.

$$P_{SW(Rise)} = 1/2 * V_{PWR} * I_{OUT} * t_R * f_{SW} \tag{6}$$

$$P_{SW(Fall)} = 1/2 * V_{PWR} * I_{OUT} * t_F * f_{SW} \tag{7}$$

$$P_{SW(Total)} = 1/2 * V_{PWR} * I_{OUT} * (t_R + t_F) * f_{SW} \tag{8}$$

4.5 Total Power Dissipation

Total power dissipation in the IC can be given by the following equation.

$$P_{TOT} = P\_R_{DS(on)} + P_{IS} + P_{SW(Total)} \tag{9}$$

4.6 Junction Temperature Estimation with Case Temperature

In this method, junction temperature calculations require the case/package top temperature (T_{CASE}) and package top thermal resistance (θ_{JT}), in addition to the total power dissipation in the IC (P_{TOT}). This is one of the common methods of estimating the junction temperature inside the IC. The junction to package top thermal resistance (θ_{JT}) does not vary much from one part to another. However it does get impacted with ambient conditions. The typical values specified in the datasheet are for the JEDEC JESD51-2 standard. While estimation of junction temperature using this method, special care should be taken in maintaining the ambient conditions as per the JEDEC JESD51-2 standard. Otherwise, θ_{JT} for the testing condition must be determined. Unlike θ_{JB} and θ_{JT}, do not vary much with the change in ambient condition.

4.7 Case temperature measurement

The case temperature (T_{CASE}) can be measured while the device is dissipating power, using a fine wire thermocouple (36-40 AWG) glued to center of the case using epoxy glue. Fine wire of a thermocouple prevents sinking heat through the thermocouple junction.

Another effective method of measuring the case temperature (T_{CASE}) is by using an IR camera which is focused at the center of the case top, as shown in the Figure 8. The package top temperature is 150 °C at the center, which happens to be the hottest spot of the die.
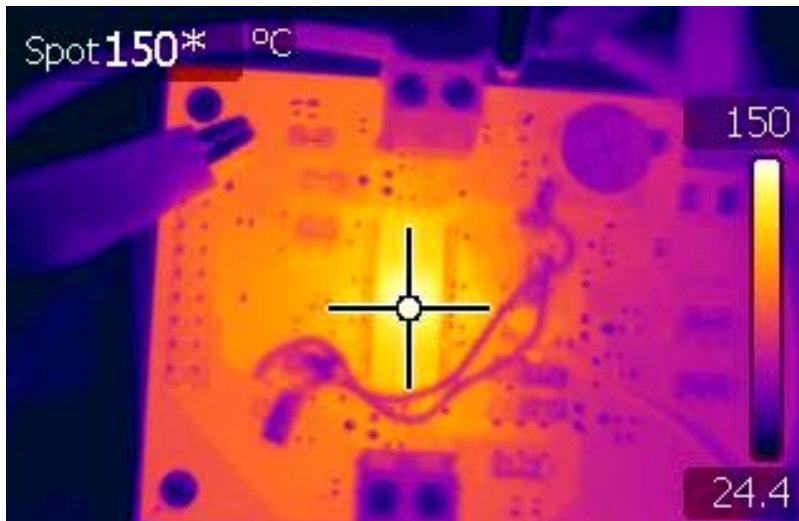
Figure 8. IR camera Image with Focus at the Center of the Package Top

Once the case temperature is known, the junction temperature can be estimated by plugging in the values in the following equation.

$$T_J = T_{CASE} + \theta_{JT} * P_{TOT} \qquad\qquad (10)$$

Equation (10) gives a good estimation of junction temperature. As discussed above, it is just an approximation, because the junction temperature is a function of package top thermal resistance, which varies according to the ambient conditions.

A better estimation of junction temperature can be achieved by calibrating the ESD diodes on the pin as temperature sensors. More details of this method are explained in the following section.

4.8   Using ESD Diodes as Temperature Sensors

Every input and output pin in the MC34932 and MC33932 has ESD protection diodes, as shown in Figure 9. It is a fact that diode voltage (V_D) decreases with increasing temperature. This characteristic of a diode is very precise and reliable, making it a good temperature sensor once calibrated. The calibration is quite simple, and can be done by putting the diode in known temperature zones and recording the corresponding diode voltages, while they are forward biased with a constant current source (CS), and with a current (I_F) low enough not to cause self heating in the device. A typical behavior of the diode voltage with a change in die temperature, while a constant current flows through the device, is shown in Figure 10. Constant current sources in the range of 1.0 mA to 1.5 mA may be a good choice. The setup is shown in Figure 9.
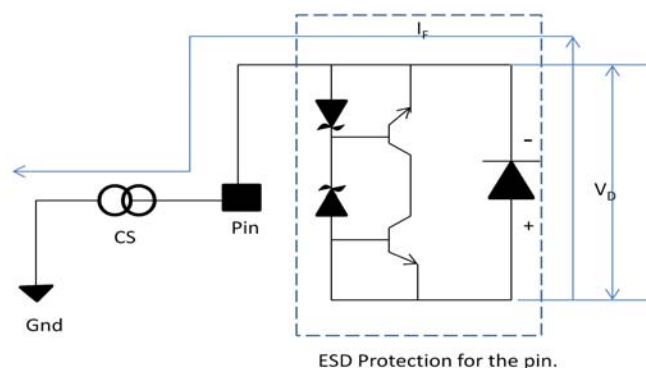

ESD Protection for the pin.

Figure 9. ESD Protection Structure for Input Pin with Setup to Measure Die Temperature

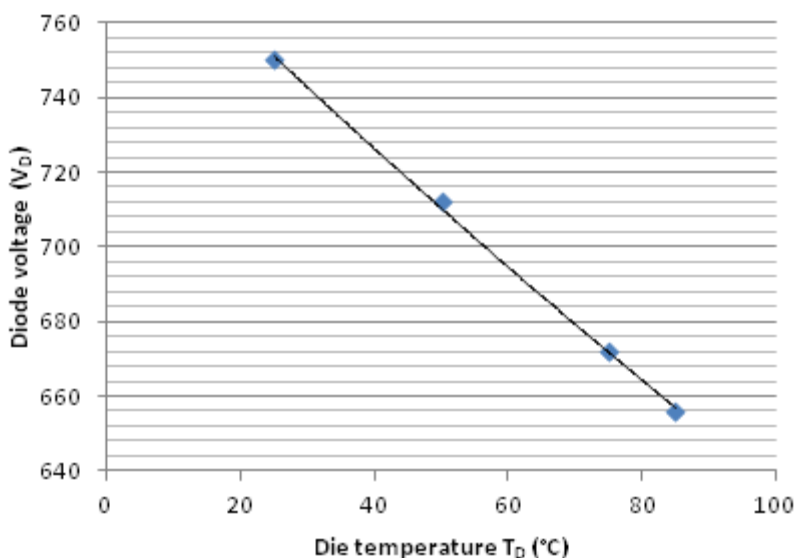**Figure 10. Typical Characteristic of the Diode as Temperature Sensor with I_D = 1 mA**

4.9   Parallel Configuration of H-Bridges

When two H-bridges are in parallel, the outputs and inputs of the two individual H-bridges on the MC34932/MC33932 formed by HS1, LS1, and HS2, LS2 are connected on the board, as shown in Figure 11, which also shows the equivalent circuit for the configuration 2 in forward mode, as explained previously.
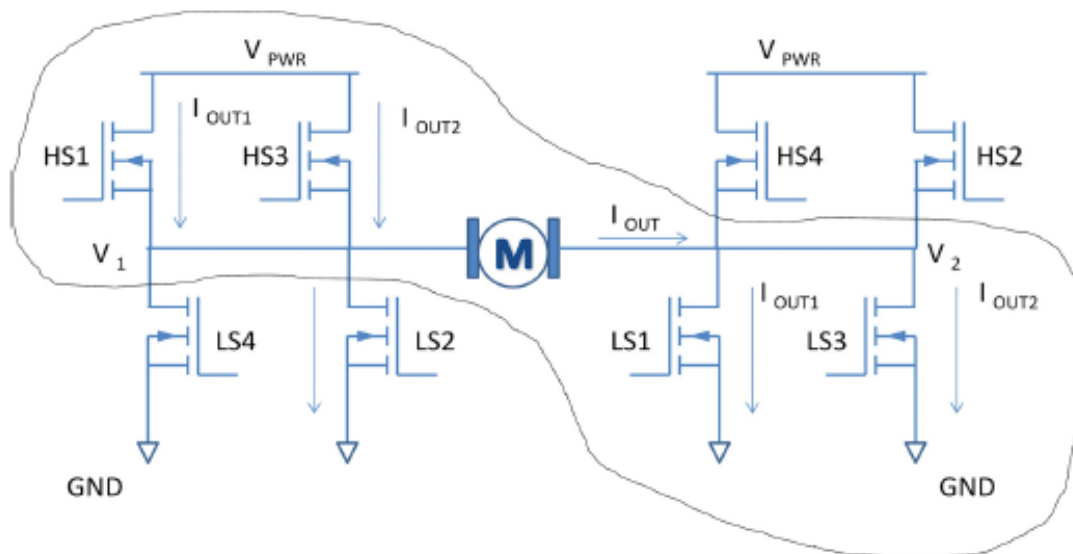

Figure 11. Equivalent Circuit of Paralleled Dual H-bridge

In this configuration, the gate control of two H-bridges are tied together to form centralized control of the two devices.

$$I_{OUT} = I_{OUT1} + I_{OUT2}$$

One important point to consider is that these are two different MOSFETS on the same die. The threshold values for current limiting is nearly the same if not exactly equal. There could be a small difference or offset in the current flowing through the two H-bridge circuits. This can be verified by monitoring the current flowing through the current feedback output pins, FBA and FBB, giving 0.24% of the total output current from individual H-bridges configured for parallel operation, and characterizing each feedback port individually, by operating it at different temperatures to minimize any offset or errors in

measurement. Any difference in the current limiting threshold or current distribution between the two H-bridges in parallel configuration can activate a status fault, which can be explicated with the following example.

4.10 Example

The values in this example were obtained from one experiment performed with an MC33932 evaluation board. Gates were connected to a PWM signal of 3.0 kHz frequency and 50% duty cycle, while maintaining the junction temperature below T_{LIM}. The load used for the experiment is a throttle control actuator motor with a resistance of 1.17 Ω and inductance of 100 mH at 100 Hz. One may expect similar values with the same device and board.

Note: The current values in this section refer to peak-to-peak values. The RMS values will be different and will depend on the duty cycle and the peak value of the PWM signal.

As per the data sheet, the current limiting threshold (I_{LIM}) has minimum value of 5.2 A with a typical of 6.5 A and a maximum up to 8.0 A. Assume that I_{LIM} = 6.5 A for both the H-bridges.

Table 1. Current Limiting Threshold (I_{LIM})

V_{PWR}	V_1	V_2	I_{OUT1}	I_{OUT2}	I_{OUT}	P_RDSon	$P_{SW(Total)}$	P_{TOT}
19	14.9	1.24	6.5	6.6	13.1	70.488	5.9736	76.4616

H-Bridge 1: HS1 and LS1 with I_{OUT1} = 6.5 A
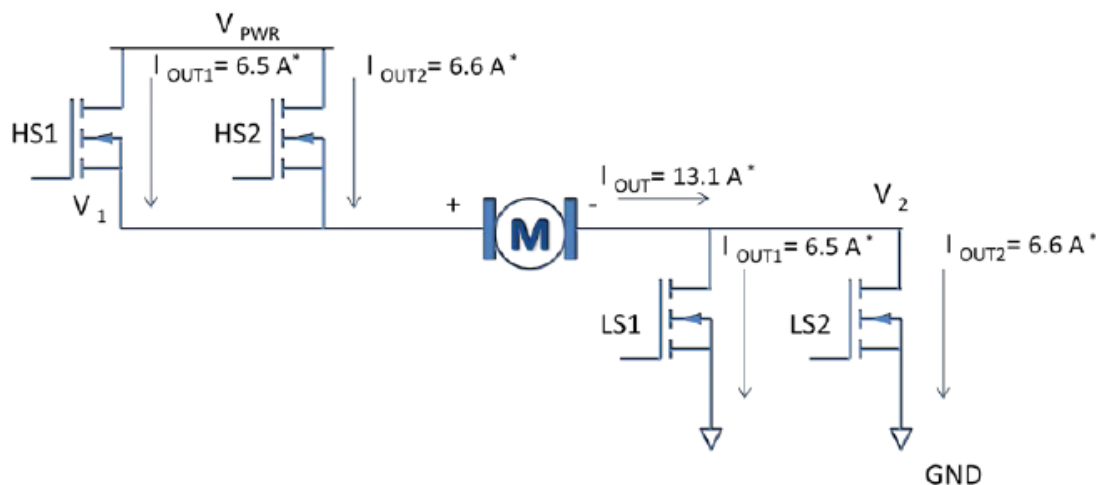
H-Bridge 2: HS2 and LS2 with I_{OUT2} = 6.6 A

Figure 12. Current Distribution for H-bridges in Parallel Configuration

There is a slight offset of 0.1 A between the output current in the two bridges, even though they are on the same die. This could be due to several process reasons such as local ambient condition and process variations. For the previous case, I_{OUT1} = 6.5 A and I_{OUT2} = 6.6 A as I_{OUT2} > I_{LIM}, the H-Bridge 2 starts the internal current limiting before H-Bridge 1, by initiating the internal PWM circuit. In this scenario, when H-Bridge 2 current reaches its minimum value, which is close to 0.0 A, the entire current in the circuit is forced through H-Bridge 2, which is about 6.5 + 6.6 = 13.1 A. As a result, it exceeds the short-circuit current threshold (I_{SCL}) minimum value of 9.0 A, as well as the typical 11.0 A value, and initiates a short-circuit fault condition, putting the circuit into sleep mode. This limits the maximum current through the parallel H-bridge of up to 13.0 A. An asynchronous activation of current limiting due to unequal current distribution among the H-bridges, imposes a limit on the amount of current handled by the two H-bridges in parallel configuration beyond the current limiting threshold (I_{LIM}).

5 Factors Affecting Current Handling Capacity

The previous example points out some of the limitations of using two H-bridges in parallel, when activating the internal PWM circuit while the device starts to limit current. There are several factors which should be considered while configuring two independent H-bridges in parallel mode. Some factors are discussed in the following sections.

5.1 Dynamic Current Sharing

Although the two power devices are on the same die in a monolithic structure with almost identical on resistance ($R_{DS(on)}$) and transconductance (g_m), there are several other parameters which can cause unequal sharing in a dynamic condition among the two MOSFETs. While the two devices operate in parallel with the gates connected to the PWM signal with very low duty cycles, the steady state current sharing among the devices, based on variation of $R_{DS(on)}$ with respect to temperature variation (which will be negligible for steady state), may not continue to hold true. For PWM signals connected to gates, the mismatch between the gate drivers also needs to be considered. This may be attributed to parasitic capacitance, resistance, and delay paths within the circuit. Within the printed circuit board, there could be additional parasitic capacitance and resistance, making the situation more complicated. Activation of internal PWM while limiting current can cause unequal instantaneous distribution between the two devices. This could become a problem while operating the device near its upper threshold limit (I_{LIM}), as explicated in the previous example.

5.2 Switching Losses

With switching circuits in power electronics, switching losses form a major part of the total power dissipation engendering an increase in junction temperature. For the above example, with rise and fall time (t_R and t_F) of 8.0 µs the switching losses accounted for significant percentage of total power dissipation with increasing frequency which can trigger thermal shutdown by converting the dissipated power into heat.

H-bridge 1: $P_{SW1(Total)} = 1/2 * V_{PWR} * I_{OUT1} * (t_R + t_F) * F_{SW}$

H-bridge 2: $P_{SW2(Total)} = 1/2 * V_{PWR} * I_{OUT2} * (t_R + t_F) * F_{SW}$

H-bridge 1 and 2: $P_{SW(Total)} = 1/2 * V_{PWR} * (I_{OUT1} + I_{OUT1}) * (t_R + t_F) * F_{SW}$

Plugging in values from Table 1 and $t_R = t_F = 8.0$ µs, $P_{SW(Total)} = 5.9736$ W. The gate connected to the PWM signal with a 3.0 kHz frequency and a 50% duty cycle, the switching losses are from 7.81% of the total power dissipation. With the highest frequency of 11 kHz, switching losses with same condition will be 23.7% of the total power dissipation.

6   Conclusion

The following summary gives the findings and recommendations concerning the configuration of dual H-bridge for parallel operation.

Since the two H-bridges are on same monolithic die, the variation in static current sharing, is minimum as as it is mainly contingent upon minimal $R_{DS(on)}$ variation. Assuming there is enough heat sinking to prevent thermal shutdown of the device, and operating the device close to the current limit thresholds, even slightest of variation in current sharing can trigger overcurrent shutdown as one of the paralleled low-side FETs start to current limit before the other, letting the entire current to flow through the other arm and exceeding the over-current shutdown threshold.

While switching the gates of the paralleled device with an external PWM signal, the dynamic current sharing is different from static current sharing. Dynamic current sharing comes into the picture when either gate is switched externally with a PWM signal, or the internal PWM circuit gets triggered by the thermal current limiting circuit. This could be due to the parasitic capacitors, resistors, and delay paths within the circuit and the pc board, which would depend on the layout of the device and PC board. Try to layout the circuit symmetrically, which will alleviate the issue of unequal dynamic current sharing, by matching the parasitic capacitance, inductance, and resistance.

Switching losses account for a significant fraction of total power dissipation, which gets converted into heat and could possibly trigger over-temperature shutdown, or if the heat sinking capacity in the system is not enough to transfer the heat to the atmosphere, keeping the device below the thermal shutdown temperature threshold, consider adding an external heat sink.

Heat sinking capability of the system may be enhanced by using more copper, adding thermal vias, external heat sinks, more layers in PCB, and symmetrical layout of circuit.

7 References

The following are URLs where you can obtain information on related Freescale products and application solutions:

Document Number and Description		URL
MC33932	Data Sheet	www.freescale.com/files/analog/doc/data_sheet/MC33932.pdf
MC34932	Data Sheet	www.freescale.com/files/analog/doc/data_sheet/MC34932.pdf
Freescale.com Support Pages		**URL**
MC33932 - Product Summary Page		http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC33932
MC34932 - Product Summary Page		http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC34932
Power Management Home Page		http://www.freescale.com/PMIC
Analog Home Page		http://www.freescale.com/analog

8   Revision History

Revision	Date	Description
1.0	1/2014	• Initial release

Document Number: AN4833
Rev.1.0
1/2014