NXP Semiconductors
Application Note

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Power Management of Xilinx AP SoC using NXP PMIC

Featuring the MMPF0100

1 Introduction

This document provides a power management solution for Xilinx Zynq®-7000 System-on-Chips (SoCs), with the Xilinx ZedBoard highlighted as a design example. The ZedBoard is a development board with a broad range of expansion options and the Zynq®7000 as its on-board processor. The document presents the power rail requirements of the Xilinx Zynq®-7000 All Programmable SoCs, many of which are also applicable to Xilinx Field Programmable Gate Arrays (FPGAs). For more details about the specific devices contained in this note, visit www.nxp.com or contact the appropriate product application team.

The PF0100 is NXP's Power Management IC (PMIC) that integrates a total of 14 regulators. Its flexibility in the range of voltage and current options makes it an optimum choice in a wide range of applications. This application note addresses the ability of the PF0100 to provide an optimal solution to the power requirements of a Zynq®-7000 based system taking into account typical I/O, memory and peripherals that are interfaced with the ZedBoard.

NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

Contents

2 ZedBoard

2.1 ZedBoard overview

The Xilinx ZedBoard is an evaluation and development board based on the Xilinx Zynq®-7000 All Programmable SoC (AP SoC). The ZedBoard provides appropriate hardware capabilities for interfacing with a number of peripherals and compatible expansion headers for Xilinx Analog to Digital Convertor (XADC), FPGA Mezzanine Card (FMC) and Diligent Pmod™.

2.2 ZedBoard features

The ZedBoard features are:

Table 1. ZedBoard features

Feature	Description
Processor	Zynq®-7000 AP SoC XC7Z020-CLG484-1
Memory	512 MB DDR3 256 Mb Quad-SPI Flash 4.0 GB SD card
Communication	Onboard USB-JTAG Programming 10/100/1000 Ethernet USB OTG 2.0 and USB-UART
Expansion Connectors	Expansion connectors FMC-LPC connector (68 single-ended or 34 differential I/Os) Five Pmod™ compatible headers (2x6) Agile Mixed Signaling (AMS) header
Clocking	33.33 MHz clock source for PS 100 MHz oscillator for PL
Display	HDMI output supporting 1080p60 with 16-bit, YCbCr, 4:2:2 mode color VGA output (12-bit resolution color) 128 x 32 OLED display
Configuration and Debug	Onboard USB-JTAG interface Xilinx Platform Cable JTAG connector
General Purpose I/O	Eight user LEDs Seven push buttons Eight DIP switches

3 Zynq®-7000 SoC

3.1 Zynq®-7000 SoC overview

The Xilinx Zynq®-7000 is a family of All Programmable SoCs, aimed at a range of applications from radio and LTE to defense-grade applications. The versatile nature and adaptability of the SoC makes it suitable for multiple applications. The Zynq®-7000 SoC in discussion here, XC7Z020-CLG484-1, has an ARM® Cortex A9 processor with a maximum frequency capability of 667 MHz.

3.2 Zynq®-7000 SoC features

The Zynq®-7000 SoC features include:

Table 2. Zynq-XC7Z020-CLG484-1 features

Feature	Description
Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™
Processor Extensions	NEON™ and Single/Double Precision Floating Point for each processor
Maximum Frequency	667 MHz
L1 Cache	32 KB Instruction, 32 KB Data per processor
L2 Cache	512 KB
On-Chip Memory	256 KB
External Memory Support	DDR3, DDR3L, DDR2, LPDDR2
External Static Memory Support	2x Quad-SPI, NAND, NOR
DMA Channels	Eight (4 dedicated to Programmable Logic)
Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO
Peripherals w/ Built-in DMA	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO
Security	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot and for Secure Programmable Logic Configuration
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory, AXI 64b ACP, 16 Interrupts
Programmable Logic Cells (Approximate ASIC Gates)	85 k Logic Cells (~1.3 M)
Look Up Tables (LUTs)	53,200
Flip-Flops	106,400
Extensible Block RAM (# 36 Kb Blocks)	560 KB (140)
Programmable DSP Slices (18 x 25 MACCs)	220
Peak DSP Performance (Symmetric FIR)	276 GMACs
Analog Mixed Signal (AMS)/XADC	2 x 12 bit, MSPS ADCs with up to 17 Differential Inputs
Processing System User I/Os (excludes DDR dedicated I/Os)	54
Multi-standards and Multi-voltage Select IOTM Interfaces (1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V)	200

3.3 Power profile requirements

Zynq® Z-7020 has three different sets of voltage requirements, one each for the following: Processing System (PS), Programming Logic (PL) and the XADC. Each set in turn has a number of different voltage level requirements. The voltage profile recommendations from Xilinx are as listed in **Table 3**

Table 3. Recommended voltage levels

Symbol	Description	Min.	Typ.	Max.	Units	Notes
PROCESSING SYSTEM (PS)						
V_{CCPINT}	PS Internal Supply Voltage	0.95	1.00	1.05	V	
V_{CCPAUX}	PS Auxiliary Supply Voltage	1.71	1.80	1.89	V	
V_{CCPLL}	PS PLL Supply Voltage	1.71	1.80	1.89	V	
V_{CCO_DDR}	PS DDR I/O Supply Voltage	1.14	–	1.89	V	
V_{CCO_MIO}	PS MIO I/O Supply Voltage for MIO Banks	1.71	–	3.465	V	
V_{PIN}	PS DDR and MIO I/O Input Voltage	-0.20	–	V_{CCO_DDR} + 0.20 V_{CCO_MIO} + 0.20	V	
PROGRAMMING LOGIC (PL)						
V_{CCINT}	PL Internal Supply Voltage	0.95	1.00	1.05	V	
V_{CCAUX}	PL Auxiliary Supply Voltage	1.71	1.80	1.89	V	
V_{CCBRAM}	PL Block RAM Supply Voltage	0.95	1.00	1.05	V	
V_{CCO}	PL Supply Voltage for 3.3 V High Range I/O Banks	1.14	–	3.465	V	
V_{IN}	I/O Input Voltage	-0.20	–	V_{CCO} + 0.20	V	
	I/O Input Voltage (when V_{CCO} = 3.3 V) for V_{REF} and Differential I/O Standards Except TMDS_33	-0.20	–	2.625	V	
V_{CCBATT}	Battery Voltage	1.0	–	1.89	V	(1)
XADC						
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V	
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V	

Notes:

1. V_{CCBATT} applies only when using bitstream encryption and is otherwise tied to V_{CCAUX} or ground.

Note:

1. These voltage ranges are the recommended supply ranges and are what the power system design in consideration is expected to deliver. Further, to ensure safe operation, the power system should be able to support these voltages at the recommended accuracies summarized in **Table 4**.

Table 4. Required accuracy levels on the different rails

Voltage	Accuracy
V_{CCPINT}	±5.0%
V_{CCPAUX}	±5.0%
V_{CCPLL}	±5.0%
V_{CCO_DDR}	±5.0%
V_{CCO_MIO}	±5.0%

Table 4. Required accuracy levels on the different rails (continued)

V_{PIN}	—
V_{CCINT}	±5.0%
V_{CCAUX}	±5.0%
V_{CCBRAM}	±5.0%
V_{CCO}	±5.0%
V_{IN}	—
V_{CCBATT}	—
V_{CCADC}	±5.0%
V_{REFP}	±0.2%, 50 ppm/℃

The current drawn is an important consideration in power supply designs. A robust power system takes into account worst-case considerations in order to arrive at an optimal value for the maximum current drawn. The currents drawn by the particular device in consideration, XC7Z020-CLG484-1, are documented in **Table 5**:

Table 5. Quiescent currents

Symbol	Description	Current
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	122 mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	13 mA
I_{CCDDRQ}	PS quiescent V_{CCO_DDR} supply current	4.0 mA
I_{CCINTQ}	PL quiescent V_{CCINT} supply current	78 mA
I_{CCAUXQ}	PL quiescent V_{CCAUX} supply current	38 mA
I_{CCOQ}	PL quiescent V_{CCO} supply current	3.0 mA[(2)]
$I_{CCBRAMQ}$	PL quiescent V_{CCBRAM} supply current	6.0 mA
Total quiescent supply current is 264 mA.		

Notes
2. In addition to the above mentioned quiescents, **Table 6** shows the minimum current required by the Zynq® device for proper power-on and configuration.

Table 6. Power-on currents[(3)]

Symbol	Description	Current
$I_{CCPINTMIN}$	Minimum power-on V_{CCPINT} supply current	192 mA
$I_{CCPAUXMIN}$	Minimum power-on V_{CCPAUX} supply current	53 mA
$I_{CCDDRMIN}$	Minimum power-on V_{CCO_DDR} supply current	104 mA
$I_{CCINTMIN}$	Minimum power-on V_{CCINT} supply current	148 mA
$I_{CCAUXMIN}$	Minimum power-on V_{CCAUX} supply current	98 mA
I_{CCOMIN}	Minimum power-on V_{CCO} supply current	453 mA
$I_{CCBRAMMIN}$	Minimum power-on V_{CCBRAM} supply current	46 mA
Total power-on current is 1094 mA.		

Notes
3. The currents are calculated assuming one DDR bank and five HR I/O banks. The values of $I_{CCDDRMIN}$ and I_{CCOMIN} increase or decrease by 100 mA and 90 mA per bank respectively for a corresponding increase or decrease in the number of banks.

The Xilinx Power Estimator (XPE) tool acts as a very important step in the pre-implementation phase of the design. Once the device startup currents are met, the current demand on each rail must be satisfied. The XPE provides an estimate of these currents, based on user inputs, and the worst case estimate helps decide the power system configuration.

Table 7 provides an approximate estimate of the current drains on each of the supply rails, obtained from the XPE. This estimate is based on the ZedBoard's utilization of the Zynq®-7000 device.

Table 7. Current drain on supplies

Symbol	Description	Current
I_{CCPINT}	Current drawn on V_{CCPINT} supply	0.8 A
I_{CCPAUX}	Current drawn on V_{CCPAUX} supply	0.04 A
I_{CCDDR}	Current drawn on V_{CCO_DDR} supply	0.4 A
I_{CCINT}	Current drawn on V_{CCINT} supply	1.9 A
I_{CCAUX}	Current drawn on V_{CCAUX} supply	0.5 A
I_{CCPLL}	Current drawn on V_{CCPLL} supply	0.11 A
I_{CCBRAM}	Current drawn on V_{CCBRAM} supply	0.1 A

3.4 Power-on sequence

The processor-centric approach of the Zynq® SoC requires the processor to be powered up first. This results in the V_{CCINT} rail occupying top priority in the power-up sequence. The PS and PL rails can be powered up independent of each other as they are isolated from each other in order to prevent damage. The device specification recommends that the power-off sequence be the reverse of the power-on sequence. **Figure 1** shows a recommendation for the power-on sequence.

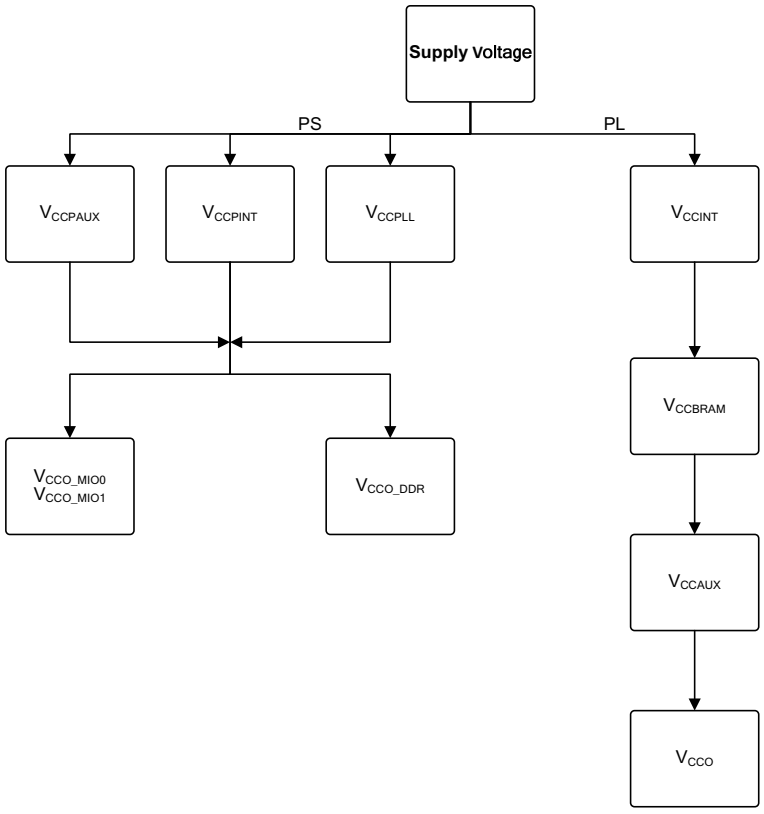

Figure 1. Power-on sequence

Table 8 and Figure 2 illustrate the constraints on the ramp times. $t_{VCCO2VCCAUX}$ is the time for which the difference between the I/O's supply in the PS or PL (V_{CCO_MIO} or V_{CCO}) and the corresponding auxiliary supply (V_{CCPAUX} or V_{CCAUX}) can exceed 2.625 V. $t_{VCCO2VCCAUX}$ has to be below 800 ms when the junction temperature is 85 °C and below 300 ms for a junction temperature of 125 °C. This constraint has to be followed to maintain safe operation of the device.

Table 8. Power supply ramp times

Symbol	Description	Min	Max	Units
$t_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}	0.2	50	ms
$t_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}	0.2	50	ms
t_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}	0.2	50	ms
t_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}	0.2	50	ms
t_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}	0.2	50	ms
t_{VCCO}	Ramp time from GND to 90% of V_{CCO}	0.2	50	ms
t_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}	0.2	50	ms

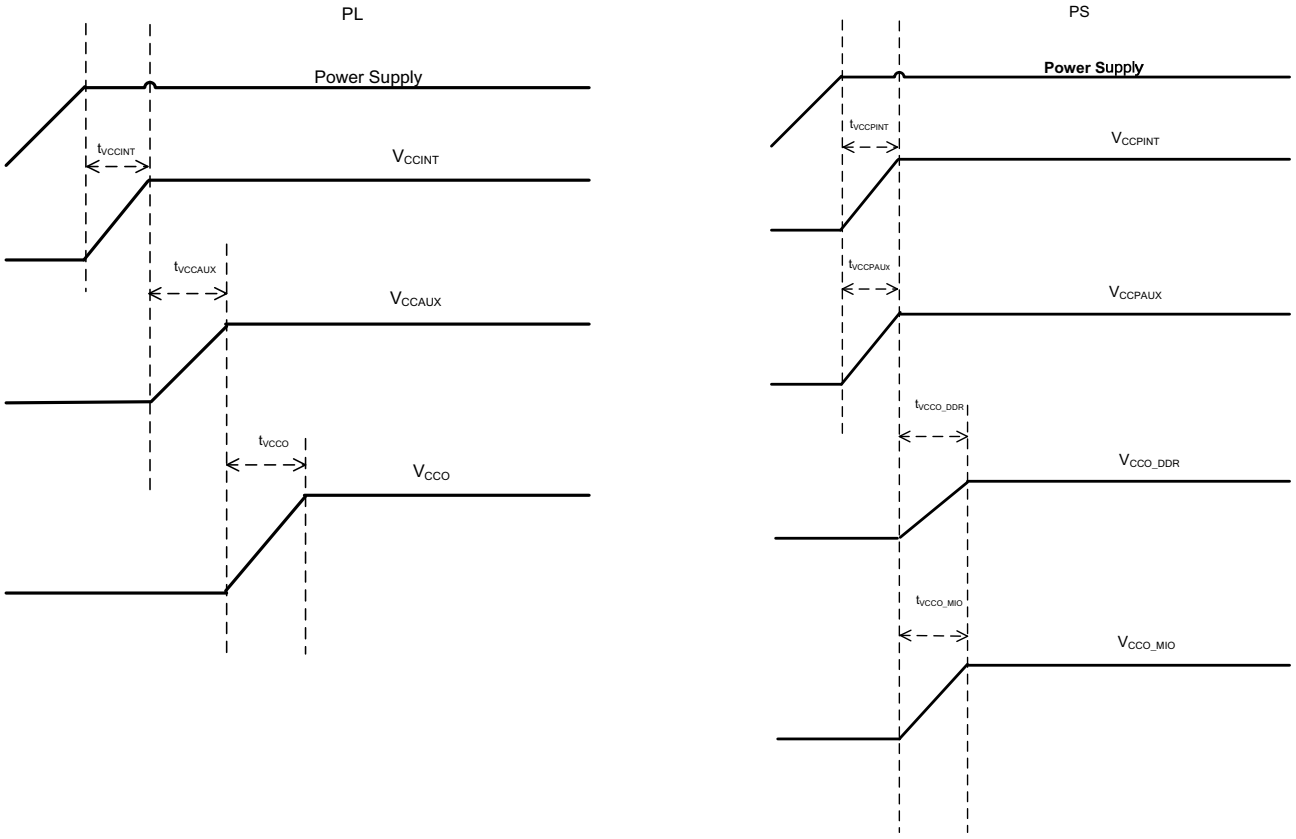

Figure 2. Ramp times

It is essential for the designer to keep in mind the voltage and current levels and accuracy, the power supply sequence, the ramp, and delay times, to ensure safe operation of the system.

4 MMPF0100

The PF0100 SMARTMOS Power Management Integrated Circuit (PMIC) provides a highly programmable/configurable architecture, with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, Real Time Clock (RTC) supply, and coin-cell charger, the PF0100 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications.

Features:

- Four to six buck converters, depending on configuration
  - Single/parallel options
  - DDR termination tracking mode option
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (One Time Programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- I^2C control
- Individually programmable ON, OFF, and Standby modes

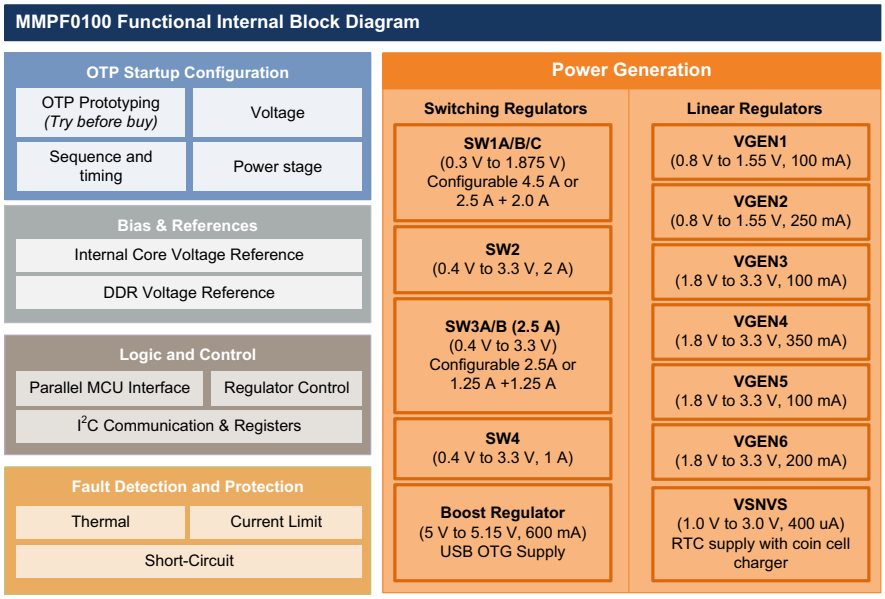

Figure 3. Functional internal block diagram of the MMPF0100

The number of available voltage options from the MMPF0100 PMIC at different currents enables it to provide to the different power needs of the ZedBoard. The buck regulators can be configured in four different modes, depending on the requirement. **Table 9** shows a configuration where the maximum number of rails are available, at reduced currents, whereas **Table 10** shows a configuration where only four rails are available but can support higher current demands.

Table 9. Six independent buck regulators

Regulator Name	Output Voltage Range	DC Current Load Capability
SW1AB	0.3 V to 1.875 V	2.5 A
SW1C	0.3 V to 1.875 V	2.0 A
SW2	0.4 V to 3.3 V	2.0 A
SW3A	0.4 V to 3.3 V	1.25 A
SW3B	0.4 V to 3.3 V	1.25 A
SW4	0.4 V to 3.3 V	1.0 A

Table 10. Four independent buck regulators

Regulator Name	Output Voltage Range	DC Current Load Capability
SW1ABC	0.3 V to 1.875 V	4.5 A
SW2	0.4 V to 3.3 V	2.0 A
SW3AB	0.4 V to 3.3 V	2.5 A
SW4	0.4 V to 3.3 V	1.0 A

SW1AB and SW1C may be combined independent of SW3A and SW3B and vice versa. This leads to two different configurations, with five regulators each, shown in **Table 11** and **Table 12**. The PF0100 used in this application is programmed according to the configuration shown in **Table 11**.

Table 11. Five independent buck regulators - option 1

Regulator Name	Output Voltage Range	DC Current Load Capability
SW1ABC	0.3 V to 1.875 V	4.5 A
SW2	0.4 V to 3.3 V	2.0 A
SW3A	0.4 V to 3.3 V	1.25 A
SW3B	0.4 V to 3.3 V	1.25 A
SW4	0.4 V to 3.3 V	1.0 A

Table 12. Five independent buck regulators - option 2

Regulator Name	Output Voltage Range	DC Current Load Capability
SW1AB	0.3 V to 1.875 V	2.5 A
SW1C	0.3 V to 1.875 V	2.0 A
SW2	0.4 V to 3.3 V	2.0 A
SW3AB	0.4 V to 3.3 V	2.5 A
SW4	0.4 V to 3.3 V	1.0 A

Of particular note are the One Time Programmable (OTP) mode and the Try Before Buy (TBB) mode. The OTP mode allows you to pre-program the default values for the PF0100 registers at start up. The TBB mode gives you the option of trying out various settings before the registers are actually written to with their values. The TBB mode is especially useful when the power system is being designed or there are modifications needed to an existing solution. You can also shift between Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM) and Auto Pulse Skip Mode (APS) for the buck regulators.

The Power Stage Control registers can be used to reduce the required inductor current limit when the regulators are not operating at their rated output currents, enabling use of smaller inductors. This provides a significant advantage to the PF0100 as there may be a number of applications where not all regulators are exercised to their current limits. Furthermore, the Dynamic Voltage Scaling (DVS) feature eliminates the need for a resistor divider network in the feedback loop of the buck regulators, thereby reducing the number of external components required.

5 Power solution for the ZedBoard

Before a power solution can be installed, it is important to have an estimate of the various voltage rails and the current drawn on each of them. Although the Zynq®-7000 SoC section provides a summary of the voltage domains necessary for proper operation of the Zynq® device, recommended settings allow—and in some cases, require—some of the voltages to be combined and powered by the same rail, whenever they are of the same voltage levels. Furthermore, there may be a need for multiple V_{CCO}, V_{CCO_MIO}, and V_{CCO_DDR} rails, depending on the voltage requirements of the peripherals. This highlights the need for doing a detailed analysis of the voltage level requirements for the case being implemented.

NXP recommends using the Xilinx Power Estimator (XPE) tool to arrive at an estimate for the particular case under consideration. Although this yields only an approximate estimate, it is usually accurate enough for the pre-synthesis phase and it provides the designer with a general idea of the current requirements. The Power Analyzer tool provides a more accurate estimate once the design is implemented. Furthermore, you can import data from the Power Analyzer tool to the XPE to compare with the pre-implementation analysis and to take corrective measures if necessary.

Designers should be aggressive in doing worst-case estimates while keeping in mind that over-designing may impact cost. The different use cases may vary significantly from the worst-case estimate.

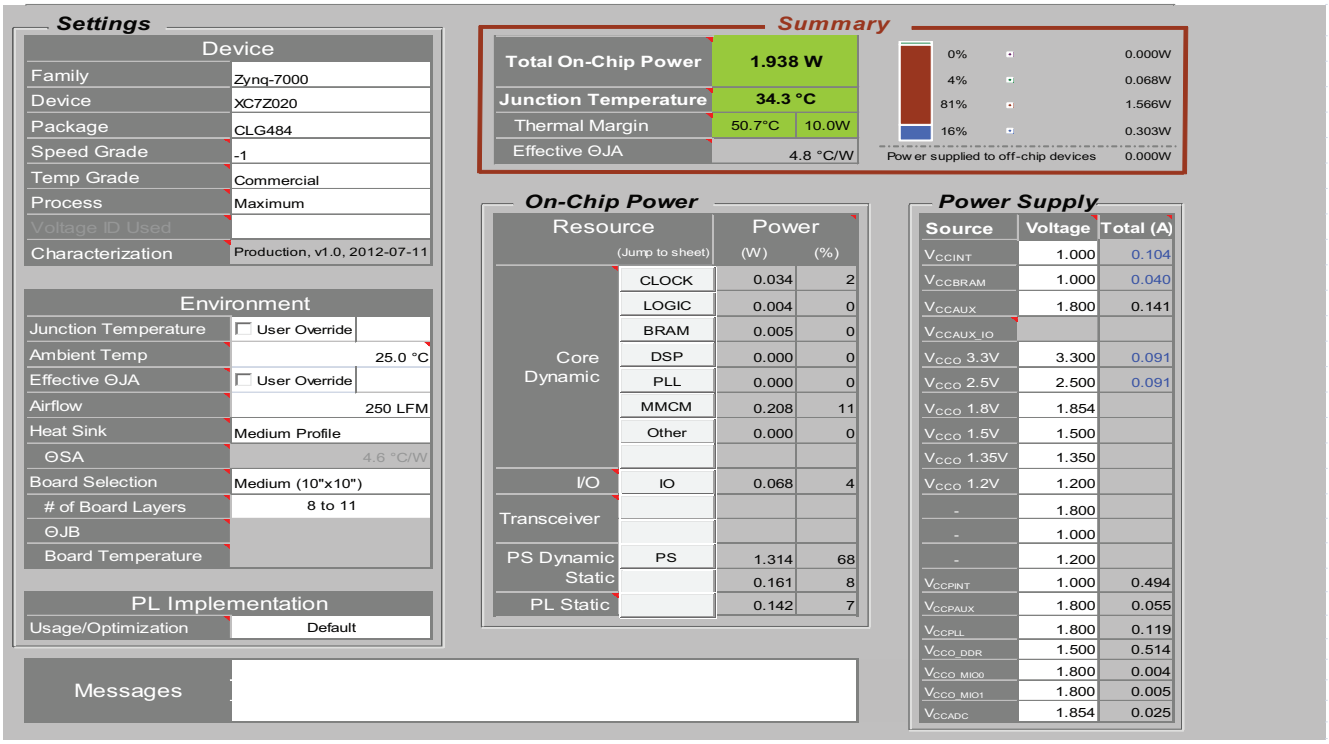

Figure 4. Power estimation data for use case 1

Figure 4 shows the power supply summary obtained from XPE for a particular use case implemented in the ZedBoard. It also involves the use of HDMI, I^2S audio, I^2C and GPIO pins, and runs PetaLinux OS from the SD card.

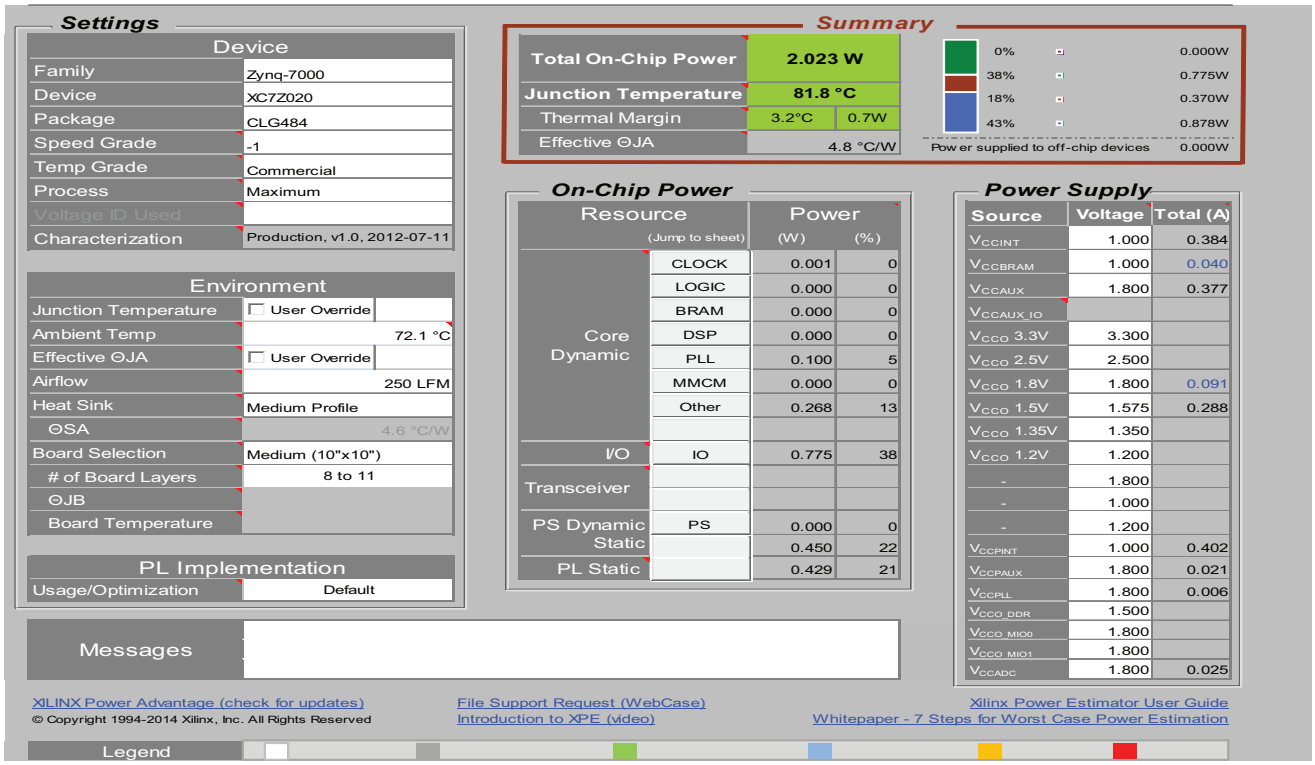

Figure 5. Power estimation data for use case 2

Figure 5 shows the power supply summary obtained from XPE for an use case that portrays the use of HDMI and DDR3 memory.

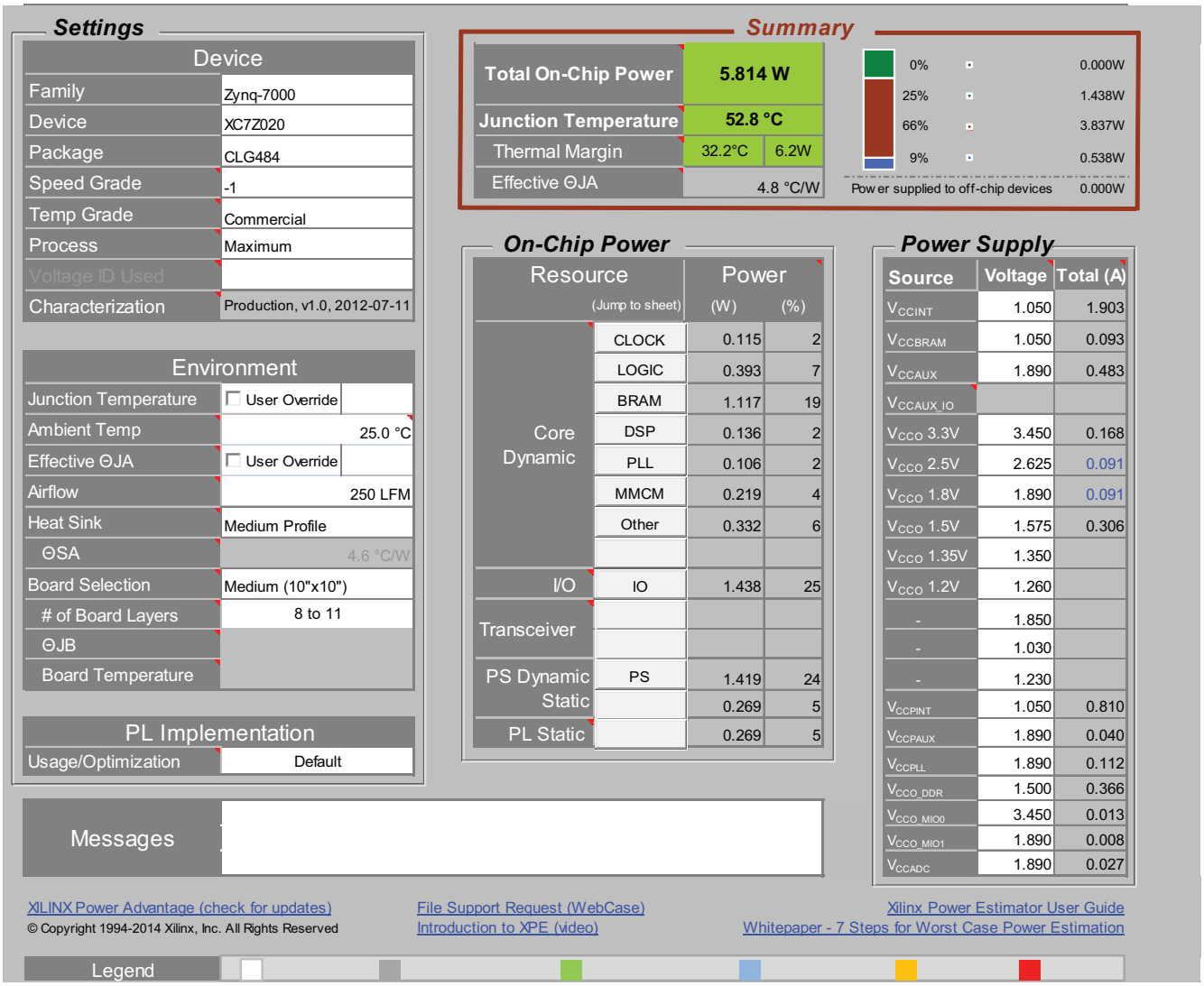

Figure 6. Worst-case estimate from XPE

Figure 6 shows the worst-case power estimates for the ZedBoard. The calculations are made using exaggerated activity rates and loads in order to account for unexpected user anomalies. Notice that the current capabilities of the PF0100 offer a satisfactory level of tolerance above this calculated limit.

Furthermore, some of the LDOs on the PF0100 are left unused and are available for other system uses.

While these cases show the PF0100's compatibility with the Zynq® XC7Z020 on the ZedBoard, you can also use them to power other platforms based on the Z-7020 or other Zynq® SoCs.

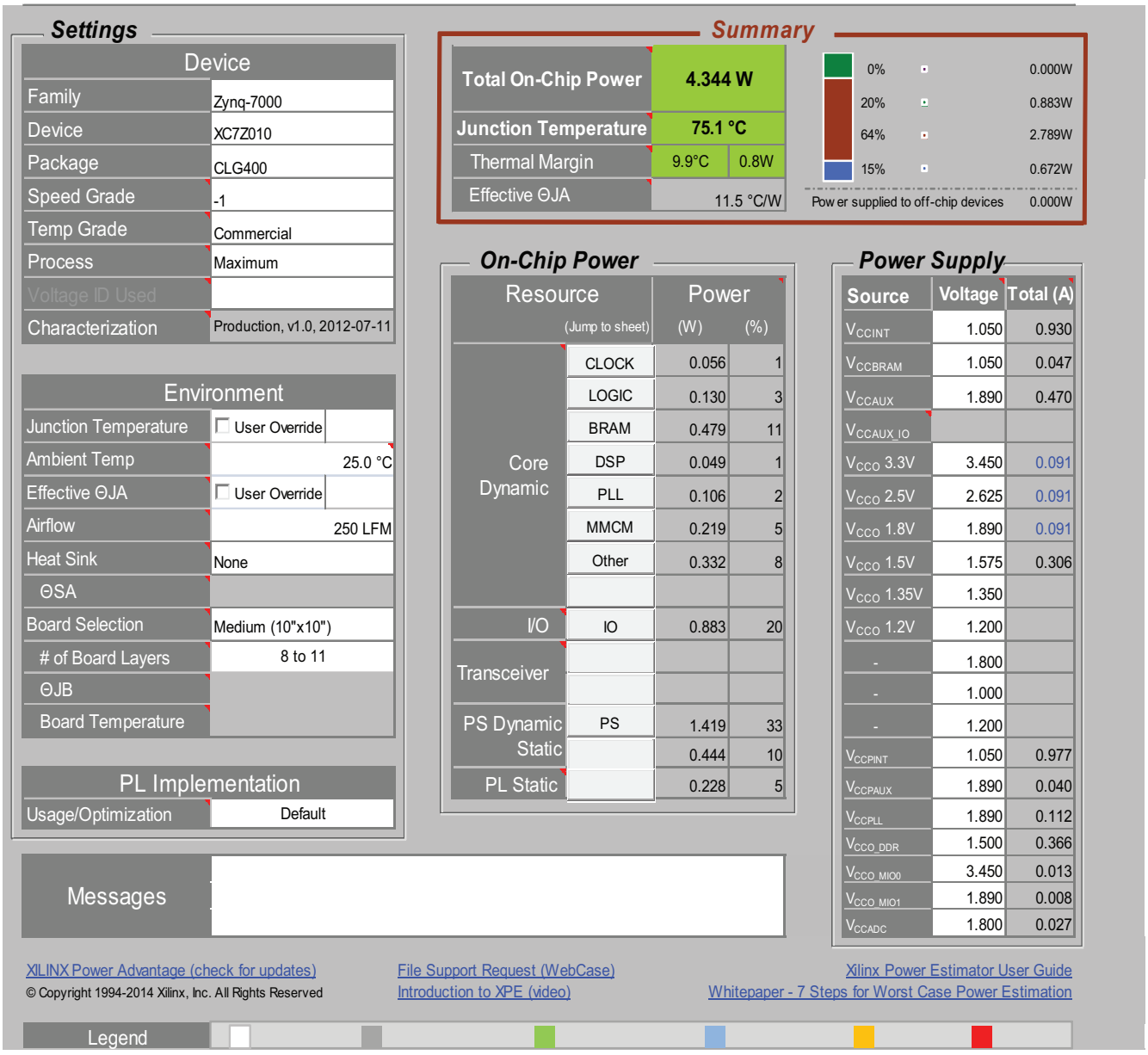

Figure 7. XPE estimate for Z-7010

The power demand of the Z-7010, presented by the estimate in **Figure 7**, is met by the PF0100.

5.1 Power tree design

The supply to the ZedBoard is from a 12 V barrel-jack connector. This is stepped down to 3.6 V in order to meet the input side supply requirement of the PF0100.

Following Xilinx recommendations:

- V_{CCINT} and V_{CCBRAM} should be connected to the same supply
- V_{CCPAUX}, V_{CCPLL} and the V_{CCO}, V_{CCO_MIO}, V_{CCO_DDR} rails which have the same voltages may be powered from the same rails
- V_{CCAUX} and V_{CCO} may be powered from the same rails if they have the same recommended voltages

Taking into account the recommendations and the ZedBoard needs, the required rails are:

- One 1 V rail for V_{CCPINT}, V_{CCINT} and V_{CCBRAM}
- One 1.8 V rail for V_{CCAUX}, V_{CCPAUX}, V_{CCPLL}, V_{CCBATT} and V_{CCO_MIO1} (supplies to USB-UART, USB-OTG, SD Card, Push buttons and Ethernet)
- One 3.3 V rail for V_{CCO} (supplies to JTAG, LEDs, OLED display, HDMI, VGA, Pmod and Audio codec) and V_{CCO_MIO0} (supplies to Pmod and QSPI)
- One adjustable 3.3/2.5/1.8 V rail for V_{CCO} (supplies to FMC, XADC, push buttons and switches)
- One 5 V rail for USB OTG, HDMI and audio codec
- One 1.5 V rail for V_{CCO_DDR}
- One 0.75 V rail for V_{TT_DDR} (DDR3 termination voltage)
- One 1.8 V rail for V_{CCADC}
- One 1.25 V rail for V_{REFP} (low current, high accuracy)

The ZedBoard power requirements and the corresponding supplies are summarized in **Table 13**.

Table 13. Power requirements for ZedBoard

Rail	Voltage level	Current drawn	Supply
V_{CCINT}	1.0 V	4.5 A	SW1ABC (PF0100)
V_{CCAUX}	1.8 V	1.0 A	SW3B (PF0100)
V_{CCO1}	3.3 V	3.0 A	MC34713
V_{CCO2}	3.3/2.5/1.8 V	2.0 A	SW2 (PF0100)
V_{CC5V0}	5.0 V	0.6 A	SWBST (PF0100)
V_{CCO_DDR}	1.5 V	1.0 A	SW3A (PF0100)
V_{TT_DDR}	0.75 V	1.0 A	SW4 (PF0100)
V_{CCADC}	1.8 V	0.1 A	VGEN4 (PF0100)
V_{REFP}	1.25 V	0.005 A	Reference generator

The buck regulators in the PF0100 may be configured as five independent regulators to power V_{CCINT}, V_{CCAUX}, V_{CCO2}, V_{CCO_DDR} and V_{TT_DDR} rails. The PF0100 VTT tracking mode is software enabled. This allows the V_{TT_DDR} rail to automatically track half of V_{CCO_DDR} if they are connected to SW4 and SW3A respectively. VGEN4 may be used to power V_{CCADC}. The boost regulator in the PF0100 is utilized to supply the V_{CC5V0} rail.

The V_{CCO1} rail requires a buck converter to convert the available 3.6 V to 3.3 V, while being capable of supplying 3 A. Because most peripherals are supplied through this rail, the current being drawn may vary. Therefore, to ensure safe operation, both this rail and the V_{CCINT} rail are provided with sufficient margins. The NXP Switched-mode Power Supply (SMPS) MC34713 provides a good option for achieving this. The MC34713 is a highly integrated, space efficient, low cost, single synchronous buck switching regulator with integrated N-channel power MOSFETs. It is a high performance point-of-load (PoL) power supply with the ability to track an external reference voltage in different configurations. Its high-efficient 5.0 A continuous output current capability combined with its voltage tracking/sequencing ability and tight output regulation, makes it ideal as a single power supply. The Shutdown pin on the MC34713 is controlled to ensure that the supply from this rail is compatible with the sequence constraints.

The power-off sequence is enforced by software. PF0100 can be communicated to via I2C. Appropriate register settings are sent over I2C so that the rails are turned off in the recommended sequence.

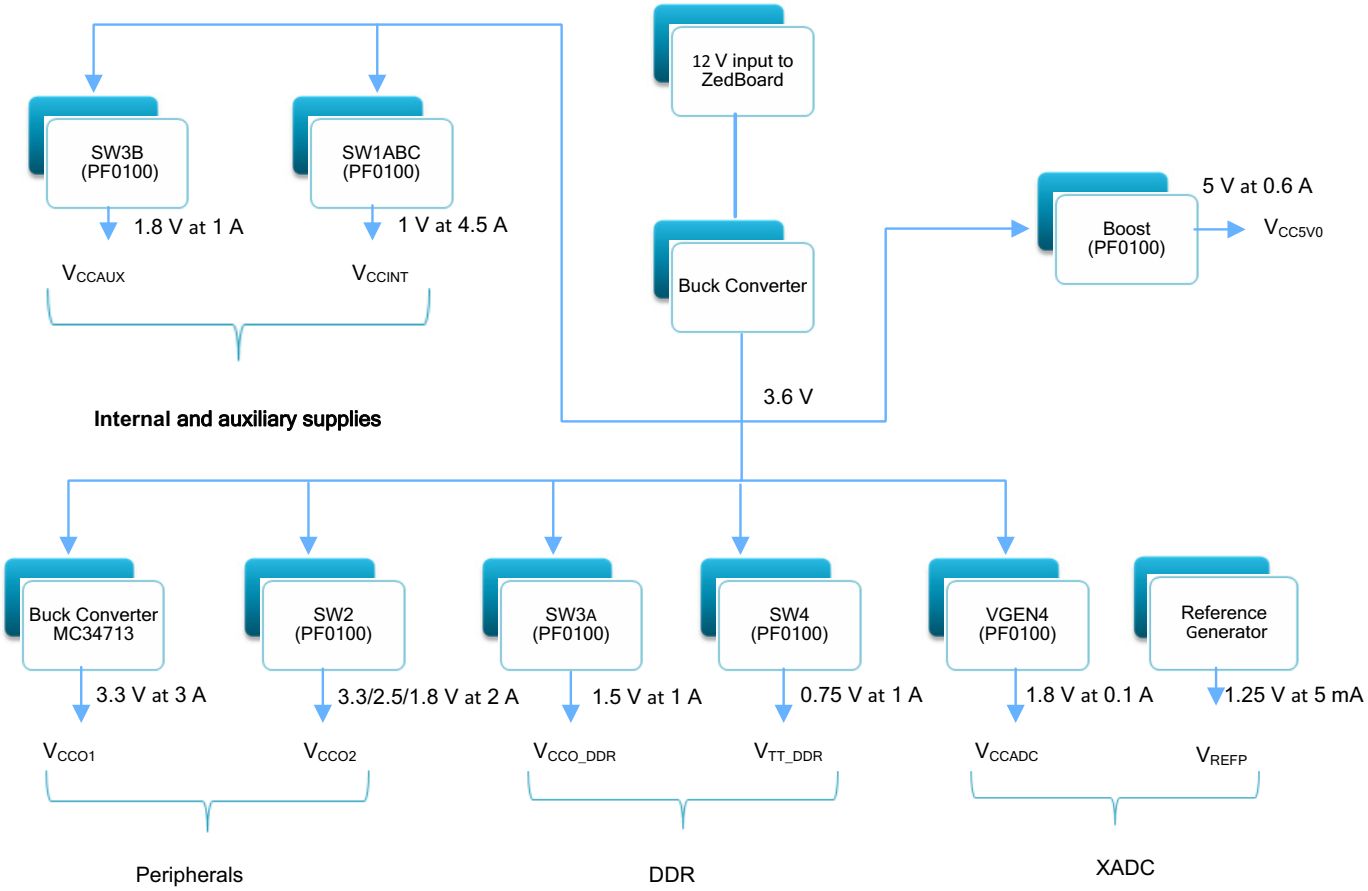

Figure 8. Power tree

The ZedBoard's power tree is represented in **Figure 8**.

5.2 PF0100 interface with Zynq®

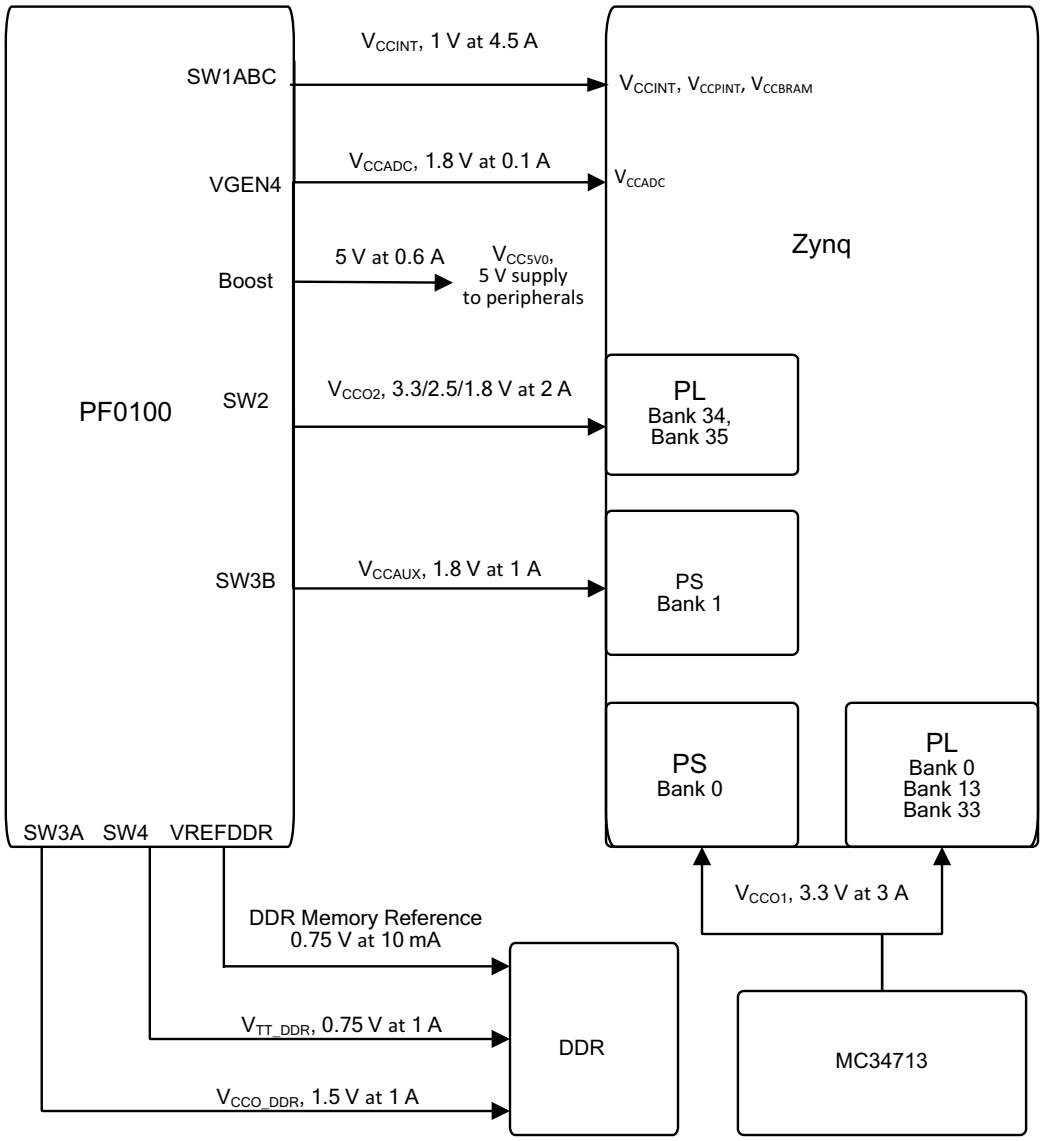

Figure 9. Zynq® power bank assignments

Figure 9 demonstrates the power bank assignments and the interface connections from the PF0100 to the XC7Z010-CLG484-1 IC on the ZedBoard.

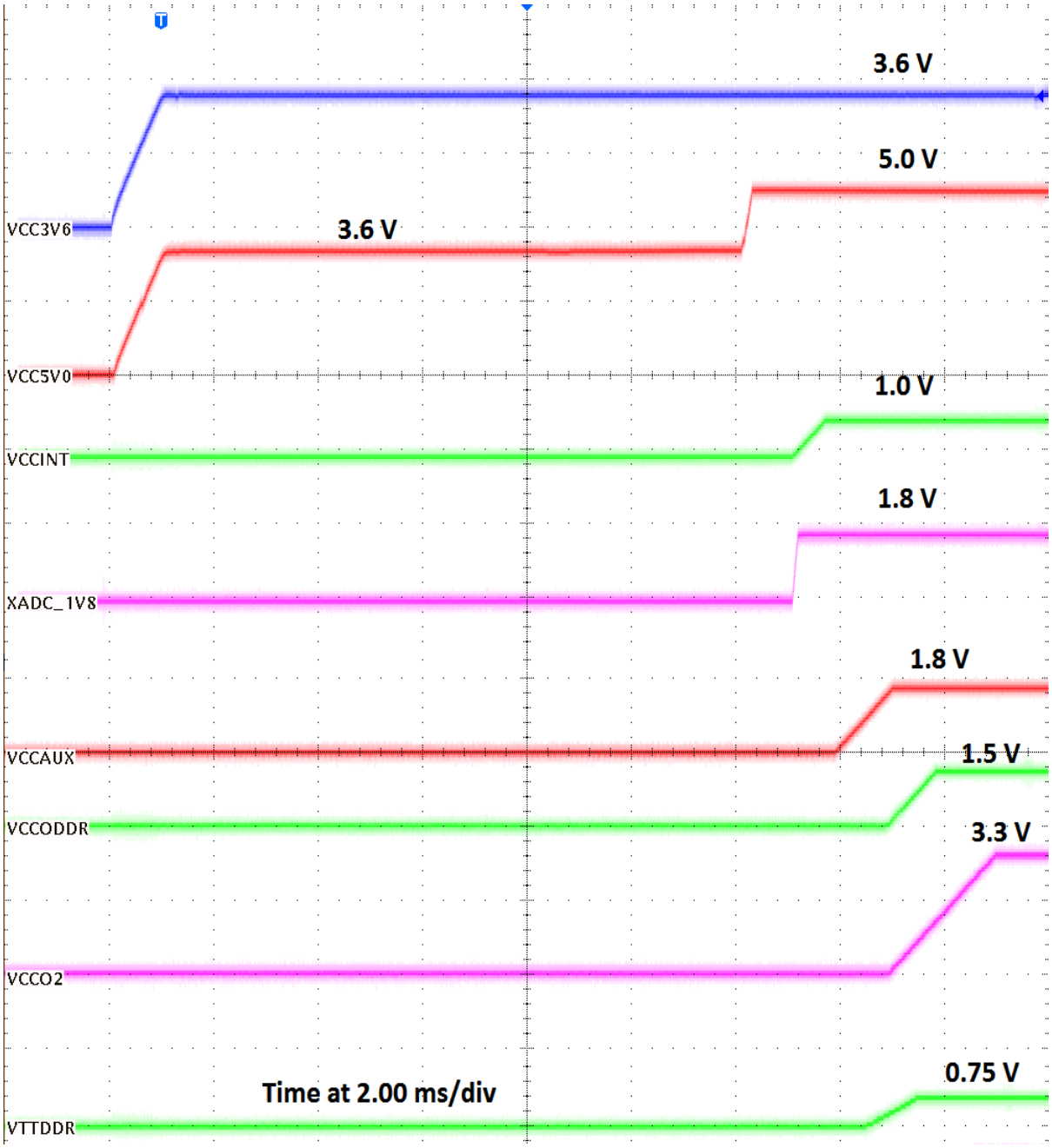

Figure 10. Power rails generated using the PF0100

Figure 10 shows the PF0100 used to supply the seven power rails required by the on-board Zynq® processor. To control ramp times, modify the DVS settings in the PF0100. A DVS setting of 3.125 mv/usec and a sequencer setting of 1.00 ms ensures that the start-up requirements are met. Using the PF0100's Power-OK output to control the MC34713's Shut-down mode input pin ensures that the V_{CCO1} signal powers up last in the sequence. Because V_{CCO1} is a peripheral rail, this complies with the power-on recommendations for the Zynq®-7020. Furthermore, the PF0100 settings, including output voltages, start-up sequences, frequency, and switching mode (PWM, APS, PFM), are completely configurable on-the-fly using I^2C. **Table 14** illustrates the ramp time and sequence configurations from the demonstration board.

Table 14. Ramp timing and sequence settings of individual rails on the hardware board

Voltage rail	Sequence position	Rise time - GND to 90% (in ms)
V_{CC3V6}	0	0.834
V_{CC5V0} [(4)(5)]	1	0.103
V_{CCINT}	2	0.258
V_{CCADC}	3	0.225
V_{CCAUX}	4	0.685
V_{CCODDR}	4	0.539
V_{TT_DDR}	4	0.616
V_{CC02}	4	1.434
V_{CC01}	5	2.710

4. Because the 5 V rail supplies peripherals like USB-OTG and does not directly impact the operation of Zynq®, it is powered on before other rails
5. The ramp time for the 5 V rail is measured from 3.6V to 90% and not from GND to 90%

5.3 Schematics

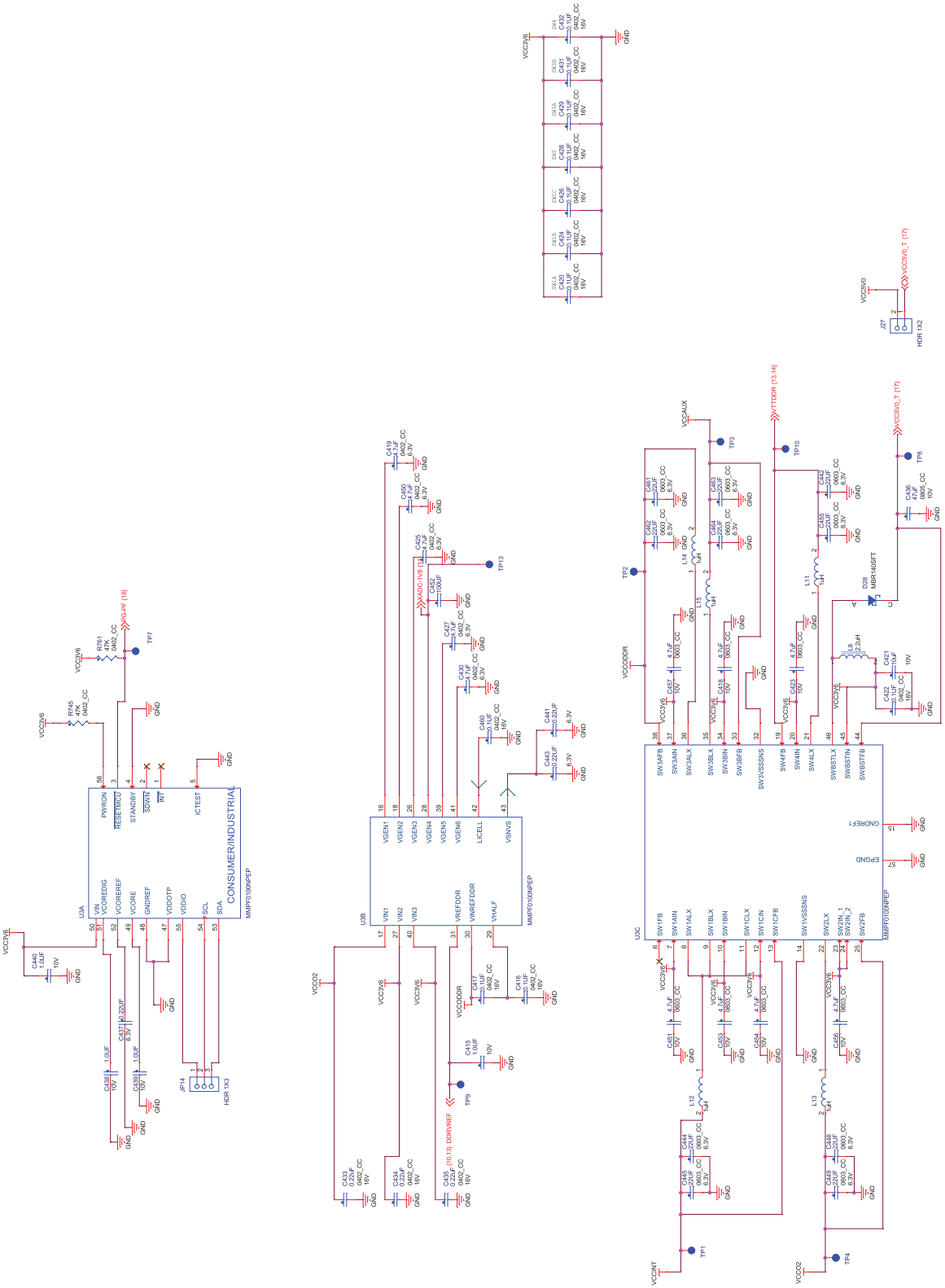

Figure 11. MMPF0100

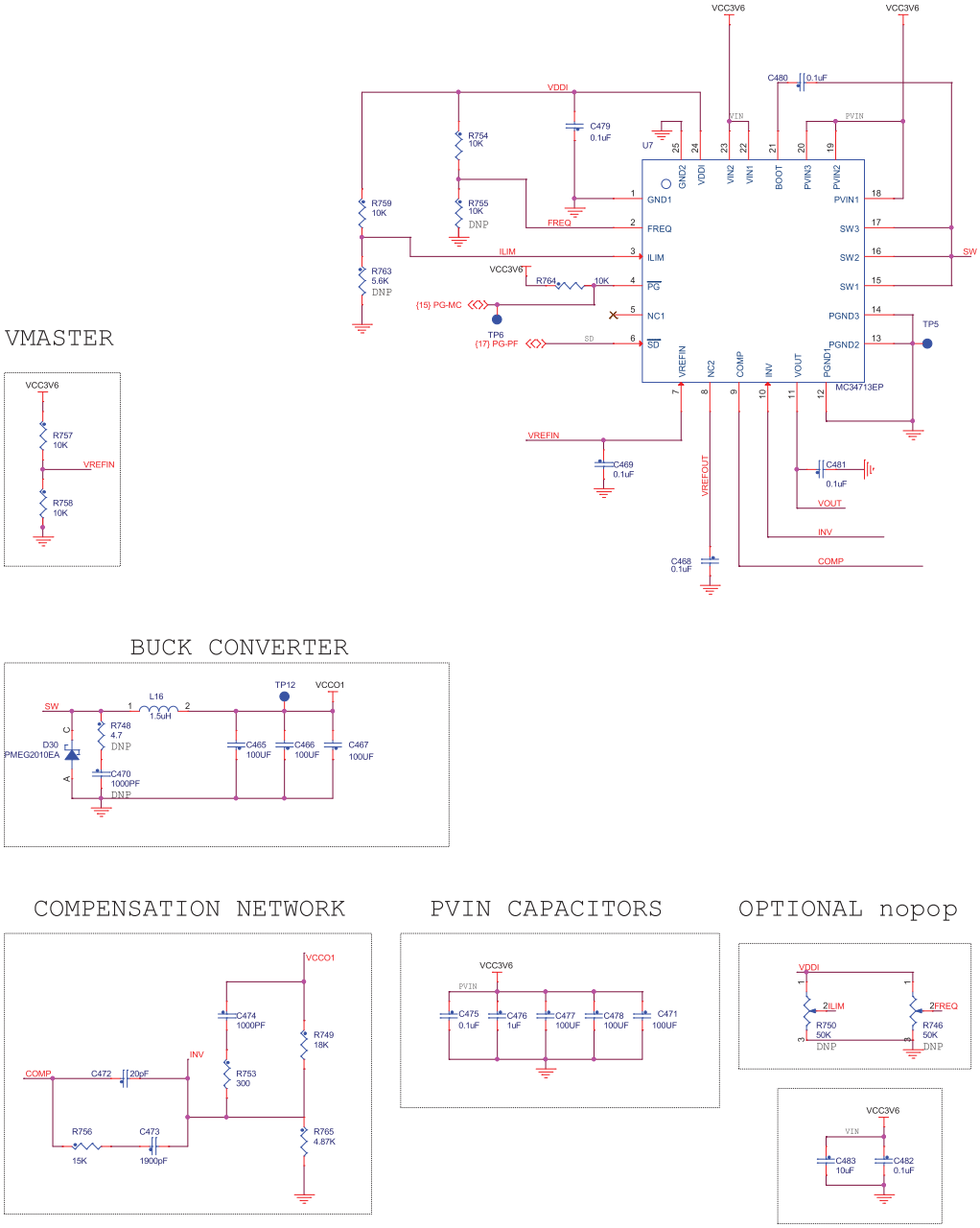

Figure 12. MC34713

NOTE

For full schematics and layout, please contact an NXP representative.

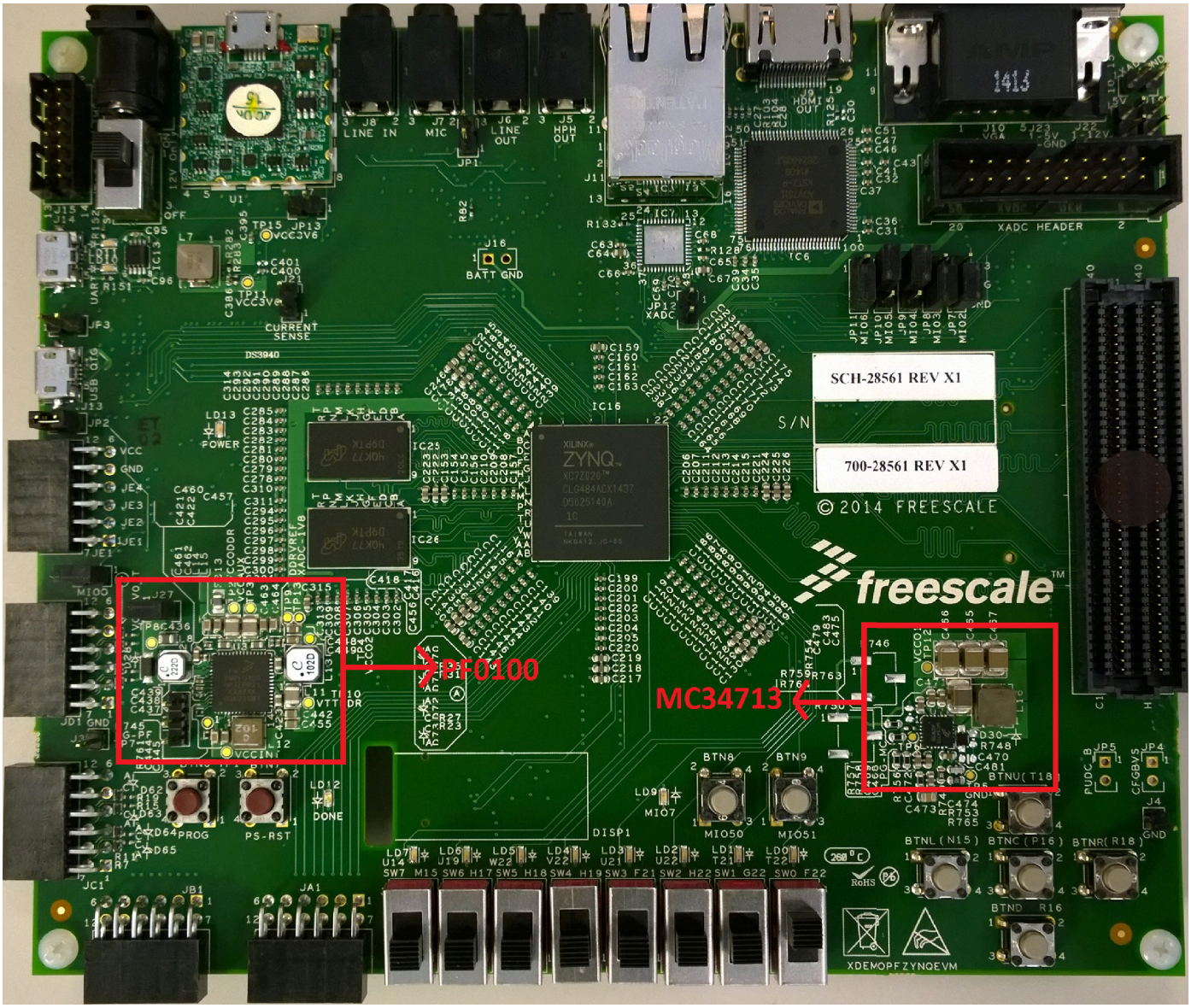

Figure 13. Zynq®-7020 board powered by PF0100

6 Conclusion

This Application Note offers an example of an optimal power management solution using the Xilinx ZedBoard development board in conjunction with the NXP's PF0100 Power Management IC (PMIC).The PF0100 PMIC is an ideal candidate for the power management of Xilinx Zynq® AP SoCs, particularly when used with the ZedBoard. The solution discussed in this document may be tweaked to provide a power solution for other systems based on Zynq® devices. Some distinct advantages of using the PF0100 are:

- The PF0100 PMIC-based power solution discussed above results in a design that uses a low number of discrete components. This offers the possibility of an overall reduction in silicon real-estate and a corresponding reduction in cost.
- The start-up sequence and output voltages can be enforced using software rather than passive components or other external circuitry. This ensures more accurate control
- Enforcing the Power Stage Control and DVS ensures a reduction in the inductor current limits and sizes, and improves efficiency and stability
- The PF0100 has a built-in VTT tracking mode which eliminates the need for an external DDR voltage termination component
- The VREFDDR option in the PF0100 may be utilized for DDR3 reference voltage
- The unused LDOs in the PF0100 are available for other user demands

7 References

Following are URLs where you can obtain information on related NXP products and application solutions:

Support Pages	Description	URL
MMPF0100	Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MMPF0100.pdf
MC34713	Data Sheet	www.nxp.com/files/analog/doc/data_sheet/MC34713.pdf
MMPF0100	Product Summary Page	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100
	Analog Home Page	http://www.nxp.com/analog
	Xilinx Home Page	http://www.xilinx.com

7.1 Support

Visit www.nxp.com/support for a list of phone numbers within your region.

7.2 Warranty

Visit www.nxp.com/warranty for a list of phone numbers within your region.

8 Revision History

Revision	Date	Description
1.0	9/2014	• Initial release
2.0	3/2015	• Updated with results from hardware board
	7/2016	• Updated to NXP document form and style

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