Freescale Semiconductor
APPLICATION NOTE

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Achieving Lowest Power Consumption with MMA8491Q Accelerometer/Tilt Sensor

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1 Introduction

The MMA8491Q 3-Axis Digital Accelerometer enables the lowest power consumption for low data rate accelerometer applications by providing a unique single sample method with a 1.8 nA low power state between samples. In order to achieve the lowest power, the recommended system configuration utilizes the single sample method and a simple 45 degree tilt sensing output on the device. This method achieves benchmark current consumption by not only reducing the current consumption of the sensor itself, but also by operating the host micro-controller in lowest possible duty cycle through the sensor's digital output pins.

This document describes the recommended low power method of operation of the sensor for low data rate applications by contrasting the tilt sensing and I^2C methods. The impact of each on power consumption is also demonstrated by providing operational details and bench test results.

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2 Recommended Implementation

MMA8491Q can basically accommodate two accelerometer configurations.

Tilt sensing configuration

As a 45° tilt sensor, MMA8491Q offers a single line output (of type logical) per axis through the XOUT, YOUT and ZOUT pins. These pins are asserted whenever the tilt angle in the respective axis is greater than 45°. For detailed information on the tilt sensing flow, refer to Freescale application note AN4296.

Digital output accelerometer configuration

As a digital output accelerometer, the 14-bit accelerometer data can be read via I^2C communication interface at the end of T_{ON} period. T_{ON} is the Active stage of the device at the end of which, newly acquired sample data is available. For more information on operation states, refer the Freescale data sheet MMA8491Q.

Note: The device should be in active state when the data is being polled (EN pin must be high). For detailed information on this configuration via the I^2C protocol refer to Freescale application note AN4296.

To achieve the lowest power consumption it is recommended to use the part in tilt sensing configuration as the digital output configuration is slightly more expensive in terms of power budget due to the overhead of I^2C communications and continuous polling for data between the host and the device.

3 Power-Up Timing Sequences

The operartional states of MMA8491Q during the acquisition of a single sample are shown in the timing sequence (Figure 1). V_{DD} is powered on and then the EN pin is activated to acquire a single sample. Additional samples can be acquired by deasserting the EN pin and reasserting it again repeatedly.

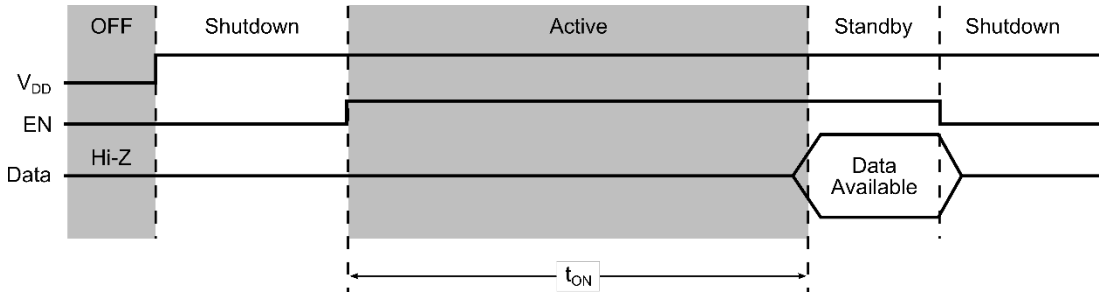

Figure 1. Timing sequence

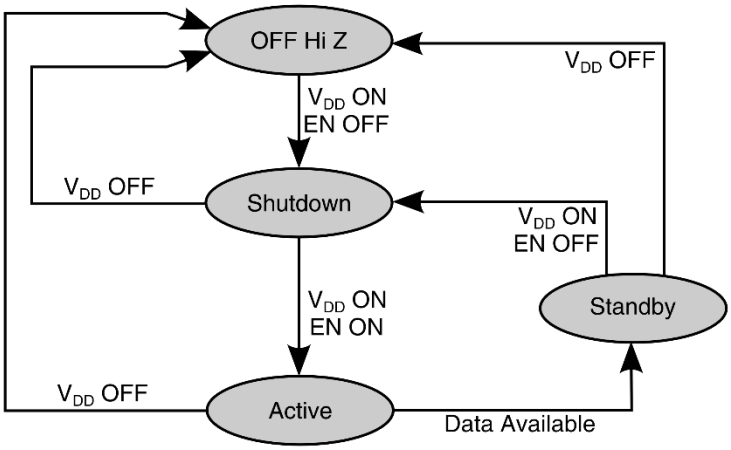

Figure 2. Transitional state diagram

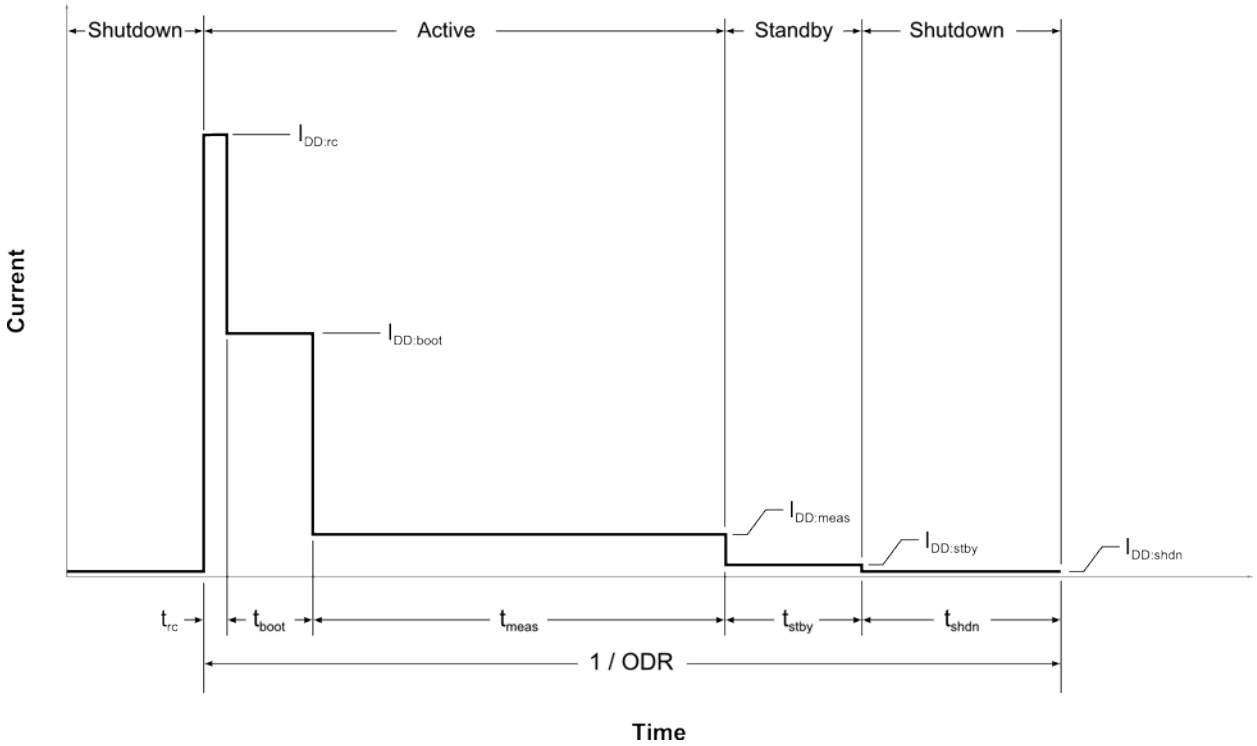

Figure 3. Current consumption profile

Figure 3 shows the I_{DD} profile of the device during a single measurement cycle. The current consumption in each mode of this cycle is discussed below and also identified in Table 1.

ACTIVE State

The current in ACTIVE state goes through three phases: regulator charge (rc), boot, and measurement (meas).

1. $I_{DD:rc}$ begins when the EN pin reaches 1.95 V, the point at which the device's internal voltage regulator begins to charge the external bypass capacitor.
2. As the bypass capacitor finishes charging, the current stabilizes to $I_{DD:boot}$.

3. After the boot process is complete, the current then drops to $I_{DD:meas}$ as the accelerometer takes a sample and processes it.

The duration of each current phase, t_{rc}, t_{boot} and t_{meas}, is internally controlled by the device.

STANDBY State

The current in this state ($I_{DD:stby}$) is mainly consumed by the digital circuitry, which makes the data outputs available. The length of this stage t_{stby} is controlled by users by deasserting the EN pin to exit this mode.

SHUTDOWN State

The current in this state ($I_{DD:shdn}$) is the IC leakage current, after the EN pin is pulled LOW. The device consumes almost no power in this state. Users also control the length of this state (t_{shdn}). It is recommended to leave the device in this mode until it is time to take the next sample. This extremely low power state enables users to achieve a low average power consumption for low data rate applications.

Table 1. Typical current consumption parameters

State	Average current		Duration	
	Symbol	Typical (µA)	Symbol	Typical (s)
ACTIVE state				
Regulator charge	$I_{DD:rc}$	3272	t_{rc}	20 x 10^{-6}
Boot-up	$I_{DD:boot}$	3109	t_{boot}	20 x 10^{-6}
Measurement	$I_{DD:meas}$	398	t_{meas}	668 x 10^{-6}
STANDBY state1	$I_{DD:stby}$	1.8	t_{stby}	User-defined
SHUTDOWN state	$I_{DD:shdn}$	0.0018	$t_{shdn} = \left(\frac{1}{ODR}\right) - (t_{rc} + t_{boot} + t_{meas} + t_{stby})$	Depends on ODR and t_{stby}

1. For the experiments and results provided in this document, if I²C communication is used in this phase instead of the logical output pins, then average current $I_{DD:I2C}$ is taken to be 180 µA (for pull up resistor values of 10 kΩ in SDA and SDL lines) and time duration to be t_{I2C}, which will depend upon the I²C communication settings (SCL clock frequency).

4 Theoretical Model for I_{DD} Calculating

When using the device as a tilt sensor, calculate the average I_{DD} using the following equation:

$$Average\ I_{DD}(in\ \mu A) = ODR\left(I_{DD:rc}t_{rc} + I_{DD:boot}t_{boot} + I_{DD:meas}t_{meas} + I_{DD:stby}t_{stby} + I_{DD:shdn}t_{shdn}\right) \quad \textbf{(1)}$$

Substituting the typical values from Table 1 results in equation **(2)**.

$$Average\ I_{DD}\ (\mu A) = ODR\left(0.3934 + 1.8\,t_{stby} + 0.0018\left(\left(\frac{1}{ODR}\right) - 0.000708 - t_{stby}\right)\right) \quad \textbf{(2)}$$

When using the device as a digital accelerometer, calculate the average I_{DD} using the following equation:

$$Average\ I_{DD}(in\ \mu A) = ODR(\ I_{DD:rc}t_{rc} + I_{DD:boot}t_{boot} + I_{DD:meas}t_{meas} + I_{DD:I2C}t_{I2C} + \ I_{DD:shdn}t_{shdn}) \quad \textbf{(3)}$$

Substituting the typical values from Table 1 results in equation **(4)**.

$$Average\ I_{DD}\ (\mu A) = ODR\left(\ 0.3934 + 180\ t_{I2C} + 0.0018\left(\left(\frac{1}{ODR}\right) - 0.000708 - t_{I2C}\right)\right) \quad \textbf{(4)}$$

I²C Time Calculations

In order to evaluate t_{I2C}, first observe the I²C protocol diagram shown in Figure 4.

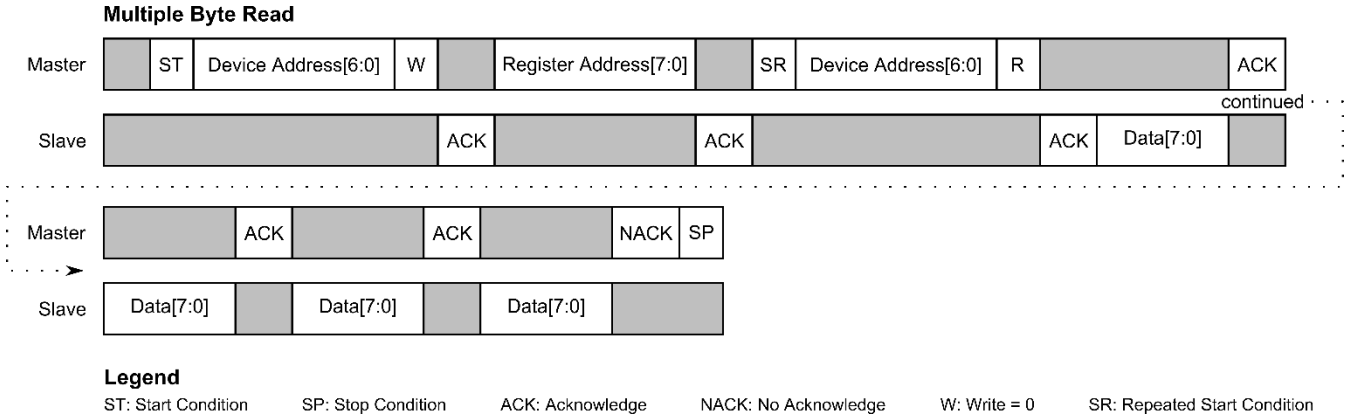

Figure 4. I²C protocol diagram (multiple byte read)

From Figure 4, the total number of clock cycles required to read eight consecutive data bytes is 93 clock cycles (93 bits).

So for a SCL clock frequency of about 375 kHz, (1 clock cycle = 2.66 µs), the above byte sequence will take about 248 µs ($93\ \text{bits} \times 2.66\ \mu\text{s/bit}$).

5 Bench Test Results

5.1 Typical Case

Figure 5 shows the typical current consumption profile of the part implemented in tilt sensing configuration with the typical application circuit as shown in the device datasheet.

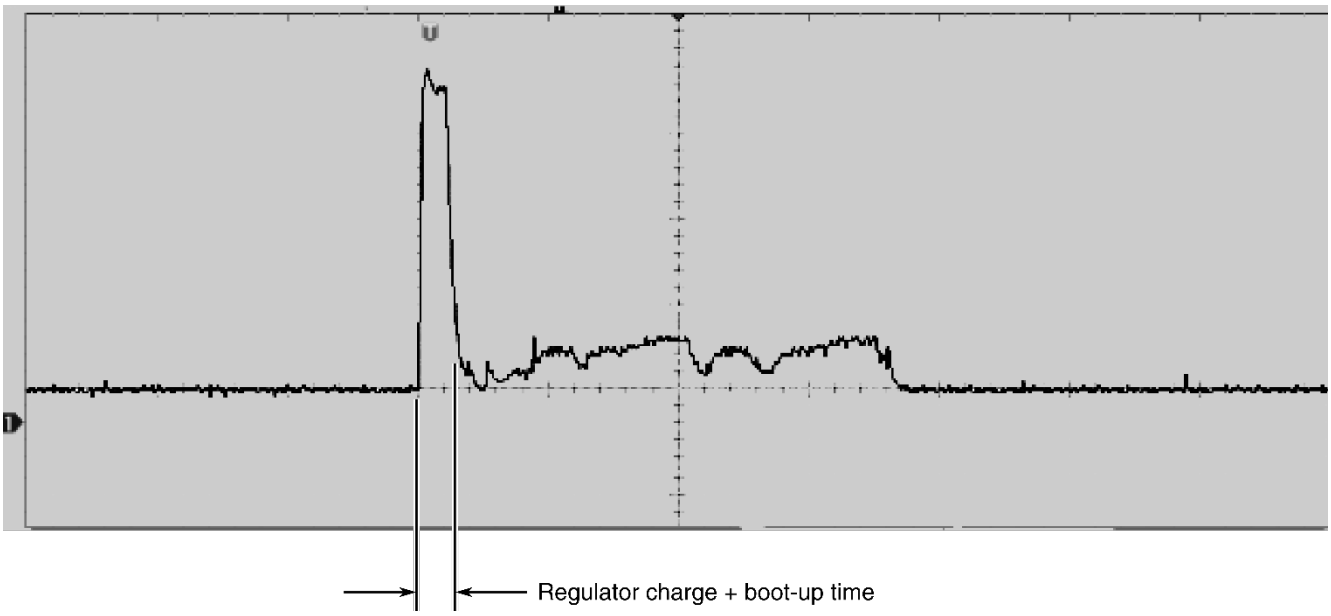

Figure 5. Typical current consumption profile

In this sample study, the standby time (t_{stby}) is 20 µs and ODR is taken to be 1 Hz.

When using the device as a tilt sensor, substituting these values into equation **(2)**, we get:

$$Average\ I_{DD}(in\ \mu A) = ODR\left(0.3934 + 1.8\,t_{stby} + 0.0018\left(\left(\frac{1}{ODR}\right) - 0.000708 - t_{stby}\right)\right) \quad \textbf{(5)}$$

$$= 1\left(0.3934 + 1.8(20 \times 10^{-6}) + 0.0018\left(\left(\frac{1}{1}\right) - 0.000708 - 20 \times 10^{-6}\right)\right)$$

$$\sim = 0.3952\ \mu A$$

Similarly, when using the device as a digital output accelerometer (using I²C), substituting the values into equation **(4)**, we get:

$$Average\ I_{DD}(in\ \mu A) = ODR\left(0.3934 + 180\,t_{I2C} + 0.0018\left(\left(\frac{1}{ODR}\right) - 0.000708 - t_{I2C}\right)\right) \quad \textbf{(6)}$$

$$= 1\left(0.3934 + 180(248 \times 10^{-6}) + 0.0018\left(\left(\frac{1}{1}\right) - 0.000708 - 248 \times 10^{-6}\right)\right)$$

$$\sim = 0.4398\ \mu A$$

5.2 Worst Case

Figure 6 shows the worst case current consumption profile when the part uses a 470 nF bypass capacitor instead of a typical 100 nF capacitor (as the typical application circuit in the device datasheet shows).

Note: Only the regulator charge and boot times are significantly increased by 100 µs each, whereas the measurement time remains fixed.

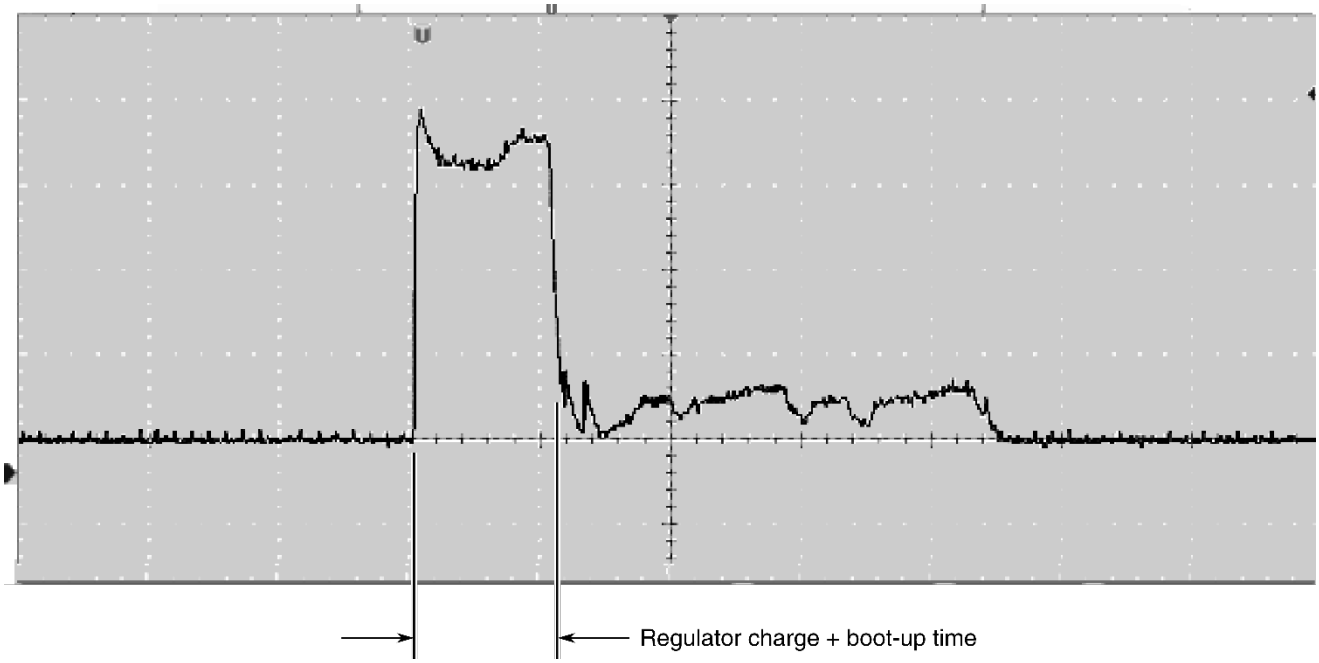

Figure 6. Worst case current consumption

When using the device as a tilt sensor, substituting these values into equation**(2)**, we get,

$$Average\ I_{DD} = ODR\left(1.0315 + 1.8\,t_{stby} + 0.0018\left(\left(\frac{1}{ODR}\right) - 0.000908 - t_{stby}\right)\right) \quad \textbf{(7)}$$

$$= 1\left(1.0315 + 1.8(20 \times 10^{-6}) + 0.0018\left(\left(\frac{1}{1}\right) - 0.000908 - 20 \times 10^{-6}\right)\right)$$

$$\sim = 1.0333\ \mu A$$

Similarly, when using the device as a digital output accelerometer (using I²C), substituting the values into equation **(4)**, we get:

$$Average\ I_{DD}(in\ \mu A) = ODR\left(1.0315 + 180\,t_{I2C} + 0.0018\left(\left(\frac{1}{ODR}\right) - 0.000908 - t_{I2C}\right)\right) \quad \textbf{(8)}$$

$$= 1\left(1.0315 + 180(248 \times 10^{-6}) + 0.0018\left(\left(\frac{1}{1}\right) - 0.000908 - 248 \times 10^{-6}\right)\right)$$

$$\sim = 1.0779\ \mu A$$

5.3 Summary

Figure 7 shows the average I_{DD} (in µA). From the figure, operating the device in tilt sensing configuration achieves the lowest power consumption for low data rate applications.

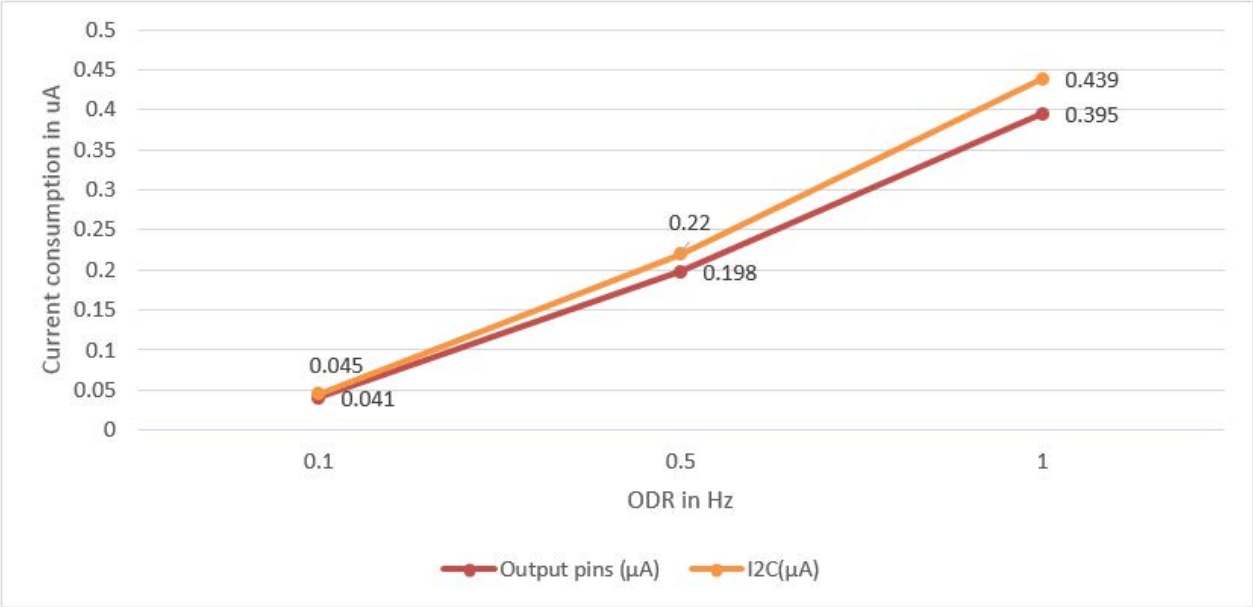

Figure 7. Current consumption vs. ODR for the two configurations

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