

# MVR5510AMMANES – NXP Standard

## Configuration report for QM OTP program ID: AN rev C

Rev. 1.0 - Feb 9 2022

Report

### 1 General description

The VR5510 is an automotive multi-output power management integrated circuit, with focus on Gateway, V2X and Infotainment applications. It includes multiple high efficiency switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The VR5510 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASILB and ASILD safety integrity level. It is developed in compliance with ISO 26262 standard.

### 2 Features and benefits

- 60V DC maximum input voltage
- Configurable VPRE synchronous buck controller with external MOSFETs.
- Configurable Single/dual-Phase Low voltage buck converters with DVS capability
- Configurable Low voltage integrated synchronous BUCK3 converter
- BOOST converter with integrated low side switch
- 3x linear voltage regulators with configurable Output Voltage
- High voltage linear regulator (HVLDO) with LDO and Switch mode operation
- EMC optimization with frequency tuning, clock synchronization, frequency spread spectrum and slew rate control
- Low power standby mode (40uA quiescent Current)
- 2x input pins for wake-up detection and battery voltage sense
- Device control via I2C interface with CRC (up to 3.4 MHz)
- Selectable OTP Default configuration

### 3 Applications

- Automotive Infotainment
- High - End Industrial

### 4 Ordering information

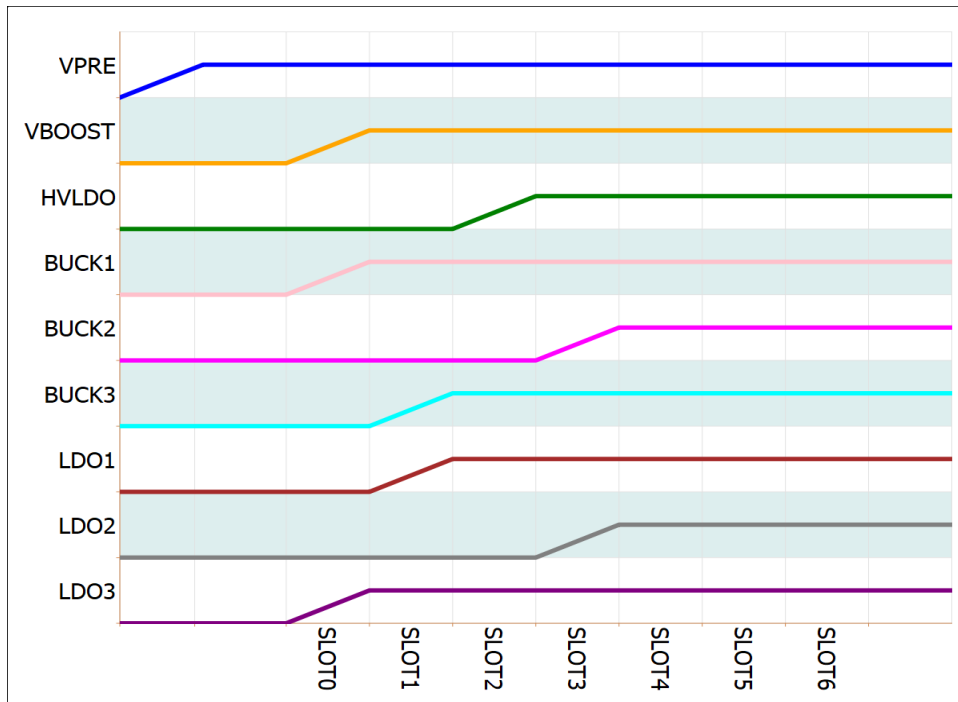
Table 1. Ordering information

Type number <sup>[1]</sup>	Package		
	Name	Description	Version
MVR5510AMMANES	QFN56 EP	QFN56 plastic thermally enhanced very thin quad flat non-leaded package. Wettable flanks; 56 terminals; 0.5mm pitch, 8mmx8mmx0.85mm body	SOT684-21

[1] To order parts in tape and reel, add the R2 suffix to the part number.

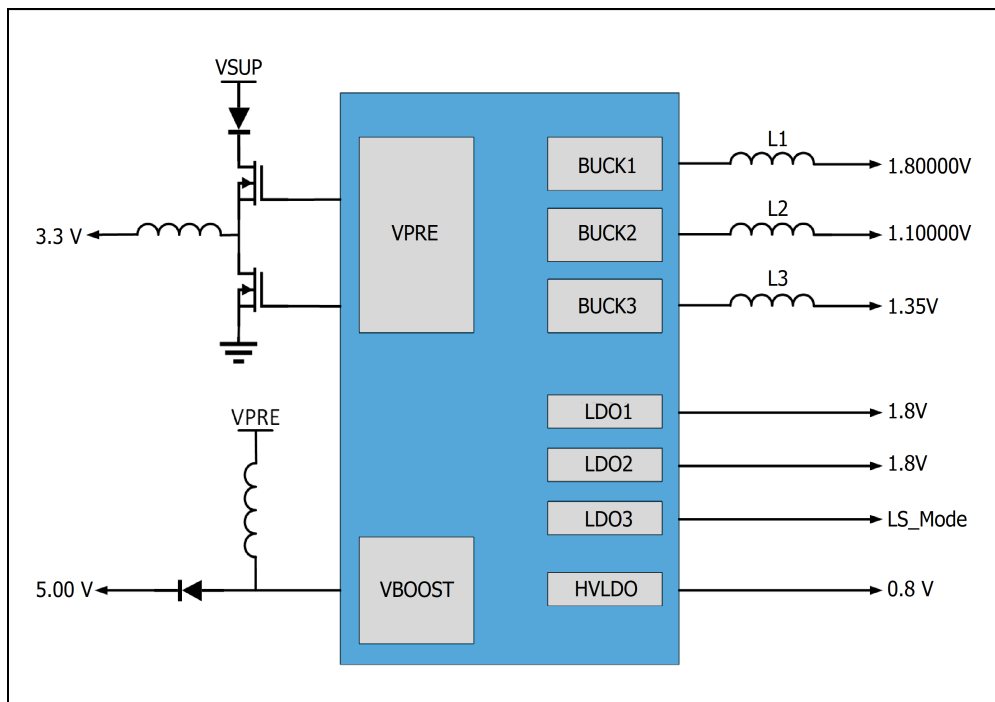


## 5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage

## 6 Hardware configuration diagram



## 7 System configuration

See VR5510 datasheet for parametric details. The OTP configuration summary for AN sequence ID is provided in Tables below.

**Table 2. Device OTP configuration**

Functional block	Feature	OTP selection
Device Configuration	Main I2C Address	0x20
	VSUP UV threshold	4.9V
	Auto Re-try Enable	Enabled (default)
	Auto Re-try Timeout	4 s (default)
	Number of Retries	Infinite Retry (default)
	PLL Enable	Disabled (default)
	Clock 1 Divider	2.22 MHz (default)
	Clock 2 Divider	455 KHz (default)
	Thermal Warning TH	105 $\mu$ C (default)
	Deep Sleep Enable	DSM Disabled (default)
IO Configuration	PWRON2 Control	Not Required
	AMUX/FOUT Select	AMUX Enabled (default)
	PSYNC Enable	PSYNC Disabled (default)
	PSYNC Mode	Sync VR5510 + LV PMIC
	PSYNC Power Down Ctrl	Ignore for PwrDown
	Standby Transition Timer	Enabled (default)
	Standby Discharge TH	75 mV (default)
	Standby Polarity	Active Low (default)
	Standby PGOOD Enable	Enabled (default)
	PSYNC PGOOD Ext	Enabled

## Configuration report for QM OTP program ID: AN rev C

	Ext Standby Discharge	Enabled
	Standby PGOOD Delay	400us for HVLDO = 3.3V
	VDDIO Supply Seletion	LDO3 (default)
	Multiphase Configuration	Single Phase

**Table 3. Voltage Regulators Configuration**

Functional block	Feature	OTP selection
VPRE Configuration	VPRE Voltage	3.3 V (default)
	Slope Compensation	41.4mv/us
	VPRE Standby Output Ctrl	Set by VPREV_STBY (I2C)
	ILIM sense Voltage	120 mV
	VPRE HighSide pull down Slew Rate Ctrl	PD/520mA (455Khz default value)
	VPRE HighSide pull up Slew Rate Ctrl	PU/520mA (455Khz default value)
	VPRE LowSide Slew Rate Ctrl	PU/PD/900mA (default value)
	Soft Start Ramp	2 mV/us (default)
	VPRE Off Time	80 ns
	TON in PFM	550 ns (default value)
	TON Min	45 ns
	Turn OFF Delay	250 us
VBOOST Configuration	VBOOST Voltage	5.00 V (default)
	Slope Compensation	67 mV/µs (default)
	Minimum TON	60 ns (default)
	Current Limit	2.25 A (default)
	Low Side Slew Rate Ctrl	500 V/us (default)
	Input Path to BOS	Enabled (default)

## Configuration report for QM OTP program ID: AN rev C

	Compensation Capacitor	125 pF (default)
	Compensation Resistor	500 kΩ (default)

**Table 4. BUCK Regulators**

Functional block	Feature	OTP selection
BUCK1 - Single Phase	Output Voltage	1.80000V
	Current Limit	3.6 A
	Output Inductor	1uH(default)
	TransConduct	65 u mho
	DVS Ramp of BUCK1 and BUCK2	7.8mV/us (power up) / 5.2mV/us (power down)
BUCK2 - Single Phase	Output Voltage	1.10000V
	Current Limit	3.6 A
	Output Inductor	1uH(default)
	TransConduct	65 u mho
BUCK3	Output Voltage	1.35V
	Current Limit	3.6 A
	Output Inductor	1uH(default)
	Ramp	3.47mV/us (power up/down)
	TransConduct BUCK3	65 u mho
	R Comp	56 KΩ

**Table 5. LDO Regulators**

Functional block	Feature	OTP selection
LDO1 Regulator	Output Voltage	1.8V
	Current Limit	400 mA (default)

## Configuration report for QM OTP program ID: AN rev C

LDO2 Regulator	Output Voltage	1.8V
	LDO Mode	LDO Mode (default)
LDO3 Regulator	Output Voltage	LS_Mode
	LDO Mode	Load Switch (default)

**Table 6. HVLDO Regulator**

Functional block	Feature	OTP selection
HVLDO Regulator	HVLDO Voltage	0.8 V (default)
	Sequence Control	Follows HVLDO_OTP slot
	Transition Mode	Switch in Normal / LDO in Standby (default)

**Table 7. Voltage Sequence and Timing Configuration**

Regulator	Sequence	Enabled	Phase Delay	Clock	TSD Event
VPRE	Auto-enabled	Enabled	No delay	CLK2	
VBOOST	Slot 0	Enabled	No delay	CLK1	Shutdown + DFS
BUCK1	Slot 0	Enabled	1 clock delay	CLK1	Shutdown + DFS
BUCK2	Slot 3	Enabled	2 clock delay	CLK1	Shutdown + DFS
BUCK3	Slot 1	Enabled	3 clock delay	CLK1	Shutdown + DFS
LDO1	Slot 1	Enabled			Shutdown + DFS
LDO2	Slot 3	Enabled			Shutdown + DFS
LDO3	Slot 0	Enabled			Shutdown + DFS
HVLDO	Slot 2	Enabled			Shutdown + DFS
SLOT Width	250 us				

**Table 8. Safety State Machine Configuration**

Functional block	Feature	OTP selection
Safety Configuration	FailSafe I2C Address	0x21

## Configuration report for QM OTP program ID: AN rev C

8sec Timer to DFS	Timer Disabled
ABIST1 to RSTB delay	5ms Delay
VCOREMON SVS Clamp Limit	No SVS
VCOREMON SVS Offset Type	Negative offset (default)
PGOOD assert with RSTB	PGOOD Asserts with RSTB Fault (default)
HVLDO Mode Select	Switch Mode (default)
WDI Polarity	Falling Edge
WDI on FCCU1	WDI Disabled (default)
STANDBY Mode	STANDBY Enabled (default)
STANDBY Polarity	Active Low in standby mode (default)
STANDBY Request Path	I2C + STBY Pin Transition (default)
STANDBY Window	STBY Window Enabled (default)
WD Init Timeout	1024ms
Fault Recovery Mode	Disabled
WD Selection	Simple WD
WD Monitoring	WD Disabled
FCCU Monitoring	FCCU Disabled
LBIST Enable	LBIST Disabled

**Table 9. Voltage Monitoring**

	VMONEN	Voltage	UV_TH	OV_TH	UV Dbnc	OV Dbnc	PGOOD Ctrl	ABIST Ctrl
<b>VCOREMON</b>	Enabled	1.80000V	95.5%	104.5%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
<b>VDDIOMON</b>	Enabled	3.3 V	95%	105%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP

## Configuration report for QM OTP program ID: AN rev C

<b>HVLDOMON</b>	Disabled	0.8 V	93%	107%	25 us	25 us	Not Assigned	No ABIST at PWRUP
<b>VMON1</b>	Enabled	0.8 V	95.5%	106%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
<b>VMON2</b>	Enabled	0.8 V	97.5%	104.5%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
<b>VMON3</b>	Enabled	0.8 V	95.5%	106%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP
<b>VMON4</b>	Enabled	0.8 V	95%	105%	25 us	25 us	PGOOD Assigned	No ABIST at PWRUP



## 8 Legal information

### 8.1 Definitions

**Draft** - The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included here in and shall have no liability for the consequences of use of such information.

**Limited warranty and liability** - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** - NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** - Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem

which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** - Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** - NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** - Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Suitability for use in automotive applications** - This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Export control** - This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** - A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 8.2 Trademarks

**Notice:** All referenced brands, product names, service names and trademarks are the property of their respective owners.

**NXP** - is a trademark of NXP B.V.

### Contents

---

1 General description .....	1
2 Features and benefits .....	1
3 Applications .....	1
4 Ordering information .....	1
5 Power up sequence summary .....	2
6 Hardware configuration diagram .....	2
7 OTP configuration .....	3
8 Legal information .....	9

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2022 .

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: Feb 9 2022

Document identifier: R\_MVR5510AMMANES