NXP Semiconductors
Engineering Bulletin

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MPC5674F: Flash Memory Accessibility Issues for Non-POR Reset

Contents

1 Description

Whenever a non-POR reset occurs, it can generate a glitch on the internal Flash A and B modules clock. There is a chance that this glitch may result in either (or both) flash modules becoming unresponsive.

The generation of the clock glitch is conditioned by a 5-degree temperature window (at high temperature) and voltage window which varies from device to device with normal process variation.

There are three different failure scenarios:

- Flash A is impacted or both flashes are impacted

  When Flash A is impacted, the device is not able to exit Boot Assist Monitor (BAM) code and the device will stay in serial boot mode, due to not finding the valid reset configuration word (RCHW) in flash memory. There is an active Software Watchdog Timer (SWT) during execution of BAM serial boot code which will assert reset after a duration that is based on the crystal frequency (see Figure 2).

- Flash B is impacted and the code is executed from Flash A

When the code is executed from Flash A and Flash B is impacted and is accessed an exception (machine check—IVOR1) is generated.

- Flash B is impacted and the code is also executed from Flash B

  When the code is executed from Flash B (the RCHW in Flash A is pointing the code execution into Flash B) and Flash B is stuck, the device stays in BAM code because the exception handler triggered by flash issue is part of BAM code. Software Watchdog Timer (SWT) is configurable during execution of BAM exception handler that is based on the crystal frequency (see Figure 3).

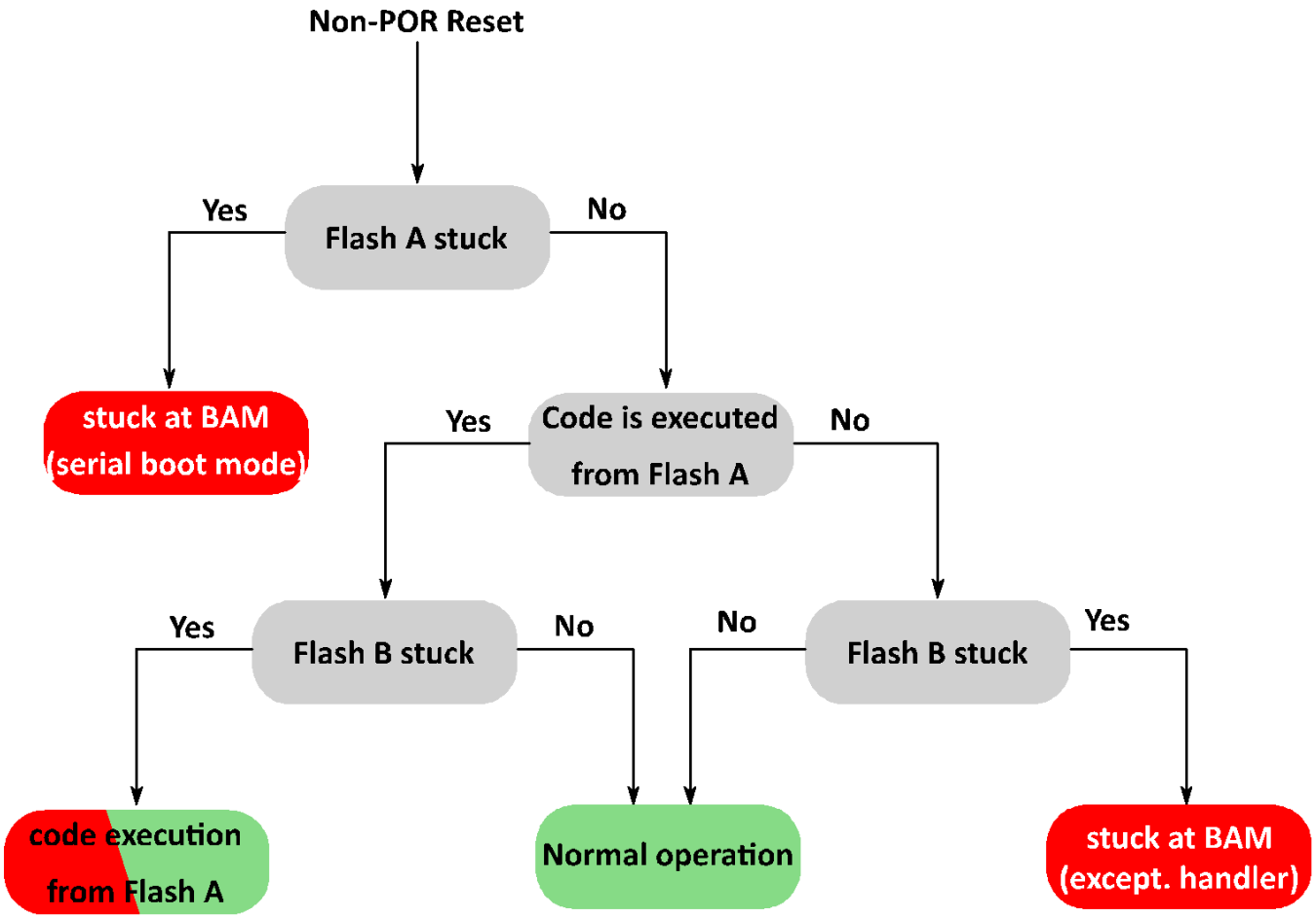

Figure 1. Possible scenarios of flash memory issues

Serial Boot Mode — Baud Rate and Watchdog Summary[1]

Crystal Frequency (MHz)	System Clock Frequency (MHz)	Desired Baud Rate (baud)	Actual eSCI Baud Rate (baud)	CAN Baud Rate (baud)	Core Watchdog Timeout period[2] (s)	SWT Timeout period during serial boot[3] (s)
f_{xtal}	$f_{sys} = 1.5*f_{xtal}$	—	f_{sys} / 1248	f_{sys} / 60	$2.5 * 2^{27} / f_{sys}$	$2.5 * 2^{27} / f_{xtal}$
8	12	9600	9615	200k	27.96	41.9
12	18	14400	14423	300k	18.64	28
16	24	19200	19230	400k	13.98	21
20	30	24000	24038	500k	11.18	16.8
40	60	48000	48077	1000k		8.4

1 With the PLL in normal mode and crystal oscillator as a reference clock source.

2 The core WD is disabled during serial boot and is then enabled after serial boot finishes (with timeouts indicated here)

3 The SWT is enabled during serial boot, but disabled after serial boot finishes.

Figure 2. Serial boot mode - Baud rate and Watchdog summary

Watchdog Timeout vs. Crystal Frequency[1]

Crystal Frequency (MHz)	Core WD Timeout (ms)	SWT Timeout (ms)
8	27.3	49
12	18.3	32.7
16	13.7	24.5
20	11	19.6
40		9.8

1 With the PLL in normal mode and crystal oscillator as a reference clock source.

Figure 3. Watchdog timer vs crystal frequency

2 Risk assessment

The risk of flash being stuck depends on the number of non-POR resets, the specific application profile of operation over voltage and temperature, and as noted above, the normal process variation from device to device. It is therefore not possible to specify an absolute risk for all conditions. A statement of impact is being included in an updated Design Failure Mode and Effect Analysis (DFMEA) document for this device.

3 Mitigation

Reduce the number of non-POR resets, which is the trigger of the issue, as much as possible.

4 Workaround

When the issue occurs, only a POR (power down/up cycle) is guaranteed to recover every time. Another source of reset (SWT reset, External reset, or Software reset) can recover the device, although there is some chance of the problem occurring again on that reset.

When Flash A is affected, an external watchdog that only asserts external RESET may work but is not guaranteed to work every time.

If Flash B is affected and the code is executed from Flash A, application code may detect the condition by checking Flash B's Module Control Register DONE bit (MCR[DONE]) and then issuing an external hardware reset via an external circuit, an internal software reset, or a system reset caused by SWT expiration. With these methods, there is some chance the issue will occur again after the reset.

When Flash B is affected and the code is executed from Flash B, you can use the system reset caused by the internal SWT to recover Flash B (SWT needs to be enabled in the RCHW configuration), although there is some chance of the problem occurring again on that reset.

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