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Using the HCS12 D Family as a Development Platform for the HCS12 B Family

1 Introduction

The purpose of this document is to help designers maintain compatibility when using a member of the HCS12 D family (Table 1) as an emulation tool when developing an application targeted at a member of the HCS12 B family (Table 2).

Allowing for some minor constraints, as detailed in each section, code can be written for a D family device which will then run unmodified on B128 and B64 devices. If the PWM module is used the code will require re-linking.

This document is intended for use in conjunction with the documents listed on the product summary page for these HCS12 products: see http://Freescale.com. A summary of the families is provided in Section 2, "Change History" followed by consideration of each peripheral module (roughly in sequence with the MC9S12DP256 Device User Guide) in Section 4, "B and D Module Summary." Memory maps and modules containing significant differences are then covered in subsequent sections.

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References to compatibility in this document describe logic level behavior where different devices contain the same modules. Typically, as new devices are developed, known errata are fixed. Before moving to a final target device, the appropriate device errata sheets should be evaluated to ensure there are no errata that might affect compatibility (in general, work-arounds for errata are compatible). An application should also be evaluated by the user when moving to a different device for application specific parameters such as EMC behavior.

2 Change History

Key changes to the MC9S12B family from Rev 3.0:

- Updated information to B128 and B64 references.

3 Overview of Families

Key points of consideration are:

- Peripheral count
  - The B128 and B64 generally have a reduced peripheral set from the D family.
  - The B128 and B64 do not support J1850 (BDLC).
  - B128 and B64 devices have one MSCAN module and one SPI module.
- Memory maps
  - Generally B128 and B64 devices of a specific Flash memory size will have less RAM and EEPROM than an equivalent D family device. Careful re-mapping of these modules is required to achieve compatible memory maps.
- Flash Memory
  - The HCS12Dx128 contains 2x 64K Flash modules where the HCS12B128 contains 1x 128K Flash module.
  - The HCS12Dx64 contains 1x 64K Flash module where the HCS12B64 contains 1x 128K Flash module (64K of which is reserved).
- Timer
  - The B128 and B64 Standard Timer is a subset of the D families Enhanced Capture Timer.
- ATD
  - The B128 and B64 have a single 16 channel, 10-bit ATD as opposed to the two 8 channel, 10-bit ATDs of the D family.

The B256 uses the D256 die tested only for B256 functionality. The B64 uses the B128 die tested only for B64 functionality. This results in identical PARTID and MEMSIZ register values as the master die. Reserved areas in the memory map should be observed when using the master die.

A summary of feature sets of appropriate D family devices can be found in Table 1. A full list of all devices in the D family can be found in the D family Product Brief.

Table 1. D Family Features[1]

Flash	RAM	EEPROM	Package	Device MC9S12–	CAN	SCI	SPI	A/D	PWM[2]	I/O
512K[3]	14K	4K	112LQFP	DP512	5	2	3	2/16	8	91
256K	12K	4K	112LQFP	DP256	5	2	3	2/16	8	91
				DT256	3	2	3	2/16	8	91
				DG256/DJ256 [4]	2	2	3	2/16	8	91
			80QFP	DG256/DJ256 [4]	2	2	3	1/8	7	59
128K	8K	2K	112LQFP	DT128	3	2	2	2/16	8	91
				DG128/DJ128 [4]	2	2	2	2/16	8	91
			80QFP	DG128/DJ128 [4]	2	2	2	1/8	7	59
64K	4K	1K	112LQFP	D64/DJ64 [4]	1	2	1	2/16	8	91
			80QFP	D64/DJ64 [4]	1	2	1	1/8	7	59

1 All devices have 8 channel ECT timer and IIC modules.
2 All devices have 8-channel PWM internally, only 7 channels are bonded out in 80QFP.
3 Implemented with physical 128K Flash module.
4 'J' devices have J1850 (BDLC module).

A summary of feature sets of the B128 and B64 devices can be found in Table 2.

Table 2. B Family Features[1]

Flash	RAM	EEPROM	Package	Device MC9S12–	CAN	SCI	SPI	A/D	PWM[2]	I/O
256K	8K	2K	112LQFP	B256	1	2	1	2/16	8ch	91
			80QFP	B256	1	2	1	8ch	7ch	59
128K[3]	4K	1K	112LQFP	B128	1	2	1	16ch	8ch	91
			80QFP	B128	1	2	1	8ch [4]	7ch	59
64K[3]	2K	1K	112QFP	B64	1	2	1	16ch [4]	8ch	91
			80QFP	B64	1	2	1	8ch [4]	7ch	59

1 All devices have an 8-channel Standard timer and IIC modules.
2 All devices have 8-channel PWM internally; only 7 channels are bonded out in 80QFP.
3 Implemented with physical 128K Flash module
4 16 channel ATD with only 8 analog input sources bonded out.

Due to the differing RAM and EEPROM sizes it is recommended that, wherever possible, development is carried out with the closest matching Flash size device. For example, if the target is a B128 then develop with a D128, etc.

Each device will have a unique identifier value encoded in the 'Part ID' registers. If desired, this value may be decoded by an application and appropriate routines selected for the specific device. See Section 5, "Part IDs," for details.

The 80-pin I/0 pitfalls, described in Engineering Bulletin EB386, are the same for both B and D families.

4 B and D Module Summary

4.1 Device Memory Maps

Each device has a unique combination of memory module sizes and peripheral modules and will therefore have a different memory map. Careful re-mapping of the memory modules is required for compatibility. See Section 6, “Device Memory Maps” for details. Where individual register addresses are presented in this document as $_ this indicates a module offset.

On the D family, there is no Flash memory mapped in the range $0000-$3FFF.

On the B128 and B64, Flash page $3D is mapped as a fixed page in the range $0000-$3FFF. Flash page $3D can alternatively be accessed via the paging mechanism in the range $3D8000-$3DBFFF, compatible with the D family. There are no compatibility issues for single chip applications as long as code is not allocated in the range $0000-$3FFF.

The ROMHM bit in the MISC register controls visibility of the internal Flash in the range $0000-$7FFF.

On the D family, ROMHM=0 – in expanded modes, accesses to addresses in the range $0000-$3FFF that are not allocated to Registers, RAM or EEPROM modules will generate external memory accesses. ROMHM=1 - unpaged accesses to fixed Flash page $3E are disabled. In expanded modes, accesses to addresses in the range $0000-$7FFF not allocated to Registers, RAM or EEPROM modules will generate external memory accesses.

On the B128 and B64, ROMHM=0 – in expanded modes, accesses to addresses in the range $0000-$3FFF that are not allocated to Registers, RAM or EEPROM modules will access internal Flash page $3D. ROMHM=1 - unpaged accesses to fixed Flash pages $3E and $3D are disabled. In expanded modes, accesses to addresses in the range $0000-$7FFF not allocated to Registers, RAM or EEPROM modules will generate external memory accesses.

The above differences must be taken into consideration when developing an expanded mode application which also runs code from internal Flash memory.

There are two configurations which offer compatibility:

- Where it is required to access expanded memory in the range $0000-$3FFF directly from code executing from paged Flash.
  - Set the ROMHM bit to disable visibility of the internal Flash in the range $0000-$7FFF.
  - Code should not be allocated to the internal fixed page $3E in the range $4000-$7FFF as visibility of the fixed Flash page $3E is disabled.
  - If required, access internal Flash pages $3D and $3E via the paging mechanism (at $3D8000-$3DBFFF and $3E8000-$3EBFFF respectively).
- Where it is acceptable to access the expanded memory via the paged window from code executing from fixed Flash or RAM.
  - Clear the ROMHM bit to retain visibility of the internal Flash in the range $0000-$7FFF (default).

— Map external resources in paged memory in a page that does not contain an internal Flash page and access via the paged window. For example, map to Page 00 and access in the range 008000-00BFFF.

— Ensure that all data accesses to expanded memory are executed from fixed memory — the PPAGE register must be configured appropriately.

— Code should not be allocated to the internal fixed page $3D in the range $0000-$3FFF as this isn't implemented on the D family.

4.2 Signal Description

Packages and pin-outs are equivalent and compatible.

Where a module on a D family device is not implemented on B128 and B64 devices its I/O functionality is not available on the appropriate ports. All other functionality of the appropriate I/O pins will be compatible.

The I/O assignment for the CAN RX and TX pins is equivalent to the default routing of CAN0 on the D family:

RXCAN pin 75/80-pin package or pin 105/112-pin package
TXCAN pin 74/80-pin package or pin 104/112-pin package

The alternative I/O routing of CAN0 is not available on B128 and B64. See Port Integration Module block guide.

4.3 System Clock

The system clock distribution is compatible.

Obviously, where modules are not implemented, the clock is not routed.

4.4 Modes of Operation

Modes of operation and security are compatible.

Earlier D family devices only use one bit for enabling the security backdoor key. Later D family devices use two bits.

All B128 and B64 devices use two bits.

For compatibility, when backdoor key access is required always ensure that bit-6 of the Flash Protection Option byte ($FF0F in Flash block 0) is programmed to zero.

4.5 Resets and Interrupts/Vector tables

Resets and Interrupts are functionally compatible.

Where an interrupt is associated with a module not implemented on B128 or B64 device the vector locations are reserved. For compatibility, these locations should remain unused and unprogrammed or, for good practice, be configured to point to a TRAP routine.

4.6 HCS12 Core

The HCS12 Core is unchanged.

Low Power Modes, External Bus Control, Background Debug Mode and Memory Mapping control are all compatible.

4.7 Clock and Reset Generator (CRG)

The CRG logic is compatible.

The oscillator module on the B128 and B64 will be selectable for either ‘low power Colpitts oscillator’ or ‘Pierce oscillator/external clock’ configurations, compatible with the Dx128 and D64 device.

The current Dx256 devices support the ‘low power Colpitts oscillator’ or ‘external clock’ options. The pin out and Colpitts oscillator circuit is compatible for either of these two options.

4.8 Timer

The B128 and B64 timer (TIM) is a subset of the D family timer (ECT).

See Section 6.3, “Timer”for details.

4.9 Analog To Digital Converter (ATD)

The D family has two 8-channel ATD converters, the B128 and B64 have a single 16-channel ATD converter. Compatibility when using eight or less channels can be achieved using ADT0 on the D family and observing constraints.

Code changes will be required to make use of analog inputs AN[15:8].

See Section 7, “ATD” for details.

4.10 Inter IC Interface (IIC)

The IIC modules are functionally compatible.

4.11 Serial Communications Interface (SCI)

The SCI modules are functionally compatible.

4.12 Serial Peripheral Interface (SPI)

The SPI0 module is functionally compatible.

SPI1 and SPI2 are not on the B128 and B64 devices. On the D family, addresses will be reserved and should therefore not be accessed.

4.13 Pulse Width Modulator (PWM)

The PWM module is functionally compatible. On the D family, it is mapped at $00A0. On the B128 and B64, it is mapped at $0200 (On the D family this location contains the CAN3 module).

4.14 Flash EEPROM

The HCS12Dx128 contains 2x 64K Flash modules where the HCS12B128 contains 1x 128K Flash module.
The HCS12Dx64 contains 1x 64K Flash module where the HCS12B64 contains 1x 128K Flash module.

Table 3. 64K vs. 128K Flash Block Differences

	64K Flash Block	128K Flash Block
Physical Flash blocks	64K	128K
Pages per block	4 x 16K	8 x 16K
Burst programming row size	64 bytes	128 bytes
Erase sector size	512 bytes	1024 bytes
Upper protection sector size (one per block)	2K / 4K / 8K /16K	2K / 4K / 8K /16K
Lower protection sector size (one per block)	0.5K / 1K / 2K /4K	1K / 2K / 4K / 8K

Read while write operations from Flash are compatible and the differences are transparent.

On the B128 device (as opposed to the D128) there is only one Flash block which rules out the capability of executing code from one Flash block while modifying the contents of another. It is still possible to execute code in RAM to modify the contents of the Flash block.

There is no register memory map change but when Flash is being programmed it must be understood that some Flash pages will be in different Flash blocks. This affects the values written to the PPAGE register and to the Block Select bits (BKSEL[1:0]) in the Flash Configuration Register (FCNFG) when writing to the Flash.

The low level Flash state machine algorithms are compatible (sector erase will erase 1024 bytes on devices with 128K Flash modules and 512 bytes on ones with 64K modules).

The B128 and B64 and D family high level Flash programming algorithms will be different. Where in-system Flash programming is required the application can select appropriate code for writing to the Flash depending on the value of the Part ID register (Table 5 and Table 6).

Low level Flash timing is compatible. On devices implemented with 128K Flash modules Sector Erase can be more efficient (as the Sector Erase timing is the same but 512 bytes are erased as opposed to 256 bytes on a 64K Flash module).

The Flash security mechanism is identical on the D family and the B128 and B64.

The Flash protection mechanism is the same on the B128 and B64 and the D family. In all devices it is possible to completely protect each of the individual Flash blocks. There are two selectable protection

areas in each Flash block. The Flash pages containing the protected areas and the size of the protected areas will be different for a device with 128K Flash blocks versus a device with 64K Flash blocks. See Table 4.

Table 4. Flash Page Physical Block Mapping

Flash Page	Dx512	Dx256	B256	Dx128	B128	D64	B64
$20	Block 3						
$21	Block 3						
$22	Block 3						
$23	Block 3						
$24	Block 3						
$25	Block 3						
$26	Block 3[1]						
$27	Block 3[1]						
$28	Block 2						
$29	Block 2						
$2A	Block 2						
$2B	Block 2						
$2C	Block 2						
$2D	Block 2						
$2E	Block 2[1]						
$2F	Block 2[1]						
$30	Block 1	Block 3	Block 3	-	-		-
$31	Block 1	Block 3	Block 3	-	-		-
$32	Block 1	Block 3[1]	Block 3	-	-		-
$33	Block 1	Block 3[1]	Block 3	-	-		-
$34	Block 1	Block 2	Block 2	-	-		-
$35	Block 1	Block 2	Block 2	-	-		-
$36	Block 1[1]	Block 2[1]	Block 2[1]	-	-		-
$37	Block 1[1]*	Block 2[1]	Block 2[1]	-	-		-
$38	Block 0	Block 1	Block 1	Block 1	Block 0		Reserved
$39	Block 0	Block 1	Block 1	Block 1	Block 0		Reserved
$3A	Block 0	Block 1[1]	Block 1[1]	Block 1[1]	Block 0		Reserved
$3B	Block 0	Block 1[1]	Block 1[1]	Block 1[1]	Block 0		Reserved
$3C	Block 0	Block 0	Block 0	Block 0	Block 0	Block 0	Block 0
$3D	Block 0	Block 0	Block 0	Block 0	Block 0	Block 0	Block 0
$3E	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]
$3F	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]	Block 0[1]

[1] Pages containing protected sectors

The Flash allocation for different Flash size devices is detailed in Engineering Bulletin EB386.

4.15 EEPROM

The EEPROM modules are functionally compatible.

The EEPROM array size on comparable Flash devices is generally smaller on B128 and B64. To ensure compatibility, usage should be limited to the array address range on the target B128 and B64 devices and the memory mapping must be compatible (it is important to ensure that the protection/reserved field is at the same location). See Section 6, “Device Memory Maps” for details.

4.16 RAM

The RAM modules are functionally compatible.

The RAM array size on comparable Flash devices is generally smaller on B128 and B64. To ensure compatibility, usage should be limited to the array address range on the target B128 and B64 devices and the memory mapping must be compatible. See Section 6, “Device Memory Maps” for details.

The B64 has 2K of RAM that is mappable to any 4K block as a 4K block, with the lower order address of the 2K space represented.

4.17 MSCAN

The MSCAN0 module is functionally compatible. MSCAN 1,2,3 and 4 are not implemented on the B128 and B64 and their registers addresses will be reserved and should therefore not be accessed.

Alternative routing of CAN0 I/O is not available on the B128 and B64.

4.18 Port Integration Module (PIM)

Since the parts each have a different set of peripherals, some minor differences in the PIM must be considered. The PIM modules on all B and D family devices contain the same Port control and status registers and are compatible when used for general purpose I/O.

As each device has a different number of peripherals requiring I/O multiplexing, some of the functionality of the larger devices will not be available on a smaller device where an equivalent module isn’t implemented. As this multiplexing occurs automatically as peripherals are enabled or disabled there are no compatibility issues.

Where a module on a D family device is not implemented on B128 and B64 devices, it’s functionality is not available on the appropriate I/O pins. For example, as only MSCAN0 is available on the B128 and B64, on B devices port pins PTM6, PTM7, PTJ6 and PTJ7 will be general purpose I/O only.

4.19 Voltage Regulator (VREG)

The VREG on the B64 and B128 have additional support for Low Voltage Interrupt (LVI) and Low Voltage Reset (LVR) functions. The default state is for Low Voltage Interrupt (LVI) to be disabled, which is compatible with the D family.

The B128 and B64 have a band-gap reference voltage regulator which allows it to run down to 3.3V. For 5V operation, it is compatible with the D family. Power supply layout for the D family devices will be compatible for B128 and B64 targets.

The B128 and B64 have an added VREG control register at $0019. This location is a reserved register on the D family.

4.20 BDLC

This module (on the DJ devices) is not implemented on B128 and B64. The relevant register addresses will be reserved and should therefore not be accessed.

5 Part IDs

The part ID on each device is “coded” in two 8-bit registers, PARTIDH and PARTIDL (address offset $_1A and $_1B), in the Core register block. The read-only value is a part ID for each revision of any device.

Bits 7:4 of PARTIDH contain the family identifier.
Bits 3:0 of PARTIDH contain the family member identifier.

The PARTIDH values for D family devices are shown in Table 5.

Table 5. D Family Device ID Value

D family Device	PARTIDH
MC9S12Dx512	$04
MC9S12Dx256	$00
MC9S12Dx128	$01
MC9S12Dx64	$02
MC9S12Dx32	$03

The PARTIDH values for B128 and B64 devices is shown in Table 6.

Table 6. B128 and B64 Device ID Value

B128 and B64 Devices	PARTIDH
MC9S12B256	$20
MC9S12B128	$21
MC9S12B64	$21

The PARTIDL value will be unique for each silicon revision.

The initial B64 device uses the same silicon as the B128 and the B256 is the same silicon as the D256, the PARTID values are the same.

6 Device Memory Maps

6.1 Peripheral Module Map

A comparison of the Register Block memory maps of the 9S12DT128 and the B128 and B64 devices following reset is provided in Table 7.

Table 7. Register Block Memory Map Comparison[1]

Address on Reset	MC9S12DT128 Module	B128 and B64 Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018	Reserved	Reserved	1
$0019		**VREGCTRL**	1
$001A – $001B	CORE (Device ID register (PARTID))	CORE (Device ID register (PARTID))	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	Reserved	8
$0028 – $002F	CORE (Background Debug Mode)	CORE (Background Debug Mode)	8
$0030 – $0033	CORE (PPAGE, Port K)	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $006F	Enhanced Capture Timer 16-bit 8 channels	Standard Timer 16-bit 8 channels	48
$0070 – $007F		**Reserved**	16
$0080 – $009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	**Analog to Digital Converter 10-bit 16 channels (ATD) ***	32
$00A0 – $00AF	Pulse Width Modulator 8-bit 8 channels (PWM)		16
$00B0 – $00C7		**Reserved**	24
$00C8 – $00CF	Serial Communications Interface 0 (SCI0)	Serial Communications Interface 0 (SCI0)	8
$00D0–$00D7	Serial Communications Interface 1 (SCI1)	Serial Communications Interface 1 (SCI1)	8
$00D8–$00DF	Reserved	Serial Peripheral Interface (SPI0)	8
$00E0–$00E7	Inter IC Bus (IIC)	Inter IC Bus (IIC)	8
$00E8–$00EF	Byte Data Link Controller (BDLC)	**Reserved**	8
$00F0–$00F7	Serial Peripheral Interface (SPI1)	**Reserved**	8
$00F8–$00FF	Serial Peripheral Interface (SPI2)	**Reserved**	8
$0100–$010F	Flash Control Register	Flash Control Register	16
$0110–$011B	EEPROM Control Register	EEPROM Control Register	12
$011 –$011F	Reserved	Reserved	4
$0120–$013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	**Reserved**	32
$0140–$017F	Freescale Scalable Can (CAN0)	Freescale Scalable Can (CAN0)	64

Table 7. Register Block Memory Map Comparison[1] (continued)

Address on Reset	MC9S12DT128 Module	B128 and B64 Module	Size (Bytes)
$0180–$01BF	Freescale Scalable Can (CAN1)	**Reserved**	64
$01C0–$01FF	Reserved	**Reserved**	64
$0200–$0227	Reserved	**Pulse Width Modulator 8-bit 8 channels (PWM)**	40
$0228–$023F		**Reserved**	24
$0240–$027F	Port Integration Module (PIM)	Port Integration Module (PIM)	64
$0280–$02BF	Freescale Scalable Can (CAN4)	**Reserved**	64
$02C0–$03FF	Reserved	Reserved	320

1 **Bold** indicates differences

The Register block can be re-mapped to any 2K boundary in the 64K memory map.

For compatibility, the registers in the reserved sections on B128 and B64 target devices should not be accessed when developing an application with a D family device.

6.2 Register Block, RAM and EEPROM Maps

6.2.1 Device maps

The following tables compare the device maps of similarly sized Flash devices from the D and B families following reset.

Table 8. 256K Flash Memory Map Following Reset

	Dx256	B256
Registers	$0000–$03FF: 1K	$0000–$03FF: 1K
RAM	$1000–$3FFF: 12K	($1000–$1FFF: 4K reserved)[1] $2000–$3FFF: 8K
EEPROM	$0000–$0FFF: 4K ($0000–$03FF: 1K not visible)	($0000–$03FF: 1K not visible /reserved) ($0400-$07FF: 1K reserved) $0800–$0FFF: 2K)[2]

1 On the B256 the 8K RAM is mappable to any 16k space as a 12K block, and alignable to top or bottom. The lower order address of the 4K space is reserved.

2 On the B256 the 2K of EEPROM is mappable to any 4k block as a 4k block, with the lower order address of the 2K space reserved.

Table 9. 128K Flash Memory Map Following Reset

	Dx128	B128
Registers	$0000–$03FF: 1K	$0000–$03FF: 1K
RAM	$0000–$1FFF: 8K ($0000–$03FF not visible)	$0000–$0FFF: 4K ($0000–$03FF: 1K not visible)
EEPROM	$0000–$07FF: 2K (not visible)	$0000–$07FF: 1K (not visible) [1]

[1] A 1K EEPROM module appears in a 2K space twice, at $0000–$03FF and $0400–$07FF. The protection/reserved field also appears twice at $03F0–$03FF and $07F0–$07FF.

Table 10. 64K Flash Memory Map Following Reset

	Dx64	B64
Registers	$0000–$03FF: 1K	$0000–$3FF: 1K
RAM	$0000–$0FFF: 4K ($0000–$03FF: 1K not visible)	($0000–$07FF: 2K reserved[1] $0800–$0FFF: 2K
EEPROM	$0000–$03FF: 1K (not visible)[2]	$0000–$07FF: 1K (not visible) [2]

[1] On the B64 the 2K of RAM is mappable to any 4K block as a 4K block, with lower order address of the 2K space reserved.

[2] A 1K EEPROM module appears in a 2K space twice, at $0000–$03FF and $0400–$07FF. The protection/reserved field also appears twice at $03F0–$03FF and $07F0–$07FF.

6.2.2 Re-mapping

When using a D family device to emulate B128 and B64 devices, a compatible memory map must be used to ensure that the equivalent memory is accessed at the same locations on each device.

Three position registers in the Core register block control the location of the memory blocks:

- INITRG – Initialization of Internal Registers Position Register
- INITRM – Initialization of Internal RAM Position Register
- INITEE – Initialization of Internal EEPROM Position Register

To ensure compatibility the D device map must be a superset of the target B device map. For software compatibility the maps should be valid for the same position register values and the top of the EEPROM maps should be aligned so that the protection/ reserved field is at the same address.

The rules that control the re-mapping of memory blocks are well documented in Engineering Bulletin EB386 and the recommended options for the position registers are also valid for the B128 and B64. Table 11 and Table 12 show examples of compatible mappings.

INITRG = 0x00;
INITRM = 0x39;
INITEE = 0x09;

Table 11. Re-mapping to Locate the Registers Block in the Direct Page

Device	Registers	RAM	EEPROM
B256	$0000–$03FF	$2000–$3FFF: 8K	$0800–$0FFF[1] : 2K
B128	$0000–$03FF	$3000–$3FFF: 4K	$0800–$0FFF [2]: 1K
B64	$0000–$03FF	$3000–$37FF[3]: 2K	$0800–$0FFF [2]: 1K

1 On the B 256 the 2K EEPROM module is mapped as a 4K block, with the lower order address of the 2K space reserved.

2 The 1K EEPROM module appears twice, at $0800–$0BFF and $0C00–$0FFF. For compatibility, access the EEPROM in the range $0C00–$0FFF. This locates the protection/reserved field at $0FF0–$0FFF on all devices.

3 On the B64 lower order address of 2K space of the 4K block of RAM is reserved.

INITRG = 0x30;
INITRM = 0x00;
INITEE = 0x39;

Table 12. Re-mapping to Locate the RAM in the Direct Page

Device	Registers	RAM	EEPROM
B256	$3000–$33FF	$0000–$1FFF: 8K	$3800–$3FFF: 2K
B128	$3000–$33FF	$0000–$0FFF: 4K	$3800–$3FFF[1]: 1K
B64	$3000–$33FF	$0000–$07FF [2]: 2K	$3800–$3FFF[1]: 1K

1 The 1K EEPROM module appears twice, at $3800–$3BFF and $3C00–$3FFF. For compatibility, access the EEPROM in the range $3C00–$3FFF. This locates the protection/reserved field at $3FF0–$3FFF on all devices.

2 On the B64 the lower order address of 2K of the 4K RAM space is reserved.

Using the above options ensures that any D family device of an equivalent or larger Flash size will have a compatible memory map.

Using D family devices to emulate the B128 and B64 restricts access to the non-paged Flash at $0000-$3FFF as there is no Flash at this location on the D family devices.

These are not the only possible configurations and alternative mappings may be more effective for some applications. For example where one of the modules might be mapped over the Flash to allow a window to external memory or where modules might be mapped over the paged window ($8000-$BFFF) to maximize access to the non-paged memory.

6.3 Timer

The B128 and B64 have a Standard Timer (TIM_16B8C) with

- A 16-bit free running timer
- A timer overflow to extend the 16-bit range of the counter

- Up to eight output compare functions (O/C).
- Up to eight input capture functions (I/C).
- A 16-bit Pulse Accumulator on channel-7 (Gated Time Accumulation and Event Counter modes).

The D family has an Enhanced Capture Timer (ECT_16B8C) which is a superset of the Standard timer. The following features are not available on the B128 and B64 timer:

- 16-bit buffer registers on input capture channels 0 to 3.
- User selectable Delay counters on channels 0 to 3 for increased noise immunity.
- A 2nd 16-bit Pulse Accumulator (Event Counter Mode) on channel 0.
- Four 8-bit, buffered Pulse Accumulators (Event Counter Mode) on channels 0 to 3 (these share registers with the two 16-bit PA so you can have either one 16-bit PA or two 8-bit PA in each case).
- A 16-bit Modulus Down Counter with 4-bit prescaler. Controls the transfer period of data into the I/C or PA buffers in Latch Modes and/or generates a periodic interrupt.

NOTE

On the ECT, the Standard Timer 16-bit PA is called Pulse Accumulator A.

6.3.1 Timer Interrupts

The following vectors are common to the D and B128 and B64 timers:

```
$FFEE-$FFEF     Timer channel 0
$FFEC-$FFED     Timer channel 1
$FFEA-$FFEB     Timer channel 2
$FFE8-$FFE9     Timer channel 3
$FFE6-$FFE7     Timer channel 4
$FFE4-$FFE5     Timer channel 5
$FFE2-$FFE3     Timer channel 6
$FFE0-$FFE1     Timer channel 7
$FFDE-$FFDF     Timer overflow
$FFDC-$FFDD     Pulse accumulator (A) overflow
$FFDA-$FFDB     Pulse accumulator (A) input edge
```

On the D family, these additional interrupts support the enhanced features of the ECT:

```
$FFCA-$FFCB     Modulus Down Counter Underflow
$FFC8-$FFC9     Pulse Accumulator B Overflow
```

On the B128 and B64 these two vector locations are reserved. For compatibility, they should remain unused and unprogrammed or, for good practice, be configured to point to a TRAP routine.

7 ATD

The HCS12 ATD converter is based on a modular design. The D family ATD module (referred to as D_ATD) and B128 and B64 ATD modules (referred to as B_ATD) are variants of the core HCS12 ATD

optimized for the two different families. The actual analog conversion module and I/O are the same design. The control and functionality of the two modules are very similar.

Each ATD converter can be configured for clock speed, sample time period, conversion resolution, result data format and interaction with MCU modes.

Conversion sequences define which analog source to start conversion at and (if multiple conversions are selected) how many sequential conversions to carry out. Scan mode can be selected to continuously repeat a conversion sequence.

A conversion sequence is initiated by a write to the ATDCTL5 register and, if enabled, a valid signal on an external trigger input.

Definitions used in this document:

- PADxx – port pin used for general purpose digital input.
- ANxx – Analog signal input pin.
- ADxx – analog converter input channel.

The D family has two independent 8 channel, 10-bit ATD modules (ATD_10B8C) each with:

- Analog Input Multiplexer for 8 Analog Input Channels.
- 1 to 8 Conversion Sequence Lengths.
- External trigger on channel AN07 (ATD0) and AN07 (ATD1).
- i/p channel wrap around at AD07.

The B128 and B64 have a single 16 channel, 10-bit ATD (ATD_10B16C) module (which is in many aspects a superset of the D_ATD module) with:

- Analog Input Multiplexer for 16 Analog Input Channels.
- 1 to 16 Conversion Sequence Lengths.
- Programmable external trigger AN0–AN15.
- Programmable I/O channel wrap around AN0–AN15.

7.1 Compatibility Constraints

Applications requiring greater than 8 analog inputs and / or using the digital input port functionality on PAD[15:08] will require code changes. Compatibility for greater than 8 channels is not considered in this document.

- Where an application’s requirements can be met with a single 8-channel D_ATD (ATD0) it is possible to achieve compatibility allowing for certain constraints:
- Only use ATD0 on the D family.
- Input channel wrap-around is compatible with special considerations only (Section 7.2, “Input Channel Wrap Around”).
- FIFO mode is not compatible (Section 7.3, “FIFO Mode”).
- External trigger is compatible with special considerations only (Section 7.4, “External Trigger Source”).

With careful planning of conversion sequences the flexibility of conversions available on the D_ATD can be maintained.

7.2 Input Channel Wrap Around

On the D_ATD, in the case of a multiple conversion sequence (MULT bit = 1), when the input selector goes past AD7 it wraps to AD0.

To make the B128 and B64 compatible for wrap around, code changes will be necessary. A write of $07 to ATDCTL0 (ATD Control Register 0) will configure ATD to wrap around from AN7 to AN0.

7.3 FIFO Mode

FIFO mode is incompatible due to the increase in FIFO depth – 2 x 8 deep FIFOs on the D family and 1x 16 deep FIFO on the B128 and B64. For compatibility, FIFO mode should not be used.

7.4 External Trigger Source

On the D family the external trigger source is located on channel AN07, and is enabled by setting the ETRIGE bit in the ATDCTL2 (ATD Control Register 2). On the B128 and B64 the channel for external trigger is selectable. Setting the ETRIGE bit in the ATDCTL2 (ATD Control Register 2) for enabling the external trigger is the same. The channel is selected by setting bits in the ATDCTL1 (ATD Control Register 1). On the D family, ATDCTL1 register is reserved.

To make the B128 and B64 compatible to the D family, code changes will be necessary. By writing a $07 to $0081, the external trigger will be configured for AN07.

NOTE

On the D family in special modes, writes to $0080 and 0081 may have affects on these registers.

7.5 ATD Interrupts

This vector is common to the B and D family ATD:

```
$FFD2-$FFD3    ATD/ATD0
```

7.6 ATD Memory Maps

D family memory map following reset (2 x ATD_10B8C)

```
$0080-$009F      ATD0     (32 bytes)
$0120-$013F      ATD1     (32 bytes)
```

B128 and B64 memory map following reset (1 x ATD_10B16C)

```
$0080-$00AF      ATD      (48 bytes)
```

7.7 Registers on the B128 and B64 ATD Containing Additional Bits

7.7.1 ATDCTL3 – Conversion Sequence Length

On the D family ATD the max conversion sequence length is 8.

On the B128 and B64 ATD it is 16. Writing the SCx bits with a value greater than 8 has a different effect on the D family than on the B64/B128. For example, the value x0000xxx on the D family will equate to 8 conversions and on the B128 and B64 it will equate to 16 conversions. Another example, the value of x1001xxx on the D family will equate to 8 conversions, and on the B128 and B64 it will equate to 9 conversions.

See ATD_10B16C BUG, V03.00, page 20 for more detail.

7.7.2 ATDSTAT0 – Conversion Complete Flags

On the D family each converter has a three-bit conversion counter to track up to 8 channel conversion sequences.

On the B128 and B64 converters there are 4-bit conversion counters to track up to 16 channel conversion sequences.

For conversion sequences of 8-channels or less CCR will always read ‘0’.

See ATD_10B8C BUG, V3.00, page 26 for more detail.

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