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Noise Considerations with the Low-Power, 32-kHz Crystal on the MC9S08GB60

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Introduction

This bulletin describes concerns when using the low-power 32-kHz (low range) crystal oscillator circuit on an MC9S08GB/GT MCU in the presence of noise. Particularly, this bulletin contains recommendations to follow when using high slew rate I/O drivers and the low-power 32-kHz (or any low-range) crystal oscillator circuit.

Due to the low-power nature of the oscillator, the oscillator circuit may be unable to distinguish between noise coupled onto the EXTAL and XTAL pins (relative to V_{DD} or V_{SS}) and the intended waveform. Noise of this type may be generated by external sources or by a large number of high slew rate I/O drivers switching simultaneously. This may result in extra clocks or variable duty cycle on the clock input, leading to possible application disruption.

Description of Noise Sensitivity

The clock input that senses the differential waveform between EXTAL and XTAL uses a hysteresis buffer which has between 75 mV and 300 mV of hysteresis (typically 150 mV). This hysteresis prevents extraneous clock switching when low-level noise is coupled onto the EXTAL or XTAL pins relative to V_{DD} or V_{SS}. This hysteresis level is appropriate given the low amplitude of oscillation required for low-power crystal oscillators.

When operating with a 32-kHz crystal oscillator (or other low-frequency oscillator), which typically is a sine wave with a peak-to-peak magnitude of 700 mV to 1000 mV, the EXTAL and XTAL signals may be within 100 mV of each other for several hundred nanoseconds. During this time, noise with a magnitude greater than the hysteresis of the input buffer may cause an extra clock pulse to the microcontroller. This extra clock pulse normally has a very

narrow pulsewidth. The types of application disturbances that are possible with this narrow clock pulse include, but are not limited to:

- Loss of accuracy when using the crystal oscillator as a timebase reference
- Loss of ICG lock when in FEE mode

The disruptive noise can be one of the following forms:

- EXTAL relative to XTAL — This form of noise is usually caused by differentially unequal coupling to a noise source (such as an errant circuit board trace, V_{SS} or V_{DD}). Noise of this form directly reduces the effective hysteresis of the buffer by the magnitude of the noise.
- EXTAL/XTAL relative to V_{SS} or V_{DD} — This form of noise is caused by the coupling of a noise source to both signals equally (such as the parasitic ESD diodes to V_{DD} internally in the microcontroller). The input buffer is most sensitive to this form of noise when the inputs are nearly equal. At this point, the amplifier will be sensitive to V_{DD} or V_{SS} noise of approximately two to three times the hysteresis of the input buffer. (The actual sensitivity depends on the noise waveshape and frequency content but has been observed as low as 250 mV.)

Description of High Slew Rate I/O Noise Generation

The MC9S08GB/GT and similar HCS08 microcontrollers provide the user the flexibility of controlling the slew rate of the I/O pads of the general-purpose ports. Most applications will prefer the controlled slew rate setting (slew rate control enabled) so that the dV/dt of the output signals and the resultant EMI are reduced. This setting also reduces the dI/dt and d^2I/dt^2 of the output drivers, which reduces the radiated noise in the parasitic inductors that are always present in the microcontroller package and on the circuit board. In some applications, the faster edge rates provided by the high slew rate setting (slew rate control disabled, which is the default setting out of reset) are preferable to low-noise operation so that restrictive timing constraints of external devices can be met.

When the high slew rate setting is used, the high dI/dt required by the pad driver to meet the slew rate requirements will cause a large transient voltage to appear across the parasitic inductances of the I/O driver package connection and the V_{DD} and V_{SS} package connections. Since the dI/dt is highest when the driver shuts off after completing a transition, the resultant undershoot and overshoot can be of a magnitude large enough to turn on the parasitic ESD protection diodes to shunt the excess current safely to V_{DD} or V_{SS}. This excess current, in addition to the transient voltage on V_{DD} or V_{SS} (due to each rail's dI/dt), results in V_{DD} or V_{SS} noise.

This noise, which is an unfortunate but necessary byproduct of achieving fast edge rates, will affect the oscillator when operated in low-range mode. On non-optimum board designs, the noise on V_{DD} caused by the simultaneous switching of several I/O pins with slew rate disabled can exceed 350 mV to 400 mV. Because the microcontroller can be sensitive to V_{DD} noise as low as 250 mV when operating with a 32-kHz crystal, the number of pins that can simultaneously switch with slew rate disabled must be limited.

The recommended limitation on simultaneous switching on high slew rate I/O pins is:

- PTC/PTF — Maximum of two high slew rate I/Os switching simultaneously
- All other ports — Maximum of four high slew rate I/Os switching simultaneously

Application and Board Recommendations for 32-kHz Crystal Operation

For proper operation of the 32-kHz (or any low-range) low-power crystal oscillator, several recommendations should be followed. Strict observance of these recommendations does not guarantee immunity to noise, and other noise-reduction techniques may be necessary in extreme situations. In most applications, the risk of noise related issues is significantly reduced if these recommendations are followed:

- A maximum of two high slew rate I/Os on PTC or PTF may switch simultaneously
- A maximum of four high slew rate I/Os on other ports may switch simultaneously
- A 0.01 µF ceramic capacitor must be within 0.5 cm of the V_{DD}/V_{SS} pins
- A 0.1 µF ceramic capacitor must be within 2 cm of the V_{DD}/V_{SS} pins
- The EXTAL and XTAL pins must have a maximum total trace length of 5 cm (3 cm strongly recommended)
- The EXTAL and XTAL signal traces must be shielded with V_{SS} from all other signals in all dimensions; this includes the entire body of all the components as well as the vias of any through-hole components
- The EXTAL and XTAL signal traces must be shielded with V_{SS} from each other in all dimensions, starting no more than 0.5 cm from the MCU package edge or 0.3 cm from shared components
- Differential V_{DD} to V_{SS} noise may not exceed 250 mV in any situation; special care must be given to applications that drive motors, solenoids, triacs, amplifiers, and other large and/or inductive loads to isolate the transients due to the load from V_{DD} and V_{SS}

Operation of High-Frequency Oscillators, Canned Oscillators, and External Clock Sources

When operating with high frequency oscillators (1 MHz – 16 MHz), canned oscillators, or other external clock sources, the noise sensitivity is greatly reduced because the oscillator spends much less time in the input buffer's sensitive range. With a 1-MHz sine wave of 700 mV amplitude, the EXTAL and XTAL signals are within 100 mV of each other for only a few nanoseconds (even less with square wave or higher-frequency inputs). Since the noise pulses that the input buffer is sensitive to are on the order of 10 ns wide, the input buffer is much less likely to react to noise than at 32 kHz.

As a result, there is no limitation on the number of high slew rate I/O pins that may simultaneously switch. Likewise, the magnitude of allowable noise on V_{DD} is not restricted to 250 mV for proper oscillator operation. However, Motorola strongly suggests that all of the recommendations for low-range oscillator operation be observed for operation with high frequency oscillators, canned oscillators, and external clock sources (with the exception of shielding EXTAL from XTAL, which is not necessary for operation with canned oscillators or external clock sources).

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