ES_LPC2103

Errata sheet LPC2103

Rev. 2 — 1 March 2011 **Errata sheet**

Document information

Info	Content
Keywords	LPC2103 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
2	20110301	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added ADC.1
1.5	20080721	• Added Rev B.
1.4	20080607	• Added VBAT.1.
1.3	20080212	• Added Rev ‘A’ and updated the errata history table
1.2	20070713	• Added MAM.2. • Added I2C1.1. • Updated ESD.1
1.1	20060227	• This table was added after document revision 1.1.

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Product identification

The LPC2103 devices typically have the following top-side marking:

LPC2103xxx

xxxxxxx

xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2103:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision
'A'	Second device revision
'B'	Third device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
Core.1	Incorrect update of the Abort link register	'-', 'A', 'B'	Section 3.1
MAM.1	Incorrect read of data from SRAM	'-'	Section 3.2
MAM.2	Code execution failure can occur with MAM Mode 2	'-', 'A'	Section 3.3
SPI.1	Incorrect shifting of data in slave mode at lower frequencies	'-'	Section 3.4
SSP.1	Initial data bits/clocks corrupted in SSP transmission	'-', 'A', 'B'	Section 3.5
Timer.1	Timer Counter reset occurs on incorrect edge in counter mode	'-'	Section 3.6
Vdd.1	Device may not work properly under increased power consumption	'-'	Section 3.7
$I^2C1.1$	I^2C1 pins are not bi-directional GPIO pins	'-'	Section 3.8
ADC.1	External sync inputs not operational	'-', 'A', 'B'	Section 3.9

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
ESD.1	ESD weakness on RTCX1 pin	'-'	Section 4.1
VBAT.1	Increased power consumption on the VBAT pin when the $VDD_{(1V8)}$ core pin is left floating	'-'	Section 4.2

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 Core.1: Incorrect update of the Abort Link register in Thumb state

Introduction:

If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem:

In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work-around:

In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

3.2 MAM.1: Incorrect read of data from SRAM after Reset and MAM is not enabled or partially enabled

Introduction:

The Memory Accelerator Module (MAM) provides accelerated execution from the on-chip flash at higher frequencies.

Problem:

If code is running from on-chip Flash, a write to an SRAM location followed by an immediate read from the same SRAM location corrupts the data been read. For instance, a stack push operation immediately followed by a stack pop operation.

Work-around:

User code should enable the MAM after Reset and before any RAM accesses; this means MAMTIM and MAMCR should be set as follows:

MAMTIM: For CPU clock frequencies slower than 20 MHz, set MAMTIM to 0x01. For CPU clock frequencies between 20 MHz and 40 MHz, set MAMTIM to 0x02, and for values above 40 MHz set MAMTIM to 0x03.

MAMCR: Set MAMCR to 0x02 (MAM functions fully enabled)

MAMTIM should be written before MAMCR.

3.3 MAM.2: Under certain conditions in MAM Mode 2 code execution out of internal Flash can fail

Introduction:

The MAM block maximizes the performance of the ARM processor when it is running code in Flash memory. It includes three 128-bit buffers called the Prefetch Buffer, the Branch Trail Buffer and the data buffer. It can operate in 3 modes; Mode 0 (MAM off), Mode 1 (MAM partially enabled) and Mode 2 (MAM fully enabled).

Problem:

Under certain conditions when the MAM is fully enabled (Mode 2) code execution from internal Flash can fail. The conditions under which the problem can occur is dependent on the code itself along with its positioning within the Flash memory.

Work-around:

If the above problem is encountered then Mode 2 should not be used. Instead, partially enable the MAM using Mode 1.

3.4 SPI.1: Incorrect shifting of data in slave mode at lower frequencies

Introduction:

In slave mode, the SPI can set the clock phase (CPHA) to 0 or 1.

Problem:

Consider the following conditions:

1. SPI is configured as a slave (with CPHA=0).
2. SPI is running at a low frequency.

In slave mode, the SPIF (SPI Transfer Complete Flag) bit is set on the last sampling edge of SCK. If CPHA is set to 0 then the last sampling edge of SCK would be the rising edge.

Under the above conditions, if the SPI Data Register (SPDR) is written to less than a half SCLK cycle after the SPIF bit is set (this would happen if the SPI frequency is low) then the SPDR will shift data one clock early for the upcoming transfers.

Lowering the SPI frequency would increase the likelihood of the SPDR write happening in the first half SCK cycle of the last sampling clock.

Work-around:

There are two possible workarounds:

1. Use CPHA=1.
2. If the data is shifted incorrectly when CPHA is set to 0 then delaying the write to SPDR after the half SCK cycle of the last sampling clock would resolve this issue.

3.5 SSP.1: Initial data bits/clocks of the SSP transmission are shorter than subsequent pulses at higher frequencies

Introduction:

The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI or a Microwire bus. The SSP can operate at a maximum speed of 30MHz and it referred to as SPI1 in the device documentation.

Problem:

At high SSP frequencies, it is found that the first four pulses are shorter than the subsequent pulses.

At 30 MHz, the first pulse can be expected to be approximately 10 ns shorter and the second pulse around 5 ns shorter. The remaining two pulses are around 2 ns shorter than subsequent pulses.

At 25 MHz, the length of the first pulse would be around 7 ns shorter. The subsequent three pulses are around 2 ns shorter.

At 20 MHz only the first pulse is affected and it is around 2 ns shorter. All subsequent pulses are fine.

The deviation of the initial data bits/clocks will decrease as the SSP frequency decreases.

Work-around:

None.

3.6 Timer.1: In counter mode, the Timer Counter reset does not occur on the correct incoming edge

Introduction:

Timer0 and Timer1 can be used in a counter mode. In this mode, the Timer Counter register can be incremented on rising, falling or both edges which occur on a selected CAP input pin.

This counter mode can be combined with the match functionality to provide additional features. One of the features would be to reset the Timer Counter register on a match. The same would also apply for Timer1.

Problem:

The Timer Counter reset does not trigger on the same incoming edge when the match takes place between the corresponding Match register and the Timer Counter register. The Timer Counter register will be reset only on the next incoming edge.

Work-around:

There are two possible workarounds:

1. Combine the Timer Counter reset feature with the “interrupt on match” feature. The interrupt on match occurs on the correct incoming edge. In the ISR, the Timer Counter register can also be reset. This solution can only work if no edges are expected during the duration of the ISR.
2. In this solution, the “interrupt on match” feature is not used. Instead, the following specific initialization can achieve the counting operation:
   a. Initialize the Timer Counter register to 0xFFFFFFFF.
   b. If “n” edges have to be counted then initialize the corresponding Match register with value n-1. For instance, if 2 edges need to be counted then load the Match register with value 1.

More details on the above example:

1. Edge 1 - Timer overflows and Timer Counter (TC) is set to 0.
2. Edge 2 - TC = 1. Match takes place.
3. Edge 3 - TC = 0.
4. Edge 4 - TC = 1. Match takes place.
5. Edge 5 - TC = 0.

3.7 Vdd.1: Device may not work properly under increased power consumption conditions

Introduction:

From the Vdd1V8 pin to the ARM7 core, there is a voltage drop. This voltage drop increases with higher currents (or higher power consumption). Higher system frequency and/or faster peripherals increase power consumption thereby increasing the voltage drop from the Vdd1V8 pin to the core.

Problem:

Under increased power consumption conditions, the device may not work properly. The likelihood of the problem showing up increases if the device is run at higher speeds (approaching 70MHz) and/or if the peripherals are running at close to system frequency speed (i.e If the APBDIV register is set to a value lower than 4 which would imply that the peripherals are run faster than 1/4 of the system frequency).

Also, having a lower voltage on Vdd1V8 pin (e.g. below 1.8 V) can cause this issue to surface.

Work-around:

Increase the voltage on Vdd1V8 to 1.95 V. It is not harmful to the device if this voltage reaches 2 V.

3.8 I2C1.1: I2C1 pins are not bi-directional GPIO pins

Introduction:

There are two I2C interfaces, I2C0 and I2C1. I2C0 functions are shared as alternate functions on port pins P0.2 and P0.3. I2C1 functions are shared on port pins P0.17 and P0.18.

Problem:

I2C1 pins are currently open-drain output pins but they should be regular bi-directional GPIO pins. I2C0 pins are configured as open-drain output pins (for I2C bus compliance).

Work-around:

None.

3.9 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START	When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
	000	No start (this value should be used when clearing PDN to 0).	
	001	Start conversion now.	
	010	Start conversion when the edge selected by bit 27 occurs on P0.16/EINT0/MAT0.2 pin.	
	011	Start conversion when the edge selected by bit 27 occurs on P0.22.	
	100	Start conversion when the edge selected by bit 27 occurs on MAT0.1.	
	101	Start conversion when the edge selected by bit 27 occurs on MAT0.3.	
	110	Start conversion when the edge selected by bit 27 occurs on MAT1.0.	
	111	Start conversion when the edge selected by bit 27 occurs on MAT1.1.	

Fig 1. A/D control register options

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P0.16 or P0.22 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing an ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 72 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

4. AC/DC deviations detail

4.1 ESD.1: The device does not meet the 2 kV ESD requirements on the RTCX1 pin

Introduction:

The LPC2103 is rated for 2 kV ESD.The RTCX1 pin is the input pin for the RTC oscillator circuit.

Problem:

The LPC2103 does not meet the required 2 kV ESD specified.

Work-around:

Observe proper ESD handling precautions for the RTCX1 pin.

4.2 VBAT.1: Increased power consumption on the VBAT pin when the VDD(1V8) core pin is left floating

Introduction:

The LPC2103 has a VDD(1V8) core pin which provides power to the internal circuitry and also, has a VBAT pin which provides power only to the RTC (Real Time Clock). VBAT pin can be to an external battery or to the 3.3 V I/O port supply (VDD(3V3) pin) used by the device.

Problem:

When the VDD(1V8) core pin is floated, power consumption increases on the VBAT pin.

Work-around:

VDD(1V8) core pin must always be connected to its power supply or to ground.

5. Errata notes detail

5.1 n/a

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

7. Contents

1 Product identification 3
2 Errata overview 3
3 Functional problems detail 4
3.1 Core.1: Incorrect update of the Abort Link register in Thumb state 4
Introduction: 4
Problem: 4
Work-around: 4
3.2 MAM.1: Incorrect read of data from SRAM after Reset and MAM is not enabled or partially enabled 5
Introduction: 5
Problem: 5
Work-around: 5
3.3 MAM.2: Under certain conditions in MAM Mode 2 code execution out of internal Flash can fail . . 5
Introduction: 5
Problem: 5
Work-around: 5
3.4 SPI.1: Incorrect shifting of data in slave mode at lower frequencies 6
Introduction: 6
Problem: 6
Work-around: 6
3.5 SSP.1: Initial data bits/clocks of the SSP transmission are shorter than subsequent pulses at higher frequencies 7
Introduction: 7
Problem: 7
Work-around: 7
3.6 Timer.1: In counter mode, the Timer Counter reset does not occur on the correct incoming edge. . 8
Introduction: 8
Problem: 8
Work-around: 8
3.7 Vdd.1: Device may not work properly under increased power consumption conditions. 9
Introduction: 9
Problem: 9
Work-around: 9
3.8 I2C1.1: I2C1 pins are not bi-directional GPIO pins 9
Introduction: 9
Problem: 9
Work-around: 9
3.9 ADC.1: External sync inputs not operational . 10
Introduction: 10
Problem: 10
Work-around: 10
4 AC/DC deviations detail 11
4.1 ESD.1: The device does not meet the 2 kV ESD requirements on the RTCX1 pin. 11
Introduction: 11
Problem: 11
Work-around: 11
4.2 VBAT.1: Increased power consumption on the VBAT pin when the VDD(1V8) core pin is left floating 11
Introduction: 11
Problem: 11
Work-around: 11
5 Errata notes detail 11
5.1 n/a 11
6 Legal information 12
6.1 Definitions 12
6.2 Disclaimers 12
6.3 Trademarks 12
7 Contents 13

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1 March 2011
Document identifier: ES_LPC2103