ES_LPC2131/01

Errata sheet LPC2131/01

Rev. 2.1 — 1 May 2012

Errata sheet

Document information

Info	Content
Keywords	LPC2131FBD64/01, LPC2131/01 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.
	Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
2.1	20120501	• Added Rev F.
2	20110301	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added ADC.1
1.3	20090209	• Added Rev E.
1.2	20080607	• Added WDT.1. • Added table for errata notes. • Added Errata Note 2.
1.1	20070608	• Added MAM.1. • Added ESD.1.
1	20060830	• Initial version.

Contact information

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1. Product identification

The LPC2131/01 devices typically have the following top-side marking:

LPC2131xxx

/01

xxxxxxx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2131/01:

Table 1.   Revision overview table

Revision identifier	Revision description
'C'	First device revision
'D'	Second device revision
'E'	Third device revision
'F'	Fourth device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2.   Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
Core.1	Incorrect update of the Abort link register	'C', 'D', 'E', 'F'	Section 3.1
Timer.1	Timer Counter reset occurs on incorrect edge in counter mode	'C', 'D'	Section 3.2
SSP.1	Initial data bits/clocks corrupted in SSP transmission	'C', 'D', 'E', 'F'	Section 3.3
DC/DC.1	DC/DC Converter start-up issue	'C'	Section 3.4
MAM.1	Code execution failure can occur with MAM Mode 2	'C', 'D'	Section 3.5
WDT.1	Accessing non-Watchdog APB registers in the middle of the feed sequence causes a reset	'D'	Section 3.6
ADC.1	External sync inputs not operational	'C', 'D', 'E', 'F'	Section 3.7

Table 3.   AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
ESD.1	ESD weakness on RTCX1 pin	'C', 'D'	Section 4.1

Table 4.   Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note 1	Port pin P0.31 must not be driven low during reset.	'C', 'D', 'E', 'F'	Section 5.1
Note 2	When the input voltage is Vi ≥ Vdd I/O + 0.5 v on port pin P0.25 (configured as general purpose input pin), current must be limited to less than 4 mA by using a series limiting resistor.	'C', 'D', 'E', 'F'	Section 5.2

3. Functional problems detail

3.1 Core.1: Incorrect update of the Abort Link register in Thumb state

Introduction:

If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem:

In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work-around:

In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this would have to be done manually.

3.2 Timer.1: In counter mode, the Timer Counter reset does not occur on the correct incoming edge

Introduction:

Timer0 and Timer1 can be used in a counter mode. In this mode, the Timer Counter register can be incremented on rising, falling or both edges which occur on a selected CAP input pin.

This counter mode can be combined with the match functionality to provide additional features. One of the features would be to reset the Timer Counter register on a match. The same would also apply for Timer1.

Problem:

The Timer Counter reset does not trigger on the same incoming edge when the match takes place between the corresponding Match register and the Timer Counter register. The Timer Counter register will be reset only on the next incoming edge.

Workaround:

There are two possible workarounds:

1. Combine the Timer Counter reset feature with the "interrupt on match" feature. The interrupt on match occurs on the correct incoming edge. In the ISR, the Timer Counter register can also be reset. This solution can only work if no edges are expected during the duration of the ISR.

2. In this solution, the "interrupt on match" feature is not used. Instead, the following specific initialization can achieve the counting operation:

   a. Initialize the Timer Counter register to 0xFFFFFFFF.

   b. If "n" edges have to be counted then initialize the corresponding Match register with value n-1. For instance, if 2 edges need to be counted then load the Match register with value 1.

More details on the above example:

1. Edge 1 - Timer overflows and Timer Counter (TC) is set to 0.
2. Edge 2 - TC = 1. Match takes place.
3. Edge 3 - TC = 0.
4. Edge 4 - TC = 1. Match takes place.
5. Edge 5 - TC = 0.

3.3 SSP.1: Initial data bits/clocks of the SSP transmission are shorter than subsequent pulses at higher frequencies

Introduction:

The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI or a Microwire bus. The SSP can operate at a maximum speed of 30 MHz and is referred to as SPI1 in the device documentation.

Problem:

At high SSP frequencies, it is found that the first four pulses are shorter than the subsequent pulses.

At 30 MHz, the first pulse can be expected to be approximately 10 ns shorter and the second pulse around 5 ns shorter. The remaining two pulses are around 2 ns shorter than subsequent pulses.

At 25 MHz, the length of the first pulse would be around 7 ns shorter. The subsequent three pulses are around 2 ns shorter.

At 20 MHz only the first pulse is affected and it is around 2 ns shorter. All subsequent pulses are fine.

The deviation of the initial data bits/clocks will decrease as the SSP frequency decreases.

Work-around:

None.

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3.4 DC/DC.1: DC/DC converter start-up issue

Introduction:

The device operating voltage range is 3.0 V to 3.6 V and it is an internal DC/DC converter that provides 1.8 V to the ARM7 Core.

Problem:

If during a power-on reset the voltage on Vdd takes longer than 200 ms to ramp from below 0.8 V to above 2.0 V, the chip-internal DC/DC converter might not start up correctly. If this happens, the crystal oscillator will not be running, resulting in no code execution. As an example, having a Vdd rise time of less than 10 V/s might trigger this problem.

The same problem might occur during a supply voltage drop during which Vdd remains between 300 mV and 80 mV for more than 200 ms before going back to the specified Vdd level. As an example, having a residual battery voltage of less than 0.3 V but more than 0.08 V in a rechargeable battery application might trigger this problem when the charger providing the 3 V supply is being connected.

Work-around:

Apply another power-on Reset during which Vdd rises from below 0.8 V to above 2.0 V in less than 200 ms.

3.5 MAM.1: Under certain conditions in MAM Mode 2 code execution out of internal Flash can fail

Introduction:

The MAM block maximizes the performance of the ARM processor when it is running code in Flash memory. It includes three 128-bit buffers called the Prefetch Buffer, the Branch Trail Buffer and the data buffer. It can operate in 3 modes; Mode 0 (MAM off), Mode 1 (MAM partially enabled) and Mode 2 (MAM fully enabled).

Problem:

Under certain conditions when the MAM is fully enabled (Mode 2) code execution from internal Flash can fail. The conditions under which the problem can occur is dependent on the code itself along with its positioning within the Flash memory.

Work-around:

If the above problem is encountered then Mode 2 should not be used. Instead, partially enable the MAM using Mode 1.

3.6 WDT.1: Accessing non-Watchdog APB registers during the feed sequence causes a reset

Introduction:

The Watchdog timer can reset the microcontroller within a reasonable amount of time if it enters an erroneous state.

Problem:

After writing 0xAA to WDFEED, any APB register access other than writing 0x55 to WDFEED may cause an immediate reset.

Work-around:

Avoid APB accesses in the middle of the feed sequence. This implies that interrupts and the GPDMA should be disabled while feeding the Watchdog.

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3.7 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADCs can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		000	No start (this value should be used when clearing PDN to 0).	
		001	Start conversion now.	
		010	Start conversion when the edge selected by bit 27 occurs on P0.16/EINT0/MAT0.2/CAP0.2 pin.	
		011	Start conversion when the edge selected by bit 27 occurs on P0.22/AD1.7/CAP0.0/MAT0.0 pin.	
		100	Start conversion when the edge selected by bit 27 occurs on MAT0.1.	
		101	Start conversion when the edge selected by bit 27 occurs on MAT0.3.	
		110	Start conversion when the edge selected by bit 27 occurs on MAT1.0.	
		111	Start conversion when the edge selected by bit 27 occurs on MAT1.1.	

Fig 1.   A/D control register options

Problem:

The external start conversion feature, ADxCR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P0.16 or P0.22 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing an ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 60 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

4. AC/DC deviations detail

4.1 ESD.1: The device does not meet the 2 kV ESD requirements on the RTCX1 pin

Introduction:

The LPC2131/01 is rated for 2 kV ESD. The RTCX1 pin is the input pin for the RTC oscillator circuit.

Problem:

The LPC2131/01 does not meet the required 2 kV ESD specified.

Work-around:

Observe proper ESD handling precautions for the RTCX1 pin.

5. Errata notes detail

5.1 Note.1

Port pin P0.31 must not be driven low during reset. If low on reset the device behavior is undetermined.

5.2 Note.2

On port pin P0.25 (when configured as general purpose input pin), leakage current increases when the input voltage is $V_i \geq$ Add I/O + 0.5 V. Care must be taken to limit the current to less than 4 mA by using a series limiting resistor.

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