ES_LPC82x

Errata sheet LPC82x

Rev. 1.4 — 13 April 2022 Errata sheet

Document information

Info	Content
Keywords	LPC824M201JHI33; LPC822M101JHI33; LPC824M201JDH20; LPC822M101JDH20; LPC82x errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
1.4	20220104	• Added BOD.1 details in Section 5 “Errata notes”. • Added ‘1B’ in Table 1 “Device revision table” and Table 2 “Functional problems table”.
1.3	20180403	Added VDD.1
1.2	20180301	Added CMP.1
1.1	20151118	Added text to the work-around of DPD.2 for clarity in Section 3.1: Deep power-down mode operates correctly for the entire temperature range (-40 °C to 105 °C) if the VDD supply is between 1.8 V and 3.35 V.
1	20140918	Initial version

Contact information

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1. Product identification

The LPC82x devices typically have the following top-side marking:

The LPC82x devices typically have the following top-side marking for HVQFN33 packages:

82xJ

xxxx xxxx

yywwxR

The last two letters in the last line (field 'xR') identify the boot code version and device revision.

Table 1. Device revision table

Revision identifier (xR)	Revision description
'1A'	Initial device revision
'1B'	Second device revision

Field 'yy' states the year the device was manufactured. Field 'ww' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
DPD.2	Deep power-down mode is not functional outside certain voltage and temperature ranges.	'1A', 1B'	Section 3.1
SYSOSC.2	When using an external crystal oscillator, the V_{DD} supply voltage must be 1.9 V or above.	'1A', 1B'	Section 3.2
UART.1	The UART controller sets the Idle status bits for receive and transmit before the transmission of the stop bit is complete.	'1A', 1B'	Section 3.3
CMP.1	PIO0_21 cannot be used as GPIO output port when enabling ACMP_I4 function on PIO0_23 pin port pin.	'1A', 1B'	Section 3.4
VDD.1	The minimum wait time of the power supply ramp must be minimum 2 ms.	'1A', 1B'	Section 3.5

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Detailed description
n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Detailed description
BOD.1	Brown-out detect (BOD) peripheral (reset and interrupt) is not functional for temperatures below -20 °C for 0.4% of the parts.	Section 5.1

3. Functional problems detail

3.1 DPD.2

Introduction:

The LPC82x has a supply voltage (V_{DD}) from 1.8 V to 3.6 V and can operate from -40 °C to 105 °C. The LPC82x supports four reduced power modes (sleep, deep-sleep, power-down, and deep power-down mode). Deep power-down mode allows for maximal power savings where the entire system is shut down except for the general purpose registers in the PMU and the self wake-up timer. Only the general purpose registers in the PMU maintain their internal states in deep power-down mode.

Problem:

At temperatures ≤ 25 °C, the deep power-down mode is not functional if the V_{DD} supply voltage is > 3.4 V. At temperatures > 25 °C, the deep power-down mode is not functional if the V_{DD} supply voltage is > 3.35 V.

Work-around:

Deep power-down mode operates correctly for the entire temperature range (-40 °C to 105 °C) if the VDD supply is between 1.8 V and 3.35 V. For temperatures ≤ 25 °C, ensure that the supply voltage is not > 3.4 V (V_{DD} = 1.8 V to 3.4 V) when using deep power-down mode. For temperatures > 25 °C, ensure that the supply voltage is not > 3.35 V (V_{DD} = 1.8 V to 3.35 V) when using deep power-down mode.

3.2 SYSOSC.1

Introduction:

On the LPC82xM, the V_{DD} supply voltage range is from 1.8 V to 3.6 V. The LPC82xM has various clock sources such as the internal oscillator (IRC), system oscillator, CLKIN, and watchdog oscillator.

An external crystal oscillator can be connected between the XTALIN and XTALOUT pins to use the system oscillator as a clock source. The system oscillator can also be bypassed by setting the BYPASS bit in the SYSOSCCTRL register, and an external clock source can be fed directly to the XTALIN pin.

Problem:

An external crystal oscillator connected to the system oscillator does not function when the V_{DD} power supply is below 1.9 V.

Work-around:

The V_{DD} supply voltage must be 1.9 V or above when connecting an external crystal oscillator to the system oscillator. If the V_{DD} supply voltage is below 1.9 V, an external clock source can be fed to the XTALIN by bypassing the system oscillator or the other clock sources mentioned above can be used.

3.3 UART.1

Introduction:

In receive mode, the UART controller provides a status bit (the RXIDLE bit in the UART STAT register) to check whether the receiver is currently receiving data. If RXIDLE is set, the receiver indicates it is idle and does not receive data.

In transmit mode, the UART controller provides two status bits (TXIDLE and TXDISSTAT bits in the UART STAT register) to indicate whether the transmitter is currently transmitting data. The TXIDLE bit is set by the controller after the last stop bit has been transmitted. The TXDISSTAT bit is set by the controller after the transmitter has sent the last stop bit and has become fully idle following a transmit disable executed by setting the TXDIS bit in the UART CTRL register.

The status bits can be used to implement software flow control, but their setting does not affect normal UART operation.

Problem:

The RXIDLE bit is incorrectly set for a fraction of the clock cycle between the reception of the last data bit and the reception of the start bit of the next word, that is while the stop bit is received. RXIDLE is cleared at the beginning of the start bit.

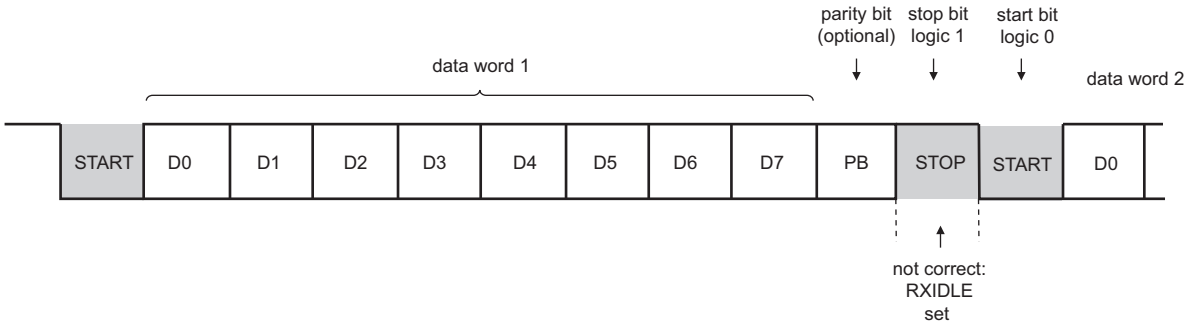

Fig 1. Incorrect setting of RXIDLE during UART receive

Both, TXIDLE and TXDISSTAT are set incorrectly between the last data bit and the stop bit while the transfer is still ongoing.

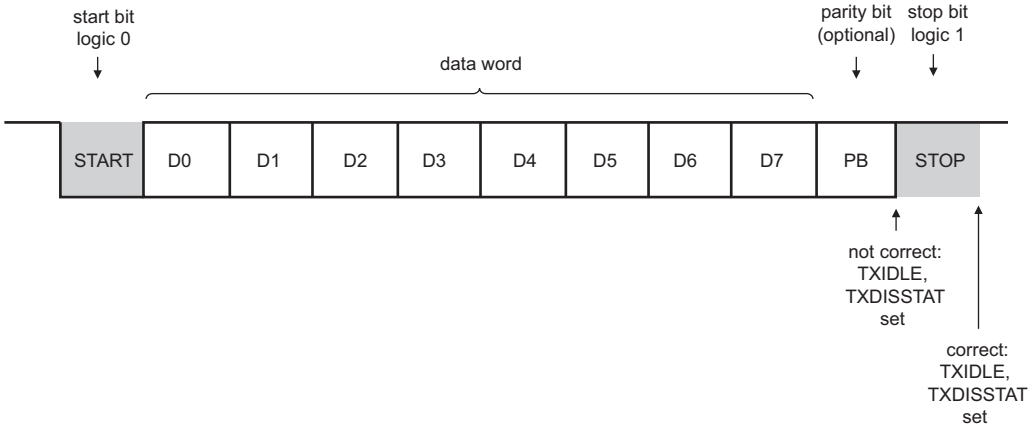

Fig 2. Incorrect setting of TXIDLE and TXDISSTAT during UART transmit

Work-around:

When writing code that checks for the setting of any of the status bits RXIDLE, TXIDLE, TXDISSTAT, check the value of the status bit in the STAT register:

- If status bit = 1, add a delay of one UART bit time (if STOPLEN = 0, one stop bit) or two bit times (if STOPLEN = 1, two stop bits) and check the value of the status bit again:
  - If status bit = 1, the receiver is idle.
  - If status bit = 0, the receiver is receiving data.
- If the status bit = 0, the receiver is receiving data.

3.4 CMP.1

Introduction:

On the LPC82x, the analog comparator has four input pins (ACMP_I[4:1]). These are fixed-pin functions and are associated with one bit in the PINENABLE0 register that selects or deselects the comparator input function.

Problem:

When the ACMP_I4 function is enabled on port pin PIO0_23 pin, port pin PIO0_21 cannot be used as GPIO output port. Also, to use the ACMP_I4 function, the port pin PIO0_23 must not be configured as GPIO output.

Work-around:

No work-around.

3.5 VDD.1

Introduction:

On the LPC82x, the V_{DD} supply voltage range is from 1.8 V to 3.6 V. The LPC82x datasheet specifies a power-up ramp condition for the user application. Before ramping up, the minimum wait time (t_{wait}) of the power supply on the V_{DD} pin (200 mV or below) is 12 μs.

Problem:

The device might not always start-up if the minimum wait time (t_{wait}) is 12 μs. The required minimum time (t_{wait}) specification is 2 ms.

Work-around:

None.

4. AC/DC deviations detail

n/a

5. Errata notes

5.1 BOD.1

Brown-out detect (BOD) peripheral (reset and interrupt) is not functional for temperatures below -20 °C for 0.4% of the parts. No workaround on device revision '1A'. Issue is fixed on '1B'.

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