Mask Set Errata for Mask 0N63P

This report applies to mask 0N63P for these products:

- MKV11Z128Vxx7, MKV11Z64Vxx7
- MKV10Z128Vxx7, MKV10Z64Vxx7

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
e8992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
e7352	DSPI: reserved bits in slave CTAR are writable
e50117	FAC: Execute-only access control feature has been deprecated
e8341	FlexCAN: Entering Freeze Mode or Low Power Mode from Normal Mode can cause the FlexCAN module to stop operating.
e10028	FTFA: For MCUs prior to work week 14 of 2016, FSEC[MEEN] = 10 disables Mass Erase only when the MCU is secured
e8010	LLWU: CMP flag in LLWU_Fx register cleared by multiple CMP out toggles when exiting LLSx or VLLSx modes.
e6395	MCG: Fast IRC Fine Trim bit is not used by the MCG Auto Trim Machine
e7993	MCG: FLL frequency may be incorrect after changing the FLL reference clock
e7735	MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock
e4647	UART: Flow control timing issue can result in loss of characters if FIFO is not enabled
e2580	UART: Start bit sampling not compliant with LIN 2.1 specification

Table 2. Revision History

Revision	Changes
08 Apr 2015	Initial revision
11 July 2019	The following errata were added. • e50117 • e10028

e8992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Description: Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

Workaround: There are two workarounds:

1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.

2) Assert NMI signal for longer than 16 bus clock cycles.

e7352: DSPI: reserved bits in slave CTAR are writable

Description: When the Deserial/Serial Peripheral Interface (DSPI) module is operating in slave mode (the Master [MSTR] bit of the DSPI Module Configuration Register [DSPIx_MCR] is cleared), bits 10 to 31 (31 = least significant bit) of the Clock and Transfer Attributes Registers (DSPIx_CTARx) should be read only (and always read 0). However, these bits are writable, but setting any of these bits to a 1 does not change the operation of the module.

Workaround: There are two possible workarounds.

Workaround 1: Always write zeros to the reserved bits of the DSPIx_CTARn_SLAVE (when operating in slave mode).

Workaround 2: Mask the reserved bits of DSPIx_CTARn_SLAVE when reading the register in slave mode.

e50117: FAC: Execute-only access control feature has been deprecated

Description: The FAC feature is no longer recommended for use.

Workaround: Do not program the XACCn registers to use the FAC feature.

e8341: FlexCAN: Entering Freeze Mode or Low Power Mode from Normal Mode can cause the FlexCAN module to stop operating.

Description: In the Flexible Controller Area Network (FlexCAN) module, if the Freeze Enable bit (FRZ) in the Module Configuration Register (MCR) is asserted and the Freeze Mode is requested by asserting the Halt bit (HALT) in MCR, in some cases, the Freeze Mode Acknowledge bit (FRZACK) in the MCR may never be asserted.

In addition, the Low-Power Mode Acknowledge bit (LPMACK) in the MCR may never be asserted in some cases when the Low-Power Mode is requested.

Under the two scenarios described above, the loss of ACK assertion (FRZACK, LPMACK) causes a lock condition. A soft reset action is required in order to remove the lock condition.

The change from Normal Mode to Low-Power Mode cannot be done directly. Instead, first change mode from Normal to Freeze Mode, and then from Freeze to Low-Power Mode.

Workaround: To avoid the lock condition, the following procedures must be used:

A) Procedure to enter in Freeze Mode:

1. Set both the Freeze Enable bit (FRZ) and the Halt bit (HALT) in the Module Control Register (MCR).

2. Check if the Module Disable bit (MDIS) in MCR register is set. If yes, clear the MDIS bit.

3. Poll the MCR register until the Freeze Mode Acknowledge bit (FRZACK) in MCR is set or the timeout is reached (see NOTE below).

4. If the Freeze Mode Acknowledge bit (FRZACK) is set, no further action is required. Skip steps 5 to 8.

5. If the timeout is reached because the Freeze Mode Acknowledge bit (FRZACK) is still cleared, then set the Soft Reset bit (SOFTRST) in MCR.

6. Poll the MCR register until the Soft Reset bit (SOFTRST) bit is cleared.

7. Reconfigure the Module Control Register (MCR)

8. Reconfigure all the Interrupt Mask Registers (IMASKn).

After Step 8, the module will be in Freeze Mode.

NOTE: The minimum timeout duration must be equivalent to:

a) 730 CAN bits if the CAN FD Operation Enable bit (FDEN) in MCR is set (CAN bits calculated at arbitration bit rate),

b) 180 CAN bits if the FDEN bit is cleared.

B) Procedure to enter in Low-Power Mode:

1. Enter in Freeze Mode (execute the procedure A).

2. Request the Low-Power Mode.

3. Poll the MCR register until the Low-Power Mode Acknowledge (LPMACK) bit in MCR is set.

e10028: FTFA: For MCUs prior to work week 14 of 2016, FSEC[MEEN] = 10 disables Mass Erase only when the MCU is secured

Description: MCUs manufactured prior to work week 14 of 2016 do not have the following features:

1) FSEC[MEEN] = 10 disables Mass Erase in all MCU operations including

a) debug mode using MDM-AP

b) EZPORT

c) internal Erase all block commands

2) Flash commands

a) 0x4A Read 1s All Execute only Segments

b) 0x4B Erase All Execute-only Segments

Workaround: If these features are required, please obtain MCUs manufactured during work week 14 of 2016 or later.

Read the Flash Version ID via the Read Resource Flash command or look at the date code marked on the device to confirm the availability of the features referenced above.

- Flash Version ID 08.01.02.00 indicates the features are available.
- Date Code 1614 (YYWW) or EN (YW) and later indicates the features are available.

Note: The last line marked on the part contains the date code.

- For parts with 8 characters on the last line, the date code is characters 4-7
- For parts with 6 characters on the last line, the date code is characters 4-5
- For parts with 5 characters on the last line, the date code is characters 3-4

e8010: LLWU: CMP flag in LLWU_Fx register cleared by multiple CMP out toggles when exiting LLSx or VLLSx modes.

Description: The comparator's corresponding wakeup flag in the LLWU_Fx register is cleared prematurely if:

1.The CMP output is toggled more than one time during the LLSx wakeup sequence and the comparator's corresponding flag in the LLWU_Fx register is cleared.

Or

2.The CMP output is toggled more than one time during the VLLSx wakeup sequence, PMC_REGSC[ACKISO] is cleared, and the comparator's corresponding flag in the LLWU_Fx register is cleared.

Workaround: When MCU is waking up from LLS, code can implement a software flag to retain the wakeup source, if required by software.

When MCU is waking up from VLLSx, code can implement a software flag prior to clearing PMC_REGSC[ACKISO] to retain the wakeup source, if required by software.

e6395: MCG: Fast IRC Fine Trim bit is not used by the MCG Auto Trim Machine

Description: The Fast IRC fine trim bit, MCG_C2[FCFTRIM], is not used by the Auto Trim Machine. This means that when the Auto Trim Machine is used to set the Fast IRC frequency, it will not be trimmed with the finest resolution. If the finer resolution is required, the MCG_C2[FCFTRIM] bit must be manually changed and the resulting fast IRC frequency must then be measured to determine whether this bit should be set or cleared to be closest to the target frequency.

Workaround: If the finest resolution of the Fast IRC trim is not required, then no workaround is required. However, if the finest resolution is required, the following steps must be performed:

1) After the auto trim machine has completed running, measure the Fast IRC frequency.

2) Clear the MCG_C2[FCFTRIM] and re-measure the Fast IRC frequency.

3) Determine which value of MCG_C2[FCFTRIM] provided the closest frequency to the desired target frequency.

4) Store the MCG_C4[FCTRIM] and MCG_C2[FCFTRIM] values in a suitable flash location. Refer to the individual device reference manual for the recommended flash location.

e7993: MCG: FLL frequency may be incorrect after changing the FLL reference clock

Description: When the FLL reference clock is switched between the internal reference clock and the external reference clock, the FLL may jump momentarily or lock at a higher than configured frequency. The higher FLL frequency can affect any peripheral using the FLL clock as its input clock. If the FLL is being used as the system clock source, FLL Engaged Internal (FEI) or FLL Engaged External (FEE), the maximum system clock frequency may be exceeded and can cause indeterminate behavior.

Only transitions from FLL External reference (FBE, FEE) to FLL Internal reference (FBI, FEI) modes and vice versa are affected. Transitions to and from BLPI, BLPE, or PLL clock modes (if supported) are not affected because they disable the FLL. Transitions between the external reference modes or between the internal reference modes are not affected because the reference clock is not changed.

Workaround: To prevent the occurrence of this jump in frequency either the MCG_C4[DMX32] bit must be inverted or the MCG_C4[DRST_DRS] bits must be modified to a different value immediately before the change in reference clock is made and then restored back to their original value after the MCG_S[IREFST] bit reflects the selected reference clock.

If you want to change the MCG_C4[DMX32] or MCG_C4[DRST_DRS] to new values along with the reference clock, the sequence described above must be performed before setting these values to the new value(s).

e7735: MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock

Description: When transitioning from MCG clock modes FBE or FEE to either FBI or FEI, the MCG_S[IREFST] bit will set to 1 before the IREFS clock multiplexor has actually selected the slow IRC as the reference clock. The delay before the multiplexor actually switches is:

2 cycles of the slow IRC + 2 cycles of OSCERCLK

In the majority of cases this has no effect on the operation of the device.

Workaround: In the majority of applications no workaround is required. If there is a requirement to know when the IREFS clock multiplexor has actually switched, and OSCERCLK is no longer being used by the FLL, then wait the equivalent time of:

2 cycles of the slow IRC + 2 cycles of OSCERCLK

after MCG_S[IREFST] has been set to 1.

e4647: UART: Flow control timing issue can result in loss of characters if FIFO is not enabled

Description: On UARTx modules with FIFO depths greater than 1, when the /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit

and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

Workaround: Always enable the RxFIFO if you are using flow control for UARTx modules with FIFO depths greater than 1. The receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

Note that only UARTx modules with FIFO depths greater than 1 are affected. The UARTs that do not have the RxFIFO feature are not affected. Check the Reference Manual for your device to determine the FIFO depths that are implemented on the UARTx modules for your device.

e2580: UART: Start bit sampling not compliant with LIN 2.1 specification

Description: The LIN 2.1 specification states that start bits should be checked at sample 7, 8, 9, and 10. The UART module checks the start bit at samples 3, 5, and 7 instead.

Workaround: Start bits longer than 5/16 of a bit time are guaranteed to be recognized. Start bits shorter than this should not be used with this version of the UART because they might not be recognized.

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