Mask Set Errata for Mask 0N16X

This report applies to mask 0N16X for these products:

- MKE1xZ64Vxx4
- MKE1xZ32Vxx4

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR010888	Core: Processor accesses to the I/O port during exception stacking can report incorrect privilege
ERR010364	LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer
ERR010752	LPI2C: Slave Busy Flag may incorrectly read as zero when 10-bit address mode enabled in slave mode.
ERR010792	LPI2C: Slave Transmit Data Flag may incorrectly read as one when TXCFG is zero.
ERR011097	LPSPI: Command word not loaded correctly when TXMSK=1
ERR011089	LPSPI: In Continuous transfer mode with CPHA =1, WCF bit is not set for every word.
ERR010527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters
ERR010656	LPUART: The RXD Pin Active Edge Interrupt flag does not assert when an active edge is detected

Table 2. Revision History

Revision	Changes
0	Initial revision
1	No changes to errata with this revision

ERR010888: Core: Processor accesses to the I/O port during exception stacking can report incorrect privilege

Description: Arm 852671: Processor accesses to the I/O port during exception stacking can report incorrect privilege

Affects: Cortex-M0+

Fault Type: System Category B

Fault Status: Present in: r0p0, r0p1 Open.

The Cortex-M0+ processor implements both an AHB-Lite master and a dedicated, low-latency I/O port. The I/O port includes side-band signaling (IOPRIV) to indicate whether a transaction originates from privileged or unprivileged code.

Due to this erratum, if the stack pointer corresponding to unprivileged code is positioned such that it lies at an address corresponding to the I/O port, a subsequent exception entry from, or return to said code erroneously results in the associated load/store of the XPSR being marked as privileged on the I/O port.

This erratum does not affect accesses to the AHB-Lite master port, or any debugger accesses. The value written to the location is limited to XPSR values corresponding to Thread mode. The value read from the location is discarded and not exposed to software.

Configurations affected

The processor and system must be configured to:

1) Include the I/O port (IOP parameter value 1).

2) Include User/Privilege support (USER parameter value 1, or MPU parameter value not 0).

3) Use IOPRIV to implement privilege sensitive peripherals on the I/O port interface.

Implications

The value of IOPRIV during the load/store of the XPSR erroneously indicates the transaction is privileged, when it should be marked as unprivileged. Systems using IOPRIV to implement protection on the I/O port can be subject to transactions generated by unprivileged code appearing as privileged transactions through unexpected use of the stack-pointer.

Workaround: If a system is using IOPRIV and implements an MPU, then the MPU can be configured to prohibit unprivileged accesses to the required location. If an MPU is not implemented, and IOPRIV is being used, then there is no workaround.

ERR010364: LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer

Description: If the transmit FIFO is empty at the end of a master receive transfer and the AUTOSTOP (MCFGR1[AUTOSTOP]) bit in the Master Configuration Register 1 is clear, the LPI2C master sends a STOP condition before the next repeated START condition.

Workaround: Use software or DMA to queue up the subsequent transfer in the transmit FIFO before the completion of the master-receive transfer.

ERR010752: LPI2C: Slave Busy Flag may incorrectly read as zero when 10-bit address mode enabled in slave mode.

Description: When operating in slave mode with 10-bit addressing enabled and an address match is detected on the first address byte, the Slave Busy Flag, SSR[SBF], may incorrectly read as zero.

Workaround: When using the LPI2C in slave mode when 10-bit addressing is enabled, and the SSR[SBF] bit is read as a one, then the flag is set. If it is read as a zero, it must be read a second time and this second read will be the correct state of the bit.

ERR010792: LPI2C: Slave Transmit Data Flag may incorrectly read as one when TXCFG is zero.

Description: When SCFGR1[TXCFG] = 0, the slave transmit data ready flag can incorrectly assert for one cycle.

Workaround: Set SCFGR1[TXCFG] = 1.

ERR011097: LPSPI: Command word not loaded correctly when TXMSK=1

Description: When the Transmit Command Register is written with TCR[TXMSK]=1 and the next write to the TX FIFO is another command, then the first command may not load correctly.

Workaround: When writing the Transmit Command Register with TCR[TXMSK]=1, wait for the TX FIFO to go empty (FSR[TXCOUNT] = 0) before writing another command to the Transmit Command Register.

ERR011089: LPSPI: In Continuous transfer mode with CPHA =1, WCF bit is not set for every word.

Description: When Transmit Command Register is written with TCR[CONT]=1 and TCR[CPHA]=1, SR[WCF] bit flag is not set after data is transferred. Therefore polling for SR[WCF] flag to identify if data has been sent can cause MCU to be stuck.

Workaround: When using continuous transfer mode TCR[CONT]=1 and TCR[CPHA]=1, do not use SR[WCF] flag to determine if data has been sent, fill up instead transmit FIFO with the following data without waiting for SR[WCF] flag to be set.

ERR010527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Description: When the LPUART transmitter is idle (LPUART_STAT[TC]=1), two break characters may be sent when using LPUART_CTRL[SBK] to send one break character. Even when LUART_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

Workaround: To queue a single break character via the transmit FIFO, set LPUART_DATA[FRETSC]=1 with data bits LPUART_DATA[T9:T0]=0.

ERR010656: LPUART: The RXD Pin Active Edge Interrupt flag does not assert when an active edge is detected

Description: The RXD Pin Active Edge Interrupt (LPUART_STAT[RXEDGIF]) flag in the LPUART Status Register should set when an active edge is detected and the Receiver Enable (LPUART_CTRL[RE]) bit in the LPUART Control Register is set. However, the LPUART_STAT[RXEDGIF] flag will only set if the RX Input Active Edge Interrupt Enable (LPUART_BAUD[RXEDGIE]) bit in the LPUART Baud Rate Register is also set. Note that LPUART_BAUD[RXEDGIE] enables the interrupt for the LPUART_STAT[RXEDGIF] flag.

Workaround: Set LPUART_BAUD[RXEDGIE] bit if using the LPUART_STAT[RXEDGIF] flag.

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