Document Number: MC34708ER
Rev. 9.0, 11/2013

MC34708, Silicon Errata

Introduction

Device Revision Identification

This errata document applies to the following devices:

Table 1. Silicon Revision

Package	Part Number	Silicon Revision	Part Marking	Die ID
13 x 13	MC34708VM	P2.4	MC34708VM	DA07N05D
8 x 8	MC34708VK	P2.4	MC34708VK	DA07N05D

Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTZW1025”). The date is coded as four numerical digits, where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1025” indicates the 25th week of the year 2010.

Device Part Number Prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MC prefix.

General Description

This errata document applies to the MC34708 data sheet.

Table 2. Definitions of Errata Severity

Errata Level	Meaning
High	Failure mode that severely inhibits the use of the device for all or a majority of intended applications.
Medium	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications.
Low	Unexpected behavior that does not cause significant problems for the intended applications of the device.
Enhancement	Improvement made to the device due to previously found issues on the design.

Table 3. Errata for the MC34708

Errata Number	Erratum	System Impact	Description
High Severity Level			
36	**Charger:** Charger function no longer supported	External charger required	Charger errata 20, 21, 24, 26, 27, 28, 29, 34, 19 are merged under this single errata. The charger functionality is no longer supported and therefore these prior errata are no longer applicable. **Workaround:** None. External charger recommended. **Fix Plan/Status:** No fix scheduled.
35	**Coulomb Counter:** Coloumb counter function no longer supported	Inaccurate readings on the coulomb counter registers by up to 50%	Coulomb counter accuracy may be off by up to 50% **Workaround:** None. If battery current sensing is required, a software solution using the ADC can be implemented. **Fix plan/Status:** No fix scheduled

Table 3. Errata for the MC34708 (Continued)

Errata Number	Erratum	System Impact	Description
9	**Power Control:** Thermal shutdown triggers when the ADCEN bit set	Part will shutdown	Thermal shutdown is triggered inadvertently when inserting or removing a charger with the ADCEN bit enabled. It can also be triggered by performing an ADC reading, if the charger voltage (VBUS) < battery voltage (V_{BATT} +600 mV). **Workarounds:** **Option 1 for silicon revisions prior to 2.4:** Disable thermal shutdown with the following steps. 1. Keep ICTEST low 2. Set bit 23 of the SW5_PWRSTAGE register to 1 a.Write to the ID register address 7(decimal), 0x08_00_00.(Note: Bits [11:0] are read only if a read back will not return all zeroes) b.Write to the SW5_PWRSTAGE register address 14(decimal), 0x80_00_7F. c.Write to the ID register address 7(decimal), 0x00_00_00. **Option 2 for silicon revision 2.4 (recommended):** Use THERM110, THERM120, THERM125 and THERM130 interrupts to determine when the die is getting hot, and take action to prevent the die from overheating by reducing the processor frequency and tasks that are running. To do this configure the ADC for a conversion (reading) using the following procedure: 1. Verify the ADC continuous read mode set ADCONT = 0. 2. Configure channels to read on ADC, and set ADSTART bit = 0, and ADEN bit =1 3. Mask off THERM110, THERM120, THERM125, THERM130 interrupts (by writing a one to the THERM110M, THERM120M, THERM125M, THERM130M bits). 4. Disable thermal foldback by setting THFB_EN = 0. 5. Trigger ADC reading by setting ADSTART bit = 1. 6. Wait for ADCDONEI bit = 1. 7. Read ADC channel results. 8. Clear ADCDONEI interrupt by writing a one to ADCDONEI bit. 9. Set ADEN and ADSTART bits = 0 (clears the THERM1xxS bits). 10. Clear THERM110, THERM120, THERM125, and THERM130 interrupt bits by writing a one to THERM110, THERM120, THERM125, and THERM130 interrupts (disregard these interrupts as they are triggered by the ADC thermal issue, disabling the ADC will revert the sense bits to where they should be). 11. Enable thermal interrupts by clearing the mask bit, set the THERM110M, THERM120M, THEM125M, and THERM130 bits to a zero. 12. Enable thermal fold back by setting THFB_EN = 1 (otherwise set THFB_EN=0). 13. Repeat steps 1-11 for **ALL** ADC conversions. **NOTE:** If the THERM130 interrupt is triggered, try to reduce the power dissipation in the system by reducing the processor frequency and the tasks that are running. If the THERM130S bit is still set after a few seconds, shutdown the PMIC and the system by bringing the WDI pin low. **Fix Plan/Status:** No fix scheduled

Table 3. Errata for the MC34708 (Continued)

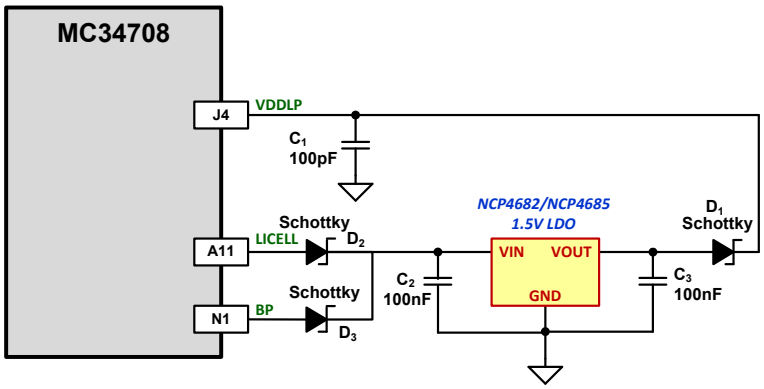
Errata Number	Erratum	System Impact	Description
High Severity Level			
23	**RTC:** V_{SRTC} drops out above 50 °C when V_{BATT} is ~2.2 V.	In applications with a Li-Ion battery, the RTC can be lost when the battery voltage drops to ~2.2 V. In applications where V_{BATT} is driven by an external source, the RTC can be lost as the voltage transitions below the 2.2 V range during power down.	There is an issue with the 'Best of Supply' switch, which powers VDDLP. During the change over from the primary power source to the coin cell, the VDDLP can dip to a voltage below the minimum voltage required to power the RTC. • The VSRTC supply is derived from VDDLP, and therefore affects the RTC of the application processor, as well as the on-board RTC • The 32 kHz clock to the processor's SRTC also drops out **Workaround:** Figure 1 is the application circuit recommended for all applications where the RTC is used with a back-up coin cell attached to the MC34708. The LDO output is set to 1.5 V with a Schottky diode in series which keeps the voltage supplied to VDDLP below the VCOREDIG (1.5 V). • Add a low quiescent current 1.5 V LDO, supplied by the coin cell (LICELL pin).Recommended LDO: NCP4682/4685 or equivalent with a 1uA typical Iq. • Add a low voltage Schottky diode (D1) to block the output capacitance (C3) of LDO. • Use Schottky diodes D2 and D3, to create a 'Diode-OR' connection on the input of the LDO. If the LICELL is always present in the system, the LDO input can be directly connected to the LICELL, therefore D2 and D3 are no longer needed. **Fix Plan/Status:** No fix scheduled
			 **Figure 1. RTC Workaround Application Circuit**
30	**Mini USB:** Wrong device type detection	A device that is attached to the USB may not be detected properly.	When a device is attached to the USB port the IC may detect the wrong device type. **Workaround:** When a USB device is detected, an attach interrupt will be generated. First clear the attach interrupt. Then issue a software reset to the mini USB by setting the RESET SPI bit in register 39 bit 4 to a one. The reset forces the mini USB module to go through the detection process again. When it has finished detecting the device, a new attach interrupt will be generated and the device type can be read via register 40. **Fix Plan/Status:** No Fix Scheduled

Table 3. Errata for the MC34708 (Continued)

Errata Number	Erratum	System Impact	Description
31	**LDO:** Current limit and SCP are no longer supported.	Current limit may not engage, thus current may exceed safe conditions. SCP may not turn off the LDO when a short circuit event is present.	The current limit is too high for all LDOs and therefore fails to engage. The short circuit protection (SCP) will fail to shut down LDO due to random variation of the shutdown timing. This behavior is present on all LDOs. **Workaround:** None. Recommended to keep REGSCPEN=0. **Fix plan/Status:** No fix scheduled
37	**Buck Regulator:** Regulator output undershoots in APS mode	Undershoot may violate processor's voltage requirements	In APS mode, the regulator output may undershoot for approximately 10 µs under transient loads of 1/2 of the max rated current. Output voltage may drop by as much as 160 mV. **Workaround:** SW1-5 must be operated in PFM mode for loads lower than 100 mA and in PWM mode for loads greater than 100 mA, in order to meet the transient load response specification. **Fix plan/Status:** No fix scheduled
38	**Power Up:** Part does not power up correctly at a high temperature (> 85 °C)	System may not startup correctly	When starting up with a high junction temperature, VCOREREF may be delayed in coming up, resulting in slow startup of all the regulators. Additionally, VSRTC may be stuck at a lower voltage. **Workaround:** See Figure 1. The 'Diode-OR' connection on the input of the LDO is optional. If LICELL is always present in the system, the LDO input can be directly connected to LICELL. **Fix plan/Status:** No fix scheduled
Medium Severity Level			
5	**Coin cell:** Extra current draw on coin cell	The coin cell will discharge faster when the battery voltage is between 1.2 V and 2.0 V.	The battery current spikes up to 212 mA, when BP is ~ 2.0 V (coin cell transition threshold) and the coin cell draws an extra 16 µA of current. **Workaround:** None **Fix Plan/Status:** No fix scheduled
8	**LDOs:** VREFDDR output accuracy out of spec	Output accuracy of VREFDDR is out of spec over temperature	VREFDDR output should be 2% accurate over temp. At 85 °C, the output accuracy of VREFDDR can go as high as 6.5%. **Workaround:** Use an external resistor divider to generate VREFDDR **Fix Plan/Status:** No fix scheduled
22	**ADC:** ADC readings with charger attached may be incorrect	ADC conversions can be incorrect when a charger is attached and the voltage on VBUS < VBATT + (600 to 800mV).	When a charger is attached and the voltage on VBUS < VBATT + (600 to 800mV), the ADC readings can be incorrect for all channels. **Note:** The channels which see the most offset are the battery current and the die temperature. **Workaround:** Use the thermal comparators THERM110, THERM120, THERM125 and THERM130 to determine when the part is heating up (See errata #9 for more information). **Fix Plan/Status:** No fix scheduled

Table 3. Errata for the MC34708 (Continued)

Errata Number	Erratum	System Impact	Description
39	**Startup:** False start and/or non-start of regulators	As BP begins its ramp up from between 100 mV and UVDET, either or both may occur: • the buck regulator outputs can momentarily glitch high • the buck regulators may not start up	When BP voltage falls below the BATT_TRKL voltage, a turn-off event occurs. When BP voltage is re-applied subsequently before the BP voltage falls below 100 mV, the turn-on event may not be recognized and regulator outputs may glitch while BP is ramping up. The above scenario can happen when BP is re-applied before the capacitors at BP have not discharged fully. **Workaround:** Design the regulator supplying BP such that its output is discharged to ground when disabled. This can be accomplished using bleeder resistors, if the supply does not have an active pull-down. **Fix Plan/Status:** No fix scheduled
40	**Incorrect CLK32K and CLK32KMCU Output**: Clock outputs not square. Falling edge may be step shaped.	Incorrect CLK32KMCU may cause system to hang. 2 to 5% of the units are affected.	When CLK32KVCC is higher than 2.0 V, ground bounce internal to the MC34708 can result in the CLK32K and CLK32KMCU outputs being step shaped. The issue does not occur when CLK32KVCC is below 2.0 V. **Workaround:** • Applications not using the CLK32K output: connect CLK32KVCC to ground. CLK32KMCU will continue to output 32 kHz clock pulses at the VSRTC level. • Applications using the CLK32K output: For CLK32K output level higher than 2.0 V, connect a 51 Ω resistor in series with the CLK32KVCC pin. The resistor should be connected between the CLK32KVCC pin and the bypass capacitor. For CLK32K output level lower than 2.0 V, no workaround is needed.
Low Severity Level			
25	**VBUS:** leakage path on VBUS	Additional 9.0 mA drawn from VBUS pin	There is a leakage path from VBUS pin that can be as high as 9.0 mA. This leakage is only present when the VBUS pin is used to detect the device attached at the USB connector. **Workaround:** None **Fix Plan/Status:** No fix scheduled
33	**SW4A/B:** Forced to PWM mode instead of APS mode	SW4A/B efficiency will be reduced.	When SW4A and SW4B are in independent configuration and one of the outputs is loaded, the unloaded channel SRFET allows negative current to flow in the inductor; this causes the unloaded regulator to be forced into PWM mode when it should be in APS mode. **Workaround:** None. **Fix Plan/Status:** No fix scheduled.

Table 4. Revision History

Revision	Date	Description of Changes
4.0	03/2012	• Modified erratum 9: workaround step 4, Data written on SW5_PWRSTAGE register changed to 0x80_00_7F. • Added High severity errata 23 and 24.
5.0	04/2012	• Added High severity errata 26, 27, 28, 29 and 30. • Added Low severity errata 25.
6.0	8/2012	• Silicon P2.5 removed from Table 1. Silicon Revision. • Removed P2.5 scheduled fixes for errata: 23, 25. • Charger errata is merge under new erratum 36. — Removed errata 20, 21, 24, 26, 27, 28, 29, 19. • Update errata: 9, 5, 22, and 25. • Added errata — High severity errata: 31, 35, 36. — Low severity errata: 33.
7.0	3/2013	• Added Errata - High severity errata: 37 and 38 • Added Errata - Medium severity errata: 39 • Updated errata 23
8.0	10/2013	• Updated errata 40
9.0	11/2013	• Redefined errata 39

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