56F8037/56F8027

Preliminary Chip Errata

56F8037/56F8027 Digital Signal Controller

This document reports errata information on chip revisions B and E. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number.

Chip Revisions B and E Errata Information:

The following errata items apply to revisions B and E 56F8037/56F8027 devices only.

Errata Number	Description	Impact and Workaround
1.0	In the DAC, the up/down-counter that implements waveform generation in automatic mode in the DAC gasket does not handle negative numbers.	Impact: Counting down to a negative number wraps the counter and continue counting down. Workaround: Adjust MAXVAL, MINVAL, and/or STEP size so the terminating value for the countdown is positive or zero.
2.0	The I^2C fails to detect arbitration loss when the loss occurs while the ACK bit of data bytes is received in master RX mode.	Impact: No impact on bus behavior. The arbitration loss software counters is not accurate in this situation. Workaround: None available.
3.0	Some I^2C slave TX FIFO flushes do not interrupt the CPU.	Impact: If the number of bytes written to the TX FIFO exceeds the number of data bytes retrieved by the remote master, there is no CPU indication that the excess data bytes were flushed from the TX FIFO. The software must accommodate this behavior. Workaround: None available.
4.0	The I^2C ACKs its own address and data during general calls when master and slave are enabled and the module initiates the general call. This means the transmission will always be completed and it is impossible to determine if another device is ACKing the call.	Impact: Because the module always ACKs the general call address and data in the scenario, the module never knows if any of the other nodes issued a NACK to the general call. Workaround: Disable slave mode prior to initiating a general call. Use this workaround until the errata is fixed.

Chip Revisions B and E Errata Information: (Continued)

The following errata items apply to revisions B and E 56F8037/56F8027 devices only.

Errata Number	Description	Impact and Workaround
5.0	Although required by the Philips spec, the I^2C does not reset its bus logic. Therefore, it does not prepare to receive an address following an unexpected START or repeated START. An unexpected START or repeated START is one that is not positioned according to the proper format.	Impact: Same as description. Workaround: Avoid all unexpected START conditions. Typically, this is not an issue in a single master system. In a multi-master system, avoid an unexpected START by powering up all master I^2Cs while the bus remains idle or by initiating master activity in a newly powered up master only when the bus is idle. Use this workaround until the errata is fixed.
6.0	The I^2C bus locks up when disabled in slave TX mode.	Impact: Same as description. Workaround: The software must ensure that SLV_ACTIVITY and MST_ACTIVITY are deasserted when disabling the module. To prevent this problem, follow the full module disabling procedure outlined in the documentation.
7.0	If you power up the I^2C in master mode and write to the TX FIFO for the first time while the bus is not idle, the I^2C may transmit onto the non-idle bus.	Impact: Same as description. Workaround: If it is possible to power up the module while the bus is busy, monitor for I^2C bus STOP detection or idle conditions before writing to the TX FIFO for the first time.
8.0	The I^2C may deassert interrupts during module disabling.	Impact: Same as description; reported to inform you of related module functionality. Workaround: If the I^2C is disabled after being enabled, the software must be able to manage the possible deassertion of asserted interrupt outputs.
9.0	The I^2C prematurely releases SCL in slave TX abort, causing all-ones data to be clocked out.	Impact: Same as description. Workaround: While operating in slave transmitter mode, do not write a read command to the TX FIFO.
10.0	The I^2C provides only one IPBus clock period of noise suppression.	Impact: Same as description. Workaround: Ensure that noise spikes do not exceed one IPBus clock period.

Chip Revisions B and E Errata Information: (Continued)

The following errata items apply to revisions B and E 56F8037/56F8027 devices only.

Errata Number	Description	Impact and Workaround
11.0	If the I^2C is generating a STOP condition on the bus, the CPU cannot write to the TX FIFO following a transmit abort.	Impact: Same as description. Workaround: If a transmit abort interrupt service routing needs to write data to the TX FIFO, poll the STAT register's ACT bit (bit 0) until the bit is zero before writing to the TX FIFO. This workaround is needed only if the TX abort source generates a STOP condition on the bus. The following TX abort sources generate STOP conditions: RNORST, SACKDET, GCREAD, GCNACK, TDNACK, AD2NACK, AD1NACK, and AD7NACK.
12.0	In the ADC, V_{REFL} and V_{REFH} functions are attached to the wrong ADC channels and are pinned out on the wrong external GPIO pads.	This errata has been corrected on devices with date codes ≥0701.
13.0	ROSC exceeds its –3% frequency variation spec when operating below –20°C.	This errata has been corrected on devices with date codes ≥0701.
14.1	The TAP instruction that initiates a mass erase to clear the flash lock security is never processed by the HFM. The flash memory cannot be forced to be unlocked via mass errase from the JTAG.	This errata has been corrected on devices with date codes ≥0701.
15.3	The ADC may not maintain accuracy of conversions if operated for extended periods of time at certain voltages below nominal voltage.	Impact: Same as description. Workaround: Maintain the VDDA and VREF inputs at a minimum of 3.1 volts. This errata has been corrected on devices marked with 4M67E.

Chip Revisions B and E Errata Information: (Continued)

The following errata items apply to revisions B and E 56F8037/56F8027 devices only.

Errata Number	Description	Impact and Workaround
16.3	If the ADC is powered down for an extended amount of time (e.g. days) and then powered back up, the ADC result may randomly drop to 0 or jump to 4095 (2^{12}-1). Periodic powering down does not exhibit a problem; however, extended periods in a continuous powered down state may result in invalid conversions. Also, shutting the power off to the entire device for an extended amount of time does not exhibit a problem. The issue has only been observed when the device is powered up while the ADC is powered off (in software).	Impact: Same as description. Workaround: If the device is to operate and the application requires the use of the ADC, keep the ADC powered up during normal operation. Do not power the ADC down, even if it is not in use at that time. Powering the ADC up or down is controlled by bits PD0 and PD1 in the POWER register of the ADC. This errata has been corrected on devices marked with 4M67E.
17.3	The comparator peripherals may develop a propensity not to assert their outputs when they should, e.g. when the plus input is greater than the negative input plus the maxium 20 mV offset specified for the device. This propensity is developed slowly over time when the comparator inputs are left in an asymmetrical postion, e.g. one input at 3.6 V and the other at 0 V for a long period of time. This condition also occurs with the comparator device powered off, but can also occur in normal operation with inputs biased asymmetrically.	Impact: Same as description. Workaround: If the comparator is not being used for a long period of time, set its inputs to similar voltage levels to avoid developing this issue. This errata has been corrected on devices marked with 4M67E.

Chip Revisions B and E Errata Information: (Continued)

The following errata items apply to revisions B and E 56F8037/56F8027 devices only.

Errata Number	Description	Impact and Workaround
18.3	The high voltage protection circuit may be engaged/not engaged on pin GPIOA10 when it should be not engaged/ engaged.	Impact: Malfunction of the comparator circuit or damage to the comparator circuit CMPAI2 is possible. Workaround: Malfunction can be avoided by configuring pin GPIOA8 for analog operation (as CMPAI1 circuit) whenever using pin GPIOA10 for analog operation (as CMPAI2 circuit). Damage can be avoided by: • configuring pin GPIOA8 for digital operation (not as CMPAI1) whenever pin GPIOA10 is configured for digital operation (not as CMPAI2 circuit) or • avoiding inputs > VDDA on pin GPIOA10. This errata has been corrected on devices marked with 4M67E.
19.3	The flash security backdoor key is not recognized.	Impact: The backdoor key cannot be used to unlock the flash at runtime. Workaround: None available.

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