



MC56F825x/MC56F824x (2M53V) Chip Errata

The following errata items apply to devices of the maskset 2M53V.

23254: IIC interrupt flag (IIC_SR[IICIF]) is automatically cleared when DSC exits stop mode

Description: When address matching occurs while the IIC operates in slave receive mode, the IIC can wake the core from stop mode. However, the IICIF flag is then cleared automatically. As a result, the IIC address matching interrupt service routine cannot be entered.

Impact: Refer to the Description.

Workaround:

1. Program the IIC slave to use address matching.
2. Before entering stop mode, program the applicable IIC module's bit in the SIM_SD1 register to enable the module's clock to continue to operate in stop mode.
3. Enter stop mode.
4. On an address match event, an interrupt occurs and the IICIF flag remains set.

25283: RAM corruption at device reset

Description: On-chip RAM data can be corrupted if a hardware or COP reset is performed.

Impact: User data stored in on-chip RAM can be corrupted any time that a hardware or COP reset occurs.

Workaround: Store data in the flash memory used as EEPROM or in the SIM's general purpose software control registers (SIM_SCR0 – SIM_SCR3), which retain data after reset.

4578: Possible incorrect readings on second ADC conversion when sampling two ADC channels and first channel input voltage < VREFL or > VREFH

Description: When sampling two ADC channels that are time-consecutively listed, if the first channel input voltage is less than VREFL or greater than VREFH, incorrect readings on the second conversion may result.

Impact: See Description.

Workaround: For the ADC pins used for the conversions, ensure that the voltages are between the values VREFL + 0.1 V and VREFH - 0.1 V.

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USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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