SECURE CONNECTIONS FOR A SMARTER WORLD

FACT SHEET
LA12xx

LAYERSCAPE® ACCESS LA12xx FAMILY OF PROGRAMMABLE BASEBAND PROCESSORS

The Layerscape Access LA12xx is an innovative family of programmable baseband processors, which delivers high-performance digital signal processing capabilities, performance scalability and application flexibility for diverse set of use cases.

LA12xx applications include 5G sub-6 GHz and mmWave Fixed Wireless Access equipment such as Integrated Small Cells, O-RAN Distributed Unit and Radio Unit, and Customer Premises Equipment (CPE). It can be also used in proprietary wireless applications such as defense and civilian radio systems and non-terrestrial networks (NTN).

The software defined nature of LA12xx provides a future proof platform for the latest 3GPP releases by over the air upgrades without modifying the underlying hardware.

The family enables a diverse ecosystem of RF devices, both sub-6 GHz and mmWave, as well as a variety of commercial-grade software and integration solutions. This open ecosystem model gives flexible choice and proven solutions to our customers.

NXP infrastructure products such as LA12xx Layerscape Access programmable baseband and Layerscape application processors are network class for device longevity and extended environmental use case conditions.

LAYERSCAPE ACCESS LA12XX DEVICE OVERVIEW

The main processing unit of the LA12xx family consists of the Vector Signal Processing Accelerator (VSPA) complex with up to eight VSPA engines delivering up to 1.3 TFLOPs of single precision floating point performance.

LA12xx integrates an analog to digital data conversion subsystem to support up to four transmit and four receive path sub-6 GHz antennas per chip, or a mmWave array supporting multi-gigabit rate radio links. These ADC/DACs provide a direct I/Q interface for power savings and wider channel bandwidth over SERDES based interfaces.

The LA12xx family also integrates a high-performance Forward Error Correction Accelerator (FECA) with a powerful integrated acceleration engine supporting both LDPC and Polar encoding/decoding required for many wireless applications.

The family features e200 Power® Architecture RISC cores, for real-time management and control, large on-chip SRAMs and operates without any external DRAM to save system cost and power. The device is securely booted from the host processor or can boot from a serial Flash memory. For I/O, the LA12xx has high speed PCIe Gen3 connectivity to provide bandwidth to the companion NXP Layerscape or i.MX® application processors.

The LA12xx based 5G solutions enable customer freedom to create their own product, with differentiated features, using NXP Codewarrior and example software, or customers can select proven software packages from NXP ecosystem partners, who are in production today.

LA12XX FEATURES

CORE AND MEMORY COMPLEX

- 6x 32-bit e200 Power® Architecture core complex @ 614.4 MHz
  - RF Management/control
  - Timing, frame structure control
- Up to 8x VSPA3-16 @ 614.4 MHz (=1.3 TFLOP)
  - Floating point SIMD compute, 32 CMAC HP/clock
- 2MB On-Chip SRAM memory

CONNECTIVITY AND I/O

- 2x PCIe Gen3 up to 8 lanes total
- 2x {I+Q} HS-DCS complex sampling up to 1.966 Gsps
  - Dual channel, <1GHz RF channel bandwidth at mmWave bands
- 4x {I+Q} LS-DCS complex sampling up to 491.52 Msps
  - Four channel, <140 MHz RF channel bandwidth at sub-6 GHz bands

ACCELERATION

- Forward Error Correction Unit (FECU)
  - 3GPP 5G/NR 38.212 compliant gNB and UE modes
  - Polar decoder/encoder
  - LDPC decoder/encoder

SYSTEM I/O AND RFIC CONTROL

- Low-speed SPI/JTAG/UART/I²C
- Fast RFIC management through LLCP
- On-Chip PLL, timebase / frame timer generator

DEVICE

- 21mm x 21mm PBGA package

FEATURES	BENEFITS
Software Defined Radio Access Network • NXP optimized DSP technology with Vector Signal Processor Accelerator (VSPA) engines. Supported by industry proven Codewarrior IDE	• Choice among several proven software vendors for the 3GPP Layer 1-3 stacks • Customization down to the Lower-PHY possible. Over the Air (OTA) field upgrade to newer 3GPP releases to protect deployed investment
Open Radio Interfaces • Integrated zero I/F 10bit high speed and 12bit low speed ADC/DAC data converters	• Open interface enables customer choice for RF transceiver solutions • Many proven RF vendors today for FR1(sub6-GHz) and FR2(mmWave). Custom solutions are possible • Lower power than SERDES based I/F options. 200-800MHz wide radio interfaces
NXP Network Class Products • Longevity & Industrial Class environment support	• Future proofed infrastructure equipment • Supports outdoor and harsh environments for 10 years or more lifetime. • Long term availability of products vs disposable-class competitor offerings
Integrated Networking and Acceleration • Forward Error Correction hardware • Large on chip memory • 2x PCIe Gen 3.0 Controllers, x8 SerDes Lanes	• Gigabit class processing for true high performance 5G applications

TARGET APPLICATIONS

- 5G sub-6 GHz or mmWave Integrated Small Cells (ISC)
- 5G O-RAN Distributed Unit (O-DU)
- 5G O-RAN sub-6 GHz or mmWave Radio Unit (O-RU)
- 5G Fixed Wireless Access CPE
- Aerospace/Military (NTN, Radar, etc.)
- Other proprietary wireless application

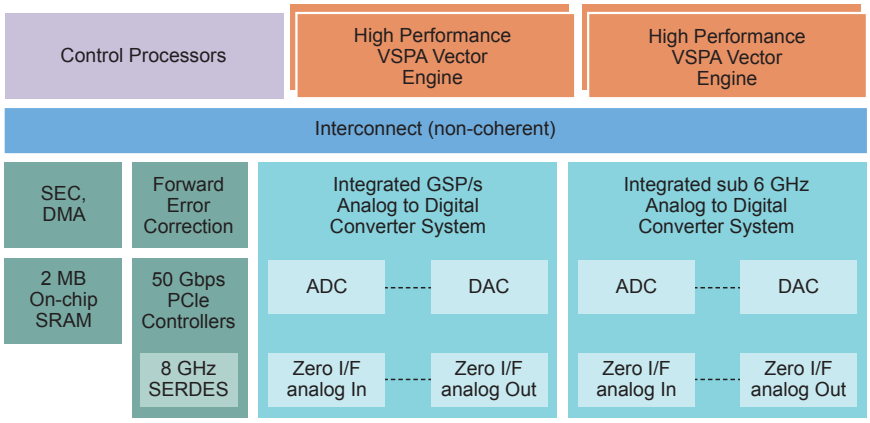
HARDWARE TOOLS

Customers can implement and develop their applications with LA12xx evaluation hardware. The LA12xx Evaluation Board is a combination of NXP LX2160 multicore Arm® processor as an host and LA12xx modem as baseband for 5G-NR Fixed Wireless applications. The boards come with pre-loaded board support package (BSP) based on a standard Linux kernel.

SOFTWARE SUPPORT

- Linux® SDK for QorIQ® Processors: Linux enablement for Layerscape® Devices
- CodeWarrior® Integrated Development Environment: Layerscape Access, VSPA and Host Layerscape Development

LAYERSCAPE ACCESS LA12xx BLOCK DIAGRAM



mmWave and Sub-6 GHz Baseband Processor

www.nxp.com

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