LAYERSCAPE® ACCESS LA9310 PROGRAMMABLE BASEBAND PROCESSOR

Ideal for peripheral 5G applications such as NLM/SON, repeater controller and femto RU radio interface

OVERVIEW

The Layerscape® Access LA9310 programmable baseband processor is a digital signal processor with integrated data converters (ADC/DAC) targeting physical layer processing of 5G infrastructure, digital front end (DFE) and custom communication-related systems at the edge of the network. Its low cost and power and programmable signal processing capabilities make it an attractive option to expensive FPGAs in applications such as network listening, small-scale radio units and repeaters.

The ADC/DAC analog subsystem supports a zero-IF I/Q interface toward an RFIC. With a sampling rate of up to 153 M samples per second, is suitable for both sub-6 GHz and limited-bandwidth mmWave applications. The Vector Signal Processing Accelerator (VSPA) DSP leverages NXP-supplied software libraries to efficiently implement sample-level baseband processing in the digital domain (e.g., digital up/down conversion, digital filtering, etc.), enabling a flexible software defined radio for standard and proprietary protocols. Results are provided to the host, typically an LS1023A or LS1043A, over a x1 Gen3 PCIe interface. The device includes DMA engines, timing blocks and RF control interfaces such as I2C, SPI and proprietary LLCP signaling.

In addition, the LA9310 is intended for industrial and measurement use cases. For such applications, the LA9310 functions as a lookaside accelerator to a host processor such as the i.MX applications processor families of devices, functioning as a signal pre-processor that includes analog sample acquisition together with initial DSP (filter/data reduction) processing or as a math accelerator. In these use cases, the lookaside accelerator often replaces an FPGA, connecting over PCIe or Ethernet.

FEATURES

CORE AND MEMORY COMPLEX

- One VSPA generation 2, 16AU DSP at up to 614 MHz (~80 GFLOP)
- One M4 32b Arm® core operating up to 307 MHz

CONNECTIVITY AND I/O

- One PCIe Gen3 lane
- Five {I+Q} ADCs, each sampling at up to 153 M samples per second
- One {I+Q} DAC, sampling at up to 153 M samples per second

ACCELERATION

- Forward error correction for proprietary communication protocols
- DMA for internal and host side data movement

LOW SPEED I/O AND RFIC CONTROL

- General purpose single lane SPI with four Chip Selects
- Lightweight LVDS Communication Protocol for RFIC Interface
- I²C controller
- UART
- JTAG

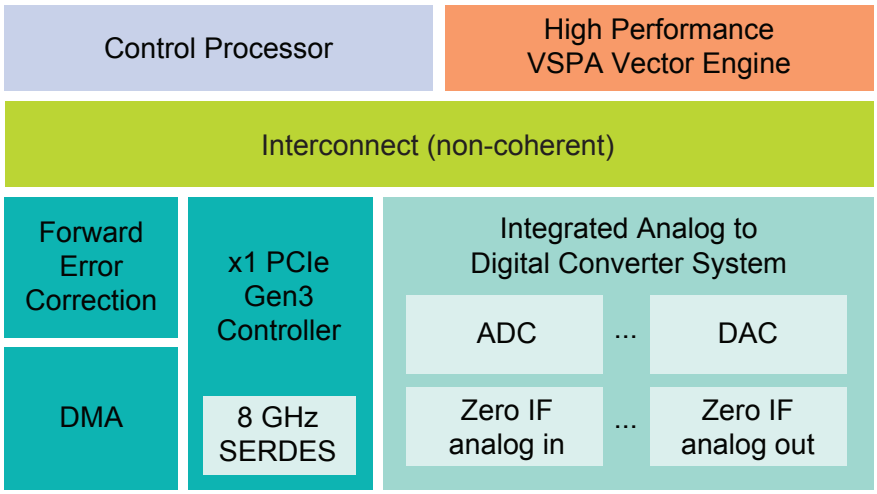
DEVICE

- 8 mm x 8 mm package
- 1.5 W total max power at 105 °C

TARGET APPLICATIONS

- Network monitoring mode (NMM)/ network listening module (NLM), for initial configuration in 5G self-organizing networks.
- Small digital 5G repeater — including digital signal filtering/ regeneration for limited bandwidth applications

LA9310 BLOCK DIAGRAM



- Analog repeater control — time/frequency and TDD switch point extraction
- Low-end radio units in O-RAN applications
- Defense: manpack, jam-resistant GPS, metadata sniffer
- Positioning: indoor/outdoor geo-location through triangulation of received (reference) signals
- 5G Dongle/RedCap or 5G-Light: minimum-hardware front-end solution for software defined radio

SOFTWARE SUPPORT

NXP provides a BSP for the LA9310 that includes drivers for all chip capabilities, example hello-world application that exercise the full data path of the device, VSPA libraries, and FreeRTOS running on the M4 core.

HARDWARE TOOLS

The LA9310 Reference Design Kit is a standalone system that consists of an LA9310 daughter card plugged into an LS1043A Reference Design Board. Customers can copy its design, use it to evaluate performance and use it to debug their own hardware.

www.nxp.com/la9310

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