Digital Signal Controllers

MC56F8006/2
Small cost. Low power. Big Performance.

Energy Efficient Solutions by Freescale

Target Applications:
- Industrial control
- Home appliances
- Smart sensors
- Fire and security systems
- Switched-mode power supply and power management
- Power metering
- Motor control (ACIM, BLDC, PMSM, SR, and stepper)
- Handheld power tools
- Arc fault protection
- Medical portable diagnostic and therapeutic devices
- Instrumentation
- Lighting ballast

Overview
The devices in the MC56F8006/2 series combine, on a single chip, the processing power of a digital signal processor (DSP) and the functionality of a microcontroller unit (MCU) with a flexible set of peripherals to create an extremely cost-effective solution.
The MC56F8006/2 series uses the 56800E core, which is based on a dual Harvard-style architecture consisting of three execution units operating in parallel. This allows as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

A full set of programmable peripherals supports various applications. Any signal pin associated with these peripherals can also be configured as a general-purpose input/output (GPIO). Power-saving features include a very low-power mode and the ability to shut down each peripheral independently. The MC56F8006/2 series adds additional features to Freescale's digital signal controller portfolio with low standby, stop and run current and an extended operating voltage range of 1.8–3.6V. The MC56F8006 series can enable power-sensitive devices with a fast wake-up time from stop mode, a very low-power crystal oscillator and ADC modules with lower run current.

The MC56F8006/2 series also offers a specific integrated peripheral set to improve the performance of motor control, power conversion and power-sensitive applications, reducing both external component count and overall system costs. The peripheral mix includes two programmable gain amplifiers, three high-speed comparators, RTC, dual 12-bit ADCs, up to six PWM outputs and various serial communication peripherals and timers.

Cost-Effective Development Tools
MC56F8006DEMO-T $99*
Cost-effective development set with demonstration board and USB TAP, enables a convenient design experience.

MC56F8006DEMO $49**
Cost-effective demonstration board allows easier and faster development, including USB interface channel, user LEDs, user push button switches, daughter card connectors and a JTAG interface.

CWH-UTP-ONCE-HE $99***
This USB TAP host target interface is a cost-effective hardware debugger tool designed for Freescale 16-bit DSC users. It is self-powered, requires no external power supply, and integrates HS USB download, flash memory programming and run-control visibility and control.

CWX-568-SE Free****
CodeWarrior™ Development Studio for Freescale 56800/E Digital Signal Controllers lets 56800E designers build and deploy even the most sophisticated DSC systems quickly and easily. The embedded Processor Expert™ technology provides GUI to enable quick generation of peripheral drivers and software libraries, which frees developers from the time-consuming effort of learning low level hardware details. This is a CodeWarrior Special Edition for DSC with a 32 KB code size limit.
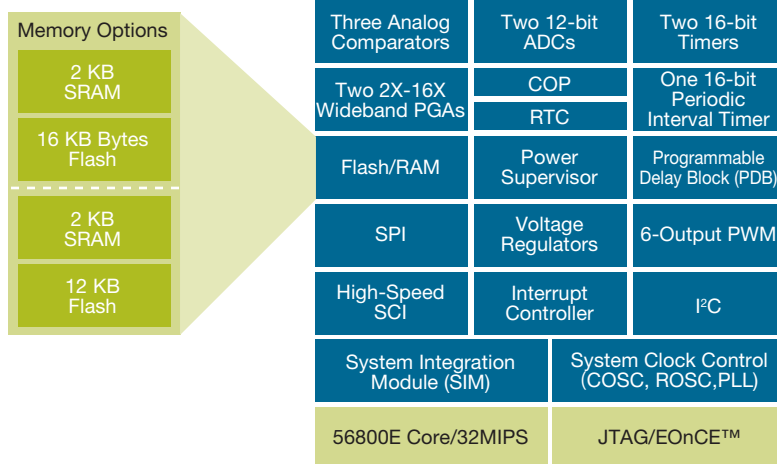
* $99 is a promotion price only valid for the first 2k sets; will go back to original price $149. Prices indicated are MSRP

** $49 is a promotion price only valid for the first 1k pcs; will go back to original price $75. Prices indicated are MSRP

***Effective from August 1, 2008 to April 3, 2009 (8 months)

****Subject to license agreement and registration

MC56F8006/2 Block Diagram

Memory Options
- 2 KB SRAM
- 16 KB Bytes Flash
- 2 KB SRAM
- 12 KB Flash

Three Analog Comparators	Two 12-bit ADCs	Two 16-bit Timers
Two 2X-16X Wideband PGAs	COP	One 16-bit Periodic Interval Timer
	RTC	
Flash/RAM	Power Supervisor	Programmable Delay Block (PDB)
SPI	Voltage Regulators	6-Output PWM
High-Speed SCI	Interrupt Controller	I²C
System Integration Module (SIM)	System Clock Control (COSC, ROSC, PLL)	
56800E Core/32MIPS	JTAG/EOnCE™	

Product Selector Guide

Part Number	Flash/SRAM (KB)	Package
MC56F8006VLF	16/2	48LQFP
MC56F8006VLC	16/2	32LQFP
MC56F8006VWL	16/2	28SOIC
MC56F8002VWL	12/2	28SOIC

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Features	Benefits
High-Performance	
• Efficient 16-bit 56800E DSP engine with dual Harvard architecture, up to 32 MIPS at 32 MHz core frequency • Four 36-bit accumulators, including extension bits, single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC) Instructions • 32-bit arithmetic and logic, multi-bit shifter • Parallel instruction set with unique addressing modes • JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, processor speed independent, real-time debugging • 155 basic instructions in conjunction with up to 20 address modes	• Hybrid architecture facilitates implementation of both control and signal processing functions in a single core device • Proven to deliver more control functionality per clock cycle than competing architectures • Ideal for closed loop control and signal processing applications • Eliminates need for expensive emulation tools
Integrated Third-Generation Flash	
• Up to 16 KB of program flash memory with security protection; 2 KB of unified program/data RAM • Flash memory emulation of EEPROM eliminates the need for external non-volatile memory • Extremely fast, word-writable programming up to 20 us/byte • Up to 100,000 write/erase cycles at typical voltage and temperature (10k minimum write/erase); 100 years typical data retention (15 years minimum)	• Flexible-flash-based systems can be reprogrammed quickly during the development cycle or late in the manufacturing cycle • Security circuitry prevents unauthorized access to RAM and flash contents • Flash memory emulation of EEPROM eliminates the need for external nonvolatile memory
Sophisticated Power Management	
• Three low and ultra-low-power modes, one of which allows limited use of peripherals • Low-power run and wait modes • 32 us typical wake up time from partial power down (PPD) mode • PPD mode allows I/O, RAM, PMC and COP to remain powered but the rest of the chip to shut down	• Allows continued application sampling in a reduced power state which extends battery life • Consistent with other Freescale low-power products, such as QE128 • Device has mode which consumes 1 uA at 3V VDD, preserving key state information in RAM
On-Chip Clock Synthesis	
• On-chip relaxation oscillator (ROSC) nominally generates an 8 MHz clock signal. It is also capable of operating at 400 KHz in low power mode. • VLP crystal oscillator (COSC) can be used with a 32 KHz watch crystal in low range mode, or 1 to 16 MHz crystal in high range mode • On-chip 1 KHz RTC clock	• Eliminates use of an external clock source, ultimately reducing total system costs • Includes ultra-low-power watch crystal OSC circuit for accurate timebase in low-power modes
Two Differential Programmable Gain Amplifiers	
• Common mode noise and offset are automatically cancelled out, two to four consecutive samples required for noise/offset cancellation • Sample may be synchronized with PWM operation using the PWM sync output and programmable delay block • Sampling time can be precisely controlled to less than 0.1 us • Several programmable gains (1x, 2x, 4x, 8x, 16x, and 32x) • Selectable tradeoff for slower/low power versus faster/more power	• Performs differential-to-single-ended conversion of analog signals • Facilitates design via availability of both software and hardware triggers • PGA operates in concert with on-chip ADC to amplify small signals, increasing ADC input dynamic range • Enables precise conversion of analog values • Multiple options selectable for gains • Several operation modes, enables low power or more power options for power consumption reduction
Three High-Speed Analog Comparators	
• Selectable interrupt on rising edge and/or falling edge of comparator output • The positive and minus inputs are both driven from 4-to-1 muxes • Two software-selectable speed levels by power consumption and propagation delay	• Selectable edge interrupt allows easy and flexible design • High speed operation enables seeing result of comparator with minimal delay • Reduces future power consumption • Allows additional flexibility in reassigning I/O pins as comparator inputs during PCB design
Dual 12-bit SAR ADC	
• Dual 12-bit SAR ADC with an integrated temperature sensor for each ADC • Up to 24 external ADC input pins • 2.5 or 3.5 us conversion time at continuous conversion or single conversion respectively • Single or continuous conversion, automatic compare function, configurable sample time and conversion speed/power • Asynchronous clock source; Input clock selectable from up to four sources	• Flexible configuration meets high-performance and low-power requirements • Calculates temperature without any external components, saving an ADC input pin for other uses • Configurable sample time and conversion speed/power • Enables lower noise operation for your design • ADC can run when MCU clocks are off, such as in STOP3 low-power mode
6-channel PWM	
• Up to 96 MHz peripherals—PWM, timers and SCI • Six-output PWM module with four programmable fault inputs • Programmable dead time insertion • Programmable PWM generation for power supply apps • Multiple PWM frequency outputs	• High-speed PWM enables more accurate control and higher speed systems • High-performance PWM with programmable fault capability simplifies design and promotes compliance with safety regulations • Enhances power conversion functionality and accuracy • Applications include motor control and digital power supply • Enables more accurate controls • Flexible, programmable PWM
Timer	
• Dual 16-bit multi-function timers • Programmable delay block (PDB) • One programmable interval timer (PIT) • Real-time counter (RTC)	• Timers can be used to generate PWM, capture events or receive quadrature encoder inputs • PDB precisely controls ADC/PGA sample timing relative to PWM reload cycles • PIT for scheduling periodic interrupt • RTC can be used to implement a real-time clock
Input/Output	
• Up to 40 GPIOs • Programmable output drive level, slew rate control and optional input low pass filters	• Large number of flexible I/O pins allow developers to easily interface the device into their own designs
System Protection	
• Computer operating properly (COP)/watchdog timer with independent 1 kHz on-chip oscillator • Low voltage detection with reset or interrupt • Low supply voltage detection • Illegal opcode and illegal address detection with reset • Flash security feature and flash protection	• Resets device in instance of runaway or corrupted code • Independent clock source provides additional protection in case of loss of clock • Allows system to write/save important variables before voltage drops too low • Holds devices in reset until reliable voltage levels are reapplied to the part • Flash security feature prevents unauthorized accesses to memory to protect valuable software intellectual property • Flash protection prevents accidental modifications

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