MPC855T PBGA PIN ASSIGNMENT

PIN	NAME	PIN	NAME
A2	CS1	B1	UPWAITB/GPL_B4
A3	CE2_A	B2	RD/WR
A4	CS4	B3	CE1_A
A5	WE3/BS_B3/PCWE	B4	CS5
A6	WE1/BS_B1/IOWR	B5	GPL_A2/GPL_B2/CS2
A7	BS_A2	B6	WE2/BS_B2/PCOE
A8	VDDL	B7	MII_CRS
A9	A31	B8	BS_A3
A10	A28	B9	TSIZ0/REG
A11	A30	B10	A22
A12	A29	B11	A23
A13	A27	B12	A21
A14	A14	B13	A17
A15	A11	B14	A13
A16	A7	B15	A10
A17	A5	B16	A6
A18	A2	B17	A4
		B18	A1
		B19	A0
C1	UPWAITA/GPL_A4	D1	TEA
C2	TA	D2	BDIP/GPL_B5
C3	CS0	D3	GPL_A5
C4	CS7/CE(2)B	D4	CS2
C5	GPL_A3/GPL_B3/CS3	D5	CS6/CE(1)B
C6	OE/GPL_A1/GPL_B1	D6	N/C
C7	WE0/BS_B0/IORD	D7	GPL_A0/GPL_B0
C8	BS_A1	D8	BS_A0
C9	TSIZ1	D9	A18
C10	A26	D10	A25
C11	A24	D11	A19
C12	A20	D12	A15
C13	A16	D13	N/C
C14	A12	D14	N/C
C15	A9	D15	A8
C16	A3	D16	PC[15]/DREQ0/RTS1/L1ST1
C17	PB[31]/REJECT1/SPISEL	D17	PA[14]/TXD1
C18	PA[15]/RXD1	D18	PC[14]/DREQ1/L1ST2
C19	PB[30]/SPICLK/RSTRT2	D19	PB[28]/SPIMISO/BRGO4

PIN	NAME	PIN	NAME
E1	$\overline{BB}$	F1	$\overline{BURST}$
E2	$\overline{BG}$	F2	$\overline{CR}$/IRQ3
E3	$\overline{BI}$	F3	$\overline{TS}$
E4	$\overline{CS3}$	F4	VDDH
E5	VDDH	F5	VDDH
E6	VDDH	F6	GND
E7	VDDH	F7	GND
E8	VDDH	F8	GND
E9	VDDH	F9	GND
E10	VDDH	F10	GND
E11	VDDH	F11	GND
E12	VDDH	F12	GND
E13	VDDH	F13	GND
E14	VDDH	F14	GND
E15	VDDH	F15	VDDH
E16	PB[29]/SPIMOSI	F16	VDDH
E17	PA[13] $\overline{}$	F17	PA[12] $\overline{}$
E18	PC[13]/L1RQB/L1ST3	F18	PC[12]/L1RQA/L1ST4
E19	PB[27]/I2CSDA/BRGO1	F19	PB[26]/I2CSCL/BRGO2
G1	IP_B3/IWP2/VF2	H1	IP_B7/PTR/AT3
G2	IP_B4/LWP0/VF0	H2	IP_B0/IWP0/VFLS0
G3	FRZ/$\overline{IRQ6}$	H3	$\overline{RSV}$/$\overline{IRQ2}$
G4	$\overline{BR}$	H4	MII_COL
G5	VDDH	H5	VDDH
G6	GND	H6	GND
G7	GND	H7	GND
G8	GND	H8	GND
G9	GND	H9	GND
G10	GND	H10	GND
G11	GND	H11	GND
G12	GND	H12	GND
G13	GND	H13	GND
G14	GND	H14	GND
G15	VDDH	H15	VDDH
G16	PA[11]/L1TXDB	H16	TCK/DSDK
G17	TDO/DSDO	H17	TDI/DSDI
G18	$\overline{TMS}$	H18	MII_MDIO
G19	$\overline{TRST}$	H19	VDDL

PIN	NAME	PIN	NAME
J1	ALE_B/DSCK/AT1	K1	KR/IRQ4/RETRY/SPKROUT
J2	IP_B2/IOIS16_B/AT2	K2	ALE_A
J3	IP_B1/IWP1/VFLS1	K3	IP_B6/DSDI/AT0
J4	IP_B5/LWP1/VF1	K4	BADDR30/REG
J5	VDDH	K5	VDDH
J6	GND	K6	GND
J7	GND	K7	GND
J8	GND	K8	GND
J9	GND	K9	GND
J10	GND	K10	GND
J11	GND	K11	GND
J12	GND	K12	GND
J13	GND	K13	GND
J14	GND	K14	GND
J15	VDDH	K15	VDDH
J16	PB[25]/SMTXD1	K16	PB[21]/SMTXD2/L1CLKOB
J17	PA[10]/L1RXDB	K17	PB[23]/SMSYN1/SDACK1
J18	PB[24]/SMRXD1	K18	PA[9]/L1TXDA
J19	PC[11]/CTS1	K19	PC[10]/CD1/TGATE1
L1	MODCK1/OP2/STS	M1	VDDL
L2	OP1	M2	BADDR29
L3	AS	M3	BADDR28
L4	OP0	M4	OP3/MODCK2/DSDO
L5	VDDH	M5	VDDH
L6	GND	M6	GND
L7	GND	M7	GND
L8	GND	M8	GND
L9	GND	M9	GND
L10	GND	M10	GND
L11	GND	M11	GND
L12	GND	M12	GND
L13	GND	M13	GND
L14	GND	M14	GND
L15	VDDH	M15	VDDH
L16	PB[20]/SMRXD2/L1CLKOA	M16	PC[7]/L1TSYNCB/SDACK2
L17	PA[8]/L1RXDA	M17	PA[6]/BRGCLK1/TOUT1/CLK2
L18	PC[9]	M18	PC8/TGATE2
L19	PB[22]/SMSYN2/SDACK2	M19	PA[7]/CLK1/TIN1/L1RCLKA/BRGO1

PIN	NAME	PIN	NAME
N1	EXTAL	P1	XTAL
N2	EXTCLK	P2	SRESET
N3	TEXP	P3	RSTCONF
N4	HRESET	P4	VDDH
N5	VDDH	P5	VDDH
N6	GND	P6	GND
N7	GND	P7	GND
N8	GND	P8	GND
N9	GND	P9	GND
N10	GND	P10	GND
N11	GND	P11	GND
N12	GND	P12	GND
N13	GND	P13	GND
N14	GND	P14	GND
N15	VDDH	P15	VDDH
N16	PB[16]/L1RQA/L1ST4	P16	VDDH
N17	PB[18]/L1ST2	P17	PA[3]/CLK5/TIN3/BRGOUT3
N18	PA5/CLK3/TIN2/L1TCLKA/BRGOUT2	P18	PB[17]/L1RQB/L1ST3
N19	PB[19]/L1ST1/RTS1	P19	PA[4]/TOUT2/CLK4
R1	KAPWR	T1	VDDSYN
R2	PORESET	T2	XFC
R3	WAIT_A	T3	IP_A7
R4	WAIT_B	T4	IP_A1
R5	VDDH	T5	IP_A0
R6	VDDH	T6	IP_A6
R7	VDDH	T7	D31
R8	VDDH	T8	D25
R9	VDDH	T9	D22
R10	VDDH	T10	D15
R11	VDDH	T11	D9
R12	VDDH	T12	D17
R13	VDDH	T13	D12
R14	VDDH	T14	VDDH
R15	VDDH	T15	PD[7]/MII-RX-ERR
R16	PD[12]/L1RSYNCB/MII-MDC	T16	PD[11]/MII-TX-ERR
R17	PB[15]/BRGO3	T17	PC[4]/L1RSYNCA
R18	PA[2]/CLK6/TOUT3/L1RCLKB/BRGCLK2	T18	PC[5]/L1TSYNCA/SDACK1
R19	PC[6]/L1RSYNCB	T19	PA[1]/CLK7/TIN4/BRGO4

PIN	NAME	PIN	NAME
U1	VSSSYN	V1	VSSSYN1
U2	N/C	V2	N/C
U3	IP_A2/IOIS16_A	V3	DP0/IRQ3
U4	IP_A4	V4	DP3/IRQ6
U5	IP_A5	V5	DP1/IRQ4
U6	D30	V6	D28
U7	D26	V7	D24
U8	D21	V8	D20
U9	D19	V9	D18
U10	D16	V10	D14
U11	D11	V11	D10
U12	D23	V12	D27
U13	D8	V13	D13
U14	IRQ1	V14	IRQ0
U15	PD[5]/MII-TXD3	V15	MII_TX_EN
U16	PD[4]/MII-TXD2	V16	PD[6]/MII-RXDV
U17	PD[15]/L1TSYNCA/MII-RXD3	V17	PD[9]/MII-TXD0
U18	PB[14]/RSTRT1	V18	PD[13]/L1TSYNCB/MII-RXD1
U19	PA[0]/CLK8/TOUT4/L1TCLKB	V19	PD[14]/L1RSYNCA/MII-RXD2

W2	IP_A3
W3	CLKOUT
W4	DP2/IRQ5
W5	D29
W6	D7
W7	D6
W8	VDDL
W9	D5
W10	D3
W11	D2
W12	D1
W13	D4
W14	D0
W15	IRQ7/MII_TXCLK
W16	PD[3]/MII-TXD1
W17	PD[8]/MII-RX_CLK
W18	PD[10]/MII-RXD0