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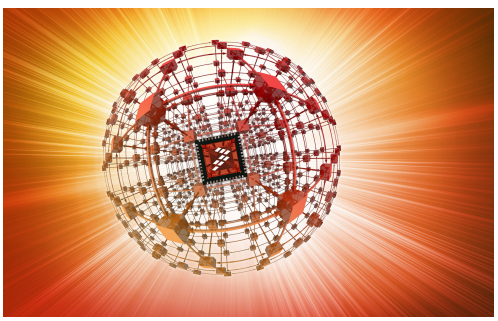
Rev 2, 3/2014

KE06 Sub-Family Product Brief

Supports all KE06 devices



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1 KE06 sub-family introduction

This sub-family includes a powerful array of analog, communication, and timing and control peripherals with specific flash memory size and the pin count.

- Core and architecture:
  - ARM Cortex-M0+ core running up to 48 MHz with zero wait state execution from memories
    - Single-cycle access to I/O: Up to 50 percent faster than standard I/O, improves reaction time to external events allowing bit manipulation and software protocol emulation
    - Two-stage pipeline: Reduced number of cycles per instruction (CPI), enabling faster branch instruction and ISR entry, and reducing power consumption
    - Excellent code density in comparison to 8-bit and 16-bit MCUs: Reduced flash size, system cost, and power consumption
    - Optimized access to program memory: Accesses on alternate cycles reduces power consumption
    - 100 percent compatible with ARM Cortex-M0 and a subset ARM Cortex-M3/M4: Reuse existing compilers and debug tools

    - Simplified architecture: 56 instructions and 17 registers enable easy programming and efficient packaging of 8/16/32-bit data in memory
    - Linear 4 GB address space removes the need for paging/banking, reducing software complexity
    - ARM third-party ecosystem support: Software and tools to help minimize development time/cost
  - Bus clock running up to 24 MHz
  - Bit-band: Enhanced SRAM bit operation by aliased SRAM bit-band region with Cortex-M0+ core
  - BME: Bit manipulation engine reduces code size and cycles for bit-oriented operations to peripheral registers and SRAM memory eliminating traditional methods where the core would need to perform read-modify-write operations.
- Power-saving:
  - Low-power ARM Cortex-M0+ core with excellent energy efficiency
  - Supports three power modes: Run, Wait and Stop
  - Supports clock gating for unused modules, and specific peripherals remain working in Stop mode
- Memory:
  - Up to 128 KB program flash, 16 KB SRAM
  - Embedded 32 B flash cache for optimizing bus bandwidth and flash execution performance
  - Support bit operation on SRAM domain through aliased bit-band region or BME
- Clocks
  - Oscillator (OSC) - supports 32.768 kHz crystal or 4 MHz to 24 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
  - Internal clock source (ICS) - internal FLL with internal or external reference, 37.5 kHz pretrimmed internal reference for 48 MHz system clock
  - Internal 1 kHz low-power oscillator (LPO)
- Mixed-signal analog:
  - Up to 16 channels of 12-bit analog-to-digital conversion (ADC) with 2.5 µs conversion time, 1.7 mV/°C temperature sensor, internal bandgap reference channel, supporting automatic compare, optional hardware trigger, and operating in Stop mode
  - Up to two analog comparators (ACMP) with both positive and negative inputs, separately selectable interrupt on rising and falling comparator output
- Human-machine interface (HMI):
  - Up to two 32-bit keyboard interrupt modules (KBI)
- Connectivity and communications:
  - Up to three serial communications interface (UART) modules with optional 13-bit break, full duplex non-return to zero (NRZ) and LIN extension support
  - Up to two serial peripheral interface (SPI) modules with full-duplex or single-wire bidirectional and master or slave mode
  - Up to two Inter-integrated circuit (I^2C) modules with support of system management bus and I2C0 supports 4-wire interface feature
  - One Freescale's scalable controller area network (MSCAN) conforming to CAN2.0A/B specification
- Reliability, safety and security:
  - Internal watchdog with independent clock source
  - Cyclic redundancy check (CRC) with programmable 16- or 32-bit polynomial generator
- Timing and control:
  - FlexTimer module (FTM) including one 6-channel FTM with deadtime insertion and fault detection, and up to two 2-channel FTMs backward compatible with TPM modules. Each channel can be configured for input capture, output compare, edge- or center-aligned PWM mode.
  - Periodic interrupt timer (PIT) for RTOS task scheduler time base or trigger source for ADC conversion and timer modules
  - 16-bit pulse width timer (PWT) for positive, negative and period capture with selectable driving clock
  - FTM and PWT modules support separate timer clock from core and bus, up to 48 MHz
  - 16-bit real timer counter (RTC)
- I/O and package:
  - Up to 71 GPIO pins with interrupt functionality
  - Up to 2 true open-drain output pins

- Up to 8 high current drive pins supporting 20 mA source/sink current
- Multiple package options from 44-pin to 80-pin

The family acts as a low-power, high-robustness, and cost-effective microcontroller to provide developers an appropriate entry-level 32-bit solution. The family is next generation MCU solution with enhanced EMC/ESD performance for cost-sensitive, high-reliability devices applications used in high electrical noise environments.

2 Block diagram

The following figure shows a superset block diagram of the device. Other devices within the family have a subset of the features.

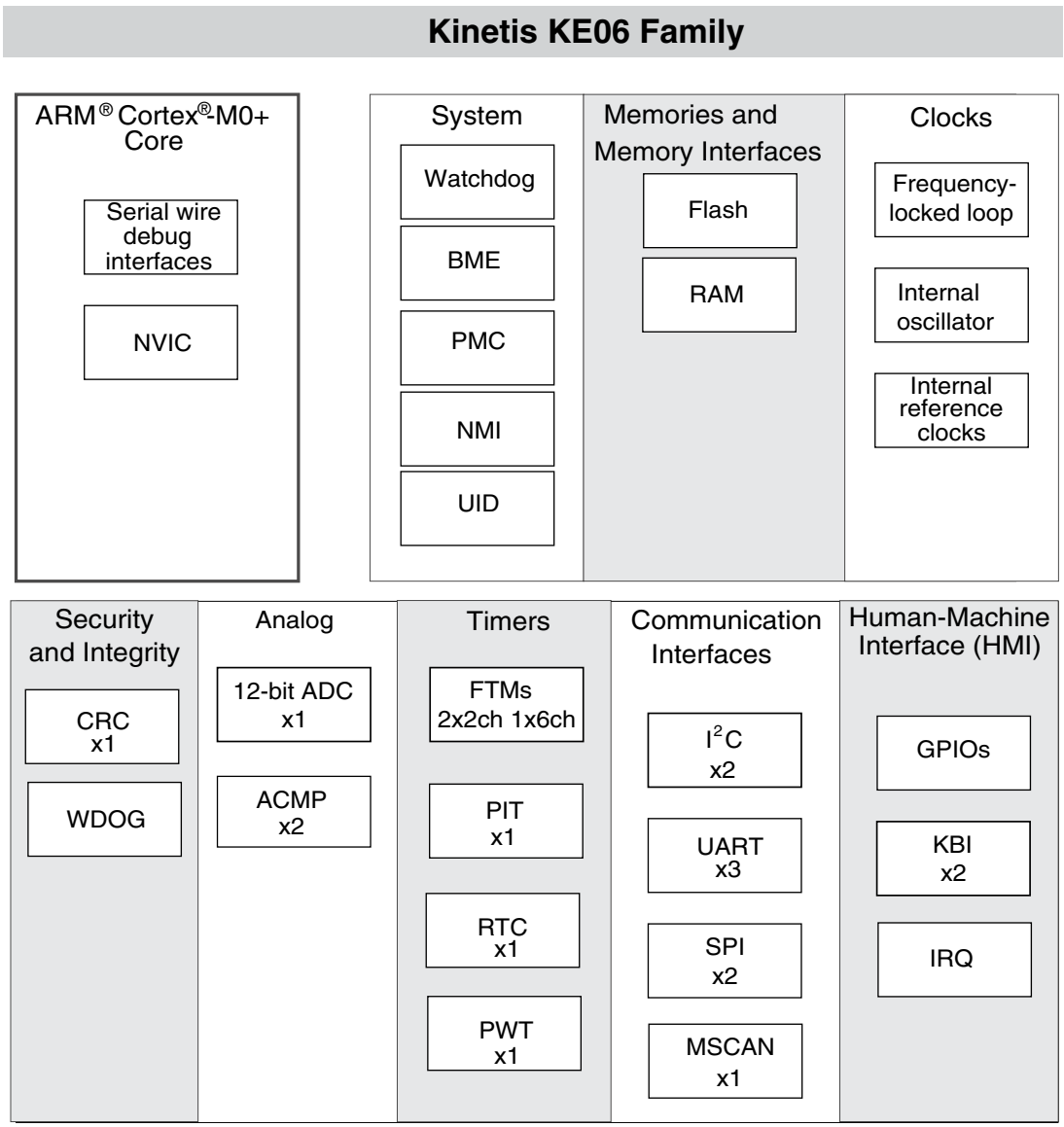

Figure 1. KE06 family block diagram

3 Features

3.1 Feature summary

All devices within the KE06 sub-family have a minimum of the following features.

Table 1. Common features among all KE06 devices

Operating characteristics	• 2.7 V to 5.5 V • Temperature range (T_A) -40 °C to 105 °C • Three operation modes: Run, Wait, Stop
Core features	• Next generation 32-bit ARM Cortex M0+ core • Supports up to 32 interrupt request sources • Nested vectored interrupt controller (NVIC) • 2-pin serial wire debug (SWD) interface
System and power management	• Watchdog • Integrated bit manipulation engine (BME) • Power management controller with three different power modes • Non-maskable interrupt (NMI) • 80-bit unique identification (ID) number

Clocks	• External crystal oscillator or resonator
	• Up to DC-48 MHz external square wave input clock
	• Internal clock references
	  • 31.25–39.063 kHz oscillator
	  • 1 kHz oscillator
	• Frequency-locked loop with the range of
	  • 40–50 MHz

Memory and memory interfaces	• Up to 128 KB flash memory • Up to 16 KB SRAM
Security and integrity	• Watchdog (WDOG) • Cyclic redundancy check (CRC) module
Analog	• One 12-bit analog-to-digital converter (ADC) • Two analog comparators (ACMP) with internal 6-bit digital-to-analog converter (DAC)
Timers	• One 6-channel and two 2-channel 16-bit FTM modules • 32-bit programmable interrupt timer (PIT) • Pulse width timer (PWT) • Real-time clock (RTC) • System tick timer (SYSTICK)
Communications	• Two serial peripheral interfaces (SPI) • Two inter-integrated circuit (I^2C) modules • Three universal asynchronous receiver/transmitter (UART) modules • One Freescale's scalable controller area network (MSCAN) module
Human-machine interface	• Up to 71 GPIO pins • Up to two 32-bit keyboard interface (KBI) modules • Interrupt (IRQ)

3.2 Memory and package options

The following table summarizes the memory and package options for the KE06 family. All devices which share a common package are pin-for-pin compatible.

Table 2. KE06 family summary

Sub-Family	Performance (MHz)	Memory		Package			
		Flash (KB)	SRAM (KB)	44 LQFP (10x10)	64 LQFP (10x10)	64 QFP (14x14)	80 LQFP (14x14)
KE06	48	64	8	+	+	+	+
		128	16	+	+	+	+

3.3 Part numbers and packaging

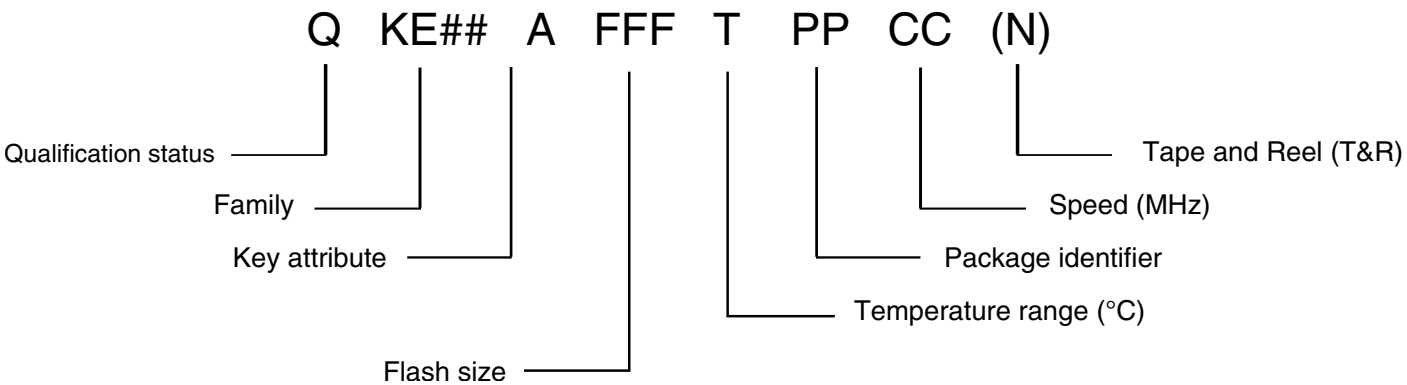

Figure 2. Part numbers diagrams

Table 3. Part number field description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE06
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105

Table continues on the next page...

Table 3. Part number field description (continued)

Field	Description	Values
PP	Package identifier	• LD = 44 LQFP (10 mm x 10 mm) • LH = 64 LQFP (10 mm x 10 mm) • QH = 64 QFP (14 mm x 14 mm) • LK = 80 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

3.4 KE06 family features (48 MHz performance)

The following table lists the differences among the various devices available within the KE06 family. The features listed below each part number specify the maximum configuration available on that device. The signal multiplexing configuration determines which modules can be used simultaneously.

Table 4. KE06 48 MHz performance table

MC part number	MKE06Z64VLD4(R)	MKE06Z128VLD4(R)	MKE06Z64VQH4(R)	MKE06Z128VQH4(R)	MKE06Z64VLH4(R)	MKE06Z128VLH4(R)	MKE06Z64VLK4(R)	MKE06Z128VLK4(R)
General								
CPU frequency	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz
Pin count	44	44	64	64	64	64	80	80
Package	LQFP	LQFP	QFP	QFP	LQFP	LQFP	LQFP	LQFP
Memories and memory interfaces								
Flash	64 KB	128 KB	64 KB	128 KB	64 KB	128 KB	64 KB	128 KB
SRAM	8 KB	16 KB	8 KB	16 KB	8 KB	16 KB	8 KB	16 KB
EEPROM	-	-	-	-	-	-	-	-
ROM	-	-	-	-	-	-	-	-
Core modules								
Debug-SWD	YES	YES	YES	YES	YES	YES	YES	YES
NMI	YES	YES	YES	YES	YES	YES	YES	YES
MTB	-	-	-	-	-	-	-	-
System modules								
Watchdog /w ind. clock	YES	YES	YES	YES	YES	YES	YES	YES
PMC	YES	YES	YES	YES	YES	YES	YES	YES
DMA	-	-	-	-	-	-	-	-
BME (bit manipulation engine)	YES	YES	YES	YES	YES	YES	YES	YES

Table continues on the next page...

Table 4. KE06 48 MHz performance table (continued)

MC part number	MKE06Z64VLD4(R)	MKE06Z128VLD4(R)	MKE06Z64VQH4(R)	MKE06Z128VQH4(R)	MKE06Z64VLH4(R)	MKE06Z128VLH4(R)	MKE06Z64VLK4(R)	MKE06Z128VLK4(R)
Clock modules								
ICS	FLL	FLL	FLL	FLL	FLL	FLL	FLL	FLL
Main OSC (32 kHz, 4-24 MHz)	YES	YES	YES	YES	YES	YES	YES	YES
IRC (~32 kHz)	YES	YES	YES	YES	YES	YES	YES	YES
LPO (~1 kHz)	YES	YES	YES	YES	YES	YES	YES	YES
16-bit RTC	1	1	1	1	1	1	1	1
Security and integrity								
CRC	YES	YES	YES	YES	YES	YES	YES	YES
Analog								
ADC with 8 buffer entry	12bit, 1x12ch	12bit, 1x12ch	12bit, 1x16ch	12bit, 1x16ch	12bit, 1x16ch	12bit, 1x16ch	12bit, 1x16ch	12bit, 1x16ch
6-bit DAC	2	2	2	2	2	2	2	2
ACMP	2	2	2	2	2	2	2	2
Bandgap Vref (no pin-out)	1	1	1	1	1	1	1	1
Timers								
16-bit FTM (6-ch)	1	1	1	1	1	1	1	1
16-bit FTM (2-ch)	2	2	2	2	2	2	2	2
PIT (32-bit)	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch
PWT	1	1	1	1	1	1	1	1
Communication interfaces								
UART (LIN slave capable)	3	3	3	3	3	3	3	3
SPI (8-bit)	2	2	2	2	2	2	2	2
I2C	2	2	2	2	2	2	2	2
MSCAN	1	1	1	1	1	1	1	1
Human-machine interface								
Segment LCD	-	-	-	-	-	-	-	-
TSI (capacitive touch)	-	-	-	-	-	-	-	-
Total GPIOs	38	38	58	58	58	58	71	71
20 mA high-drive GPIO	8	8	8	8	8	8	8	8
True open-drain	2	2	2	2	2	2	2	2
Operating characteristics								
Voltage range	2.7-5.5 V	2.7-5.5 V	2.7-5.5 V	2.7-5.5 V	2.7-5.5 V	2.7-5.5 V	2.7-5.5 V	2.7-5.5 V
Flash write V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V

Table continues on the next page...

Table 4. KE06 48 MHz performance table (continued)

MC part number	MKE06Z64VLD4(R)	MKE06Z128VLD4(R)	MKE06Z64VQH4(R)	MKE06Z128VQH4(R)	MKE06Z64VLH4(R)	MKE06Z128VLH4(R)	MKE06Z64VLK4(R)	MKE06Z128VLK4(R)
Temperature range	-40 to 105 °C	-40 to 105 °C	-40 to 105 °C	-40 to 105 °C	-40 to 105 °C	-40 to 105 °C	-40 to 105 °C	-40 to 105 °C

3.5 Module-by-module feature list

The following sections describe the high-level module features for the family's superset device. See KE06 family features (48 MHz performance) for differences among the subset devices.

3.5.1 Core modules

3.5.1.1 ARM Cortex-M0+ core

- Up to 48 MHz core frequency from 2.7 V to 5.5 V across temperature range of –40 °C to 105 °C
- Supports up to 32 interrupt request sources
- 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial wire debug (SWD) reduces the number of pins required for debugging
- Single cycle 32 bits by 32 bits multiply

3.5.1.2 Nested Vectored Interrupt Controller (NVIC)

Following are the features of the NVIC module.

- Up to 32 interrupt sources
- Includes a single non-maskable interrupt

3.5.1.3 Asynchronous Wake-up Interrupt Controller (AWIC)

The features of the AWIC module are given below.

- Supports interrupt handling when system clocking is disabled in low-power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very deep sleep mode.
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected
- Contains no programmer’s model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

3.5.1.4 Debug controller

- 2-pin serial wire debug (SWD) provides external debugger interface

3.5.2 System modules

3.5.2.1 Power Management Control (PMC) unit

The features of the PMC module are listed below.

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable power saving modes
- No output supply decoupling capacitors required
- Available wake-up from power saving modes via RTC and external inputs
- Integrated power-on-reset (POR)
- Integrated low voltage detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable low-voltage warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz low-power oscillator (LPO)

3.5.2.2 Bit Manipulation Engine (BME)

Bit manipulation engine reduces code size and cycles for bit-oriented operations to peripheral registers and SRAM memory eliminating traditional methods where the core would need to perform read-modify-write operations. The features of the BME module are listed below.

- Lightweight implementation of decorated storage for peripheral address space
- Additional access semantics encoded into the reference address
- Two-stage pipeline design matching the AHB system bus protocol
- Combinationally passes non-decorated accesses to peripheral bridge bus controller
- Conversion of decorated loads and stores from processor core into atomic readmodify- writes
- Decorated loads support unsigned bit field extracts, load-and-{set,clear} 1-bit operations
- Decorated stores support bit field inserts, logical AND, OR, and XOR operations
- Support for byte, halfword and word-sized decorated operations
- Supports minimum signal toggling on AHB output bus to reduce power dissipation

3.5.2.3 Watchdog (WDOG) module

The features of the Watchdog module are described as follows.

- Independent clock source input (independent from CPU/bus clock)
- Choice between clock sources
  - 1 kHz internal low-power oscillator (LPOCLK)
  - Internal 32 kHz reference clock (ICSIRCLK)
  - External clock (OSCERCLK)
  - Bus clock

3.5.2.4 System clocks

The following clock sources can be used as system clocks.

- System oscillator (OSC)—Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 to 39.0625 kHz (low-range mode) or 4-24 MHz (high-range mode)
- Internal clock source (ICS)
  - Frequency-locked loop (FLL) controlled by internal or external reference
    - 40 MHz~50 MHz FLL output
  - Internal reference clocks—Can be used as a clock source for the other on-chip peripherals
    - On-chip RC oscillator range of 31.25 to 39.0625 kHz oscillator as the reference of FLL input.

3.5.3 Memories and memory interfaces

3.5.3.1 On-chip memory

- 48 MHz performance devices
  - Up to 128 KB flash memory
  - Up to 16 KB SRAM
- Security circuitry to prevent unauthorized access to RAM and flash contents

3.5.4 Analog

3.5.4.1 Analog-to-Digital Converter (ADC)

The features of the ADC module are given below.

- Linear successive approximation algorithm with 8-, 10-, or 12-bit resolution
- Up to 16 external analog inputs, and 5 internal analog inputs including internal bandgap, temperature sensor, and references
- Output formatted in 8-, 10-, or 12-bit right-justified unsigned format
- Single or continuous conversion (automatic return to idle after single conversion)
- Supports up to eight result FIFO with selectable FIFO depth
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in Wait or Stop modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value

3.5.4.2 Analog Comparator (ACMP)

The ACMP module has the following features.

- Operational over the whole supply range of 2.7–5.5 V
- On-chip 6-bit resolution DAC with selectable reference voltage from V_{DD} or internal bandgap
- Configurable hysteresis
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Up to four selectable comparator inputs; one of these is fixed and connected to built-in DAC output while the others are externally mapped on pinouts.
- Operational in Stop mode

3.5.5 Timer

3.5.5.1 FlexTimers (FTM)

The FlexTimer module exhibits the following features.

- Selectable FTM source clock, supporting separate timer clock from core and bus, up to 48 MHz
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Up to four fault inputs for global fault control
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition

3.5.5.2 Periodic Interrupt Timer (PIT)

The features of the PIT module are given below.

- Two general-purpose interrupt timers
- One interrupt timer for triggering ADC conversions
- 32-bit counter resolution
- Clocked by bus clock frequency

3.5.5.3 Real-Time Clock (RTC)

Following are the features of the real-time clock.

- 16-bit up-counter
  - 16-bit modulo match limit
  - Software controllable periodic interrupt on match
- Software selectable clock sources for input to prescaler with programmable 16 bit prescaler
  - OSC 32.768 kHz nominal
  - LPO (~1 kHz)
  - Bus clock
  - Internal reference clock

3.5.5.4 Pulse Width Timer (PWT)

The pulse width timer (PWT) includes the following features:

- Automatic measurement of pulse width with 16 bit resolution
- Separate positive and negative pulse width measurements
- Programmable triggering edge for starting measurement
- Programmable measuring time between successive alternating edges, rising edges or falling edges
- Programmable prescaler from clock input as 16 bit counter time base
- Two selectable clock sources, supporting separate timer clock up to 48 MHz
- Four selectable pulse inputs
- Programmable interrupt generation upon pulse width value updated and counter overflow

3.5.6 Communication interfaces

3.5.6.1 Inter-Integrated Circuit (I^2C)

The features of the I^2C module are as follows.

- Compatible with I^2C bus standard
- Up to 100 kbit/s with maximum bus loading
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt-driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low-power mode.
- I2C0 supports 4-wire interface

3.5.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The UART module has the following features.

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Programmable 1-bit or 2-bit stop bits
- Receiver wake-up by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

3.5.6.3 Serial Peripheral Interface (SPI)

The features of the SPI module are listed below.

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during Wait mode
- Selectable MSB-first or LSB-first shifting
- Receive data buffer hardware match feature

3.5.6.4 Freescale's scalable controller area network (MSCAN)

The features of the MSCAN module are listed below.

- Implementation of the CAN protocol - Version 2.0A/B
  - Standard and extended data frames
  - Zero to eight bytes data length Introduction
  - Programmable bit rate up to 1 Mbps[1]
  - Support for remote frames
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization using a "local priority" concept
- Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, or four 16-bit filters, or eight 8-bit filters
- Programmable wake-up functionality with integrated low-pass filter
- Programmable loopback mode supports self-test operation
- Programmable listen-only mode for monitoring of CAN bus
- Programmable bus-off recovery functionality
- Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
- Programmable MSCAN clock source either bus clock or oscillator clock
- Internal timer for time-stamping of received and transmitted messages
- Three low-power modes: sleep, power down, and MSCAN enable
- Global initialization of configuration registers

3.5.7 Human machine interface

3.5.7.1 General-Purpose Input/Output (GPIO)

The features of the GPIO module are listed below.

- Hysteresis and configurable pull up device on all input pins
- Configurable drive strength on some output pins
- Independent pin value register to read logic level on digital pin
- Fast IO access in single-cycle core clock

3.5.7.2 Keyboard Interrupts (KBI)

The KBI features include:

- Up to 32 keyboard interrupt pins with individual pin enable bits
- Each keyboard interrupt pin is programmable as:
  - falling-edge sensitivity only
  - rising-edge sensitivity only
  - both falling-edge and low-level sensitivity
  - both rising-edge and high-level sensitivity
- One software-enabled keyboard interrupt
- Exit from low-power modes

1. Depending on the actual bit timing and the clock jitter of the clock source.

4 Power modes

The power management controller (PMC) provides the user with multiple power options. The different modes of operation are supported to allow the user to optimize power consumption for the level of functionality needed.

The device supports Run, Wait, and Stop modes which are easy to use for customers both from different power consumption level and functional requirement. I/O states are held in all the modes.

- Run mode—CPU clocks can be run at full speed and the internal supply is fully regulated.
- Wait mode—CPU shuts down to conserve power; system clocks and bus clock are running and full regulation is maintained.
- Stop mode—LVD optional enabled, and voltage regulator is in standby.

The three modes of operation are Run, Wait, and Stop. The WFI instruction invokes both Wait and Stop modes for the chip.

Table 5. Chip power modes

Power mode	Description	Core mode	Normal recover method
Normal RUN	Allows maximum performance of chip. Default mode out of reset; on-chip voltage regulator is on.	Run	—
Normal Wait via WFI	Allows peripherals to function while the core is in Sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt
Normal Stop via WFI	Places chip in static state. Lowest power mode that retains all registers while optionally maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Sleep Deep	Interrupt

5 Revision history

The following table provides a revision history for this document.

Table 6. Revision history

Rev. No.	Date	Substantial Changes
2	3/2014	Initial public release

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