MCF51CN128PP
Rev. 3, 1/2009

MCF51CN128 Family Product Brief

32-bit Low-Cost, Low-Power, High-Performance Version 1 ColdFire® Microcontroller with Ethernet

The MCF51CN128 device is a 32-bit ColdFire V1 microcontroller (MCU) with up to 128 KB flash memory and a 12-channel, 12-bit analog-to-digital converter (ADC). It also features 10/100 BASE-T/TX fast ethernet controller (FEC), media independent interface (MII) to connect an external physical transceiver (PHY), and multi-function external bus interface. MCF51CN128 also highlights multiple communication interfaces for various ethernet gateway applications.

MCF51CN128 is the first ColdFire V1 device to incorporate ethernet and external bus interface along with new features to minimize power consumption and increase functionality within low power modes.

Not all features are available in all devices or packages; see Table 1 for details.

Table of Contents

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1 Application Examples

MCF51CN128 series MCUs are general-purpose devices suitable for a range of applications, including:

- Wireless picture frame
- Ethernet to POTS
- Home HeartBeat
- Health Monitor
- Glucose Meter
- Hotel Room Access
- Building Access/Monitor
- Cash Handling Safe
- Utility Power Control
- Electric Meter Monitor
- PLC high speed serial
- Fast food cooker/warmer
- HVAC monitor
- Hospital Bed Interface

2 Features

Table 1 describes the key features of the MCF51CN128 series.

Table 1. MCF51CN128 Series Features by MCU and Package

Feature	MCF51CN128		
	80-pin	64-pin	48-pin
Flash memory size (KB)	128		
RAM size (KB)	24		
V1 ColdFire core equiped with BDM (background debug module) and 2X3 Crossbar switch	Yes		
ADC (analog-to-digital converter) channels (12-bit)	12		
FEC (Fast Ethernet Controller with MII Interface)	Yes		
COP (computer operating properly)	Yes		
IIC1 (inter-integrated circuit)	Yes		
IIC2	Yes		
IRQ (interrupt request input)	Yes		
KBI (keyboard interrupts)	16	12	6
LVD (low-voltage detector)	Yes		
MCG (multipurpose clock generator)	Yes		
Port I/O[1]	70	54	38

Table 1. MCF51CN128 Series Features by MCU and Package (Continued)

Feature	MCF51CN128		
	80-pin	64-pin	48-pin
RGPIO (rapid general-purpose I/O)	16	16	8
RTC (real-time counter)	Yes		
SCI1, SCI2 & SCI3 (serial communications interface)	Yes		
SPI1 & SPI2 (serial peripheral interface)	Yes		
TPM1 (Timer/PWM Module) channels	3	3	3
TPM2 channels	3	3	3
MTIM1 & MTIM2	Yes[2]		
External Timer Clocks	2	1	1
Mini-FlexBus	Yes	0	0
XOSC (crystal oscillator)	Yes		

1 All GPIO are muxed with other functions

2 TMRCLK2 is not available on the 48 pin package, although MTIM2 can be used as an internal timebase using on-chip clock sources.

2.1 Block Diagram

Figure 1 shows a top-level block diagram for the MCF51CN128.

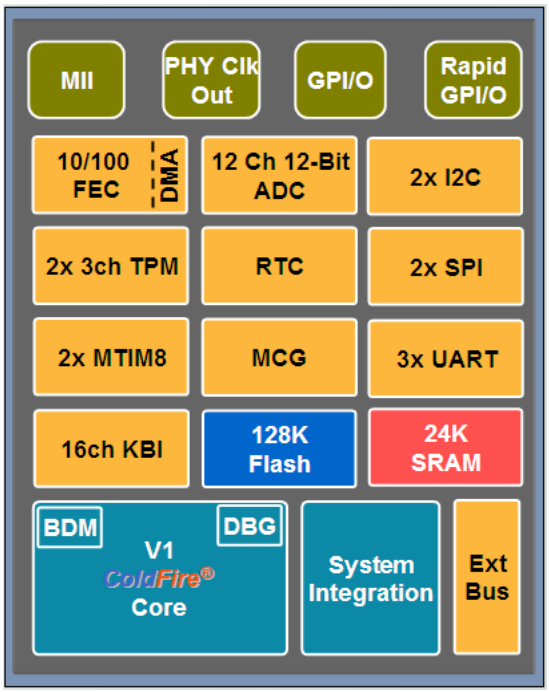

Figure 1. MCF51CN128 Series Block Diagram

2.2 Critical Performance Parameters

This section describes the critical performance parameters of the MCF51CN128 series.

- Operating voltage (V_{DD}) of 1.8 V to 3.6 V
- Operating temperature (T_A) of –40 °C to 85 °C
- Bus frequency (f_{Bus})
  - 3.0 V < V_{DD} < 3.6 V, DC, 50.33 MHz
  - 2.1 V < V_{DD} < 3.0 V, DC, 40 MHz
  - 1.8 V < V_{DD} < 2.1 V, DC, 20 MHz
- Packaging
  - 80-LQFP, case 917A, 14 mm × 14 mm
  - 64-LQFP, case 840F, 10 mm × 10 mm
  - 48-QFN, case 1314, 7 mm × 7 mm

2.3 Chip-Level Features

- Up to 50.33 MHz ColdFire CPU from 3.6 V to 3.0 V, up to 40 MHz CPU from 3.0 V to 2.1 V, and up to 20 MHz CPU from 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
- Flash read/program/erase over full operating voltage and temperature
- 128 KB flash, 24 KB RAM
- Security circuitry to prevent unauthorized access to Peripherals, RAM, and flash contents
- 10/100 BASE-T/TX, bus-mastering fast ethernet controller with direct memory access (DMA); supports half or full duplex
- Media independent interface to connect ethernet controller to external PHY
- Multi-function external bus interface
- Oscillator (XOSC)
  - Loop-control pierce oscillator
  - Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 25 MHz
- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Flash block protection
- Single-wire background debug interface
- 4 PC plus 2 address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
- 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Analog-to-digital converter (ADC) with 12-channel, 12-bit resolution
- Three serial communications interface (SCIs) modules with optional 13-bit break
- Two serial peripheral interfaces (SPIs) with full-duplex or single-wire bidirectional
- Two Inter-Integrated Circuits (IICs)
- Two timers/pulse width modulators (TPMs) with 3-channel and 16-bit resolution
- 8-bit real-time counter with binary or decimal-based prescaler
- Up to 70 GPIOs, all with pin mux controls to select alternate functions
- 16 keyboard interrupt (KBI) pins with selectable polarity
- 16 bits of Rapid GPIO connected to the CPU's high-speed local bus with set, clear, and toggle functionality

2.4 Module Features

This section provides more detail of the modules implemented on the MCF51CN128 series devices.

2.4.1 Version 1 ColdFire® Central Processor Unit (CPU)

- Up to 50.33 MHz ColdFire CPU from 3.6 V to 3.0 V, up to 40 MHz CPU from 3.0 V to 2.1 V, and up to 20 MHz CPU from 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
- Provides 0.94 Dhrystone 2.1 MIPS per MHz performance when running from internal RAM (0.76 DMIPS/MHz from flash)
- ColdFire Instruction Set Revision C (ISA_C)
- Support for up to 45 peripheral interrupt requests and 7 software interrupts

2.4.2 On-Chip Memory

- 128 KB flash, 24 KB RAM
- Flash read/program/erase over full operating voltage and temperature
- On-chip memory aliased to create a contiguous memory space with off-chip memory
- Security circuitry to prevent unauthorized access to RAM and flash contents

2.4.3 Ethernet

- FEC — 10/100 BASE-T/TX, bus-mastering fast ethernet controller with direct memory access (DMA); supports half or full duplex
- MII — media independent interface to connect ethernet controller to external PHY; includes output clock for external PHY

2.4.4 External Bus

- Mini-FlexBus — Multi-function external bus interface; supports up to 1 MB memories, gate-array logic, simple slave device or glueless interfaces to standard chip-selected asynchronous memories
- Programmable options: access time per chip select, burst and burst-inhibited transfers per chip select, transfer direction, and address setup and hold times

2.4.5 Power-Saving Modes

- Two low-power stop modes, one of which allows limited use of some peripherals (ADC, KBI, RTC)
- Reduced-power wait mode shuts off CPU and allows full use of all peripherals; FEC can remain active and conduct DMA transfers to RAM and assert an interrupt to wake up the CPU upon completion
- Low-power run and wait modes allow peripherals to run while the voltage regulator is in standby
- Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- Low-power external oscillator that can be used in stop3 mode to provide accurate clock source to active peripherals

- Low-power real-time counter for use in run, wait, and stop modes with internal and external clock sources
- 6 µs typical wake-up time from stop3 mode
- Pins and clocks to peripherals not available in smaller packages are automatically disabled for reduced current consumption; no user interaction is needed

2.4.6 Clock Source Options

- Oscillator (XOSC)
  - Loop-control pierce oscillator
  - Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 25 MHz
- Multi-Purpose Clock Generator (MCG)
  - Flexible clock source module with either frequency-locked-loop (FLL) or phase-lock loop (PLL) clock options
  - FLL can be controlled by internal or external reference and includes precision trimming of internal reference, allowing 0.2% resolution and 2% deviation over temperature and voltage
  - PLL derives a higher accuracy clock source derived by an external reference

2.4.7 System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode and illegal address detection with programmable reset or exception response
- Flash block protection

2.4.8 Analog-to-Digital Converter (ADC)

- Up to 12 channel, 12-bit resolution;
- 2.5 µs conversion time
- Automatic compare function
- 1.7 mV/°C temperature sensor
- Internal bandgap reference channel
- Operation in stop3
- Fully functional from 3.6 V to 1.8 V

2.4.9 Serial Communication Interfaces (SCI)

- Three modules with optional 13-bit break

2.4.10 Serial Peripheral Interfaces (SPI)

- Two interfaces with full-duplex or single-wire bi-directional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting

2.4.11 Inter-Integrated Circuits (IIC)

- Two IICs with up to 100 kbps with maxmimum bus loading
- Multi-master operation
- Programmable slave address
- Interrupt-driven byte-by-byte data transfer
- Supports broadcast mode and 11-bit addressing

2.4.12 Timers/Pulse-Width Modulators (TPM)

- Two 3-channel, 16-bit resolution timer pulse-width modulator modules
- Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel

2.4.13 Real-Time Counter (RTC)

- 8-bit modulus counter with binary- or decimal-based prescaler
- External clock source for precise time base, time-of-day, calendar- or task-scheduling functions
- Free-running on-chip low-power oscillator (1 kHz) for cyclic wake-up without external components
- Runs in all MCU modes

2.4.14 Modulo Timer (MTIM)

- Two 8-bit resolution modulo timers with 8-bit prescaler

2.4.15 Input/Output

- Up to 70 general-purpose input/output (GPIO) pins, all with pin mux controls to select alternate functions
- 16 keyboard interrupt (KBI) pins with selectable polarity
- Hysteresis and configurable pull-up device or input filtering on all input pins; configurable slew rate and drive strength on all output pins
- 16 Rapid GPIO pins connected to the CPU's high-speed local bus with set, clear, and toggle functionality (PTD and PTF)

3 Developer Environment

- Single-wire background debug module (BDM) interface; supports same electrical interface used by the S08 family debug modules
- 4 PC plus 2 address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
- 64-entry processor status and debug data trace buffer with programmable start/stop conditions

4 Part Numbers

Table 2. Orderable Part Number Summary

Freescale Part Number[1]	Memory		Temperature Range (°C)	Package
	Flash	RAM		
PCF51CN128CLK	128K	24K	-40 to +85	80-pin LQFP
PCF51CN128CLH	128K	24K	-40 to +85	64-pin LQFP
PCF51CN128CGT	128K	24K	-40 to +85	48-pin QFN

1 See the reference manual, *MCF51CN128RM*, for a complete description of modules included on each device.

5 Revision History

Table 3. Revision History

Rev.	Date	Description of Change
1	August 2008	Alpha Customer Release.
2	January 2009	Pre-Launch Release.
3	January 2009	Launch Release.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
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