MCF5213 Reference Manual Errata

Supported Devices: MCF5211, MCF5212, MCF5213

by: Microcontroller Solutions Group

This errata document describes corrections to the *MCF5213 Reference Manual*, order number MCF5213RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/coldfire for the latest updates.

The current available version of the *MCF5213 Reference Manual* is Revision 5.

Contents

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1 Errata for Revision 5

Table 1. MCF5213RMAD Reference Manual Rev 5 Errata

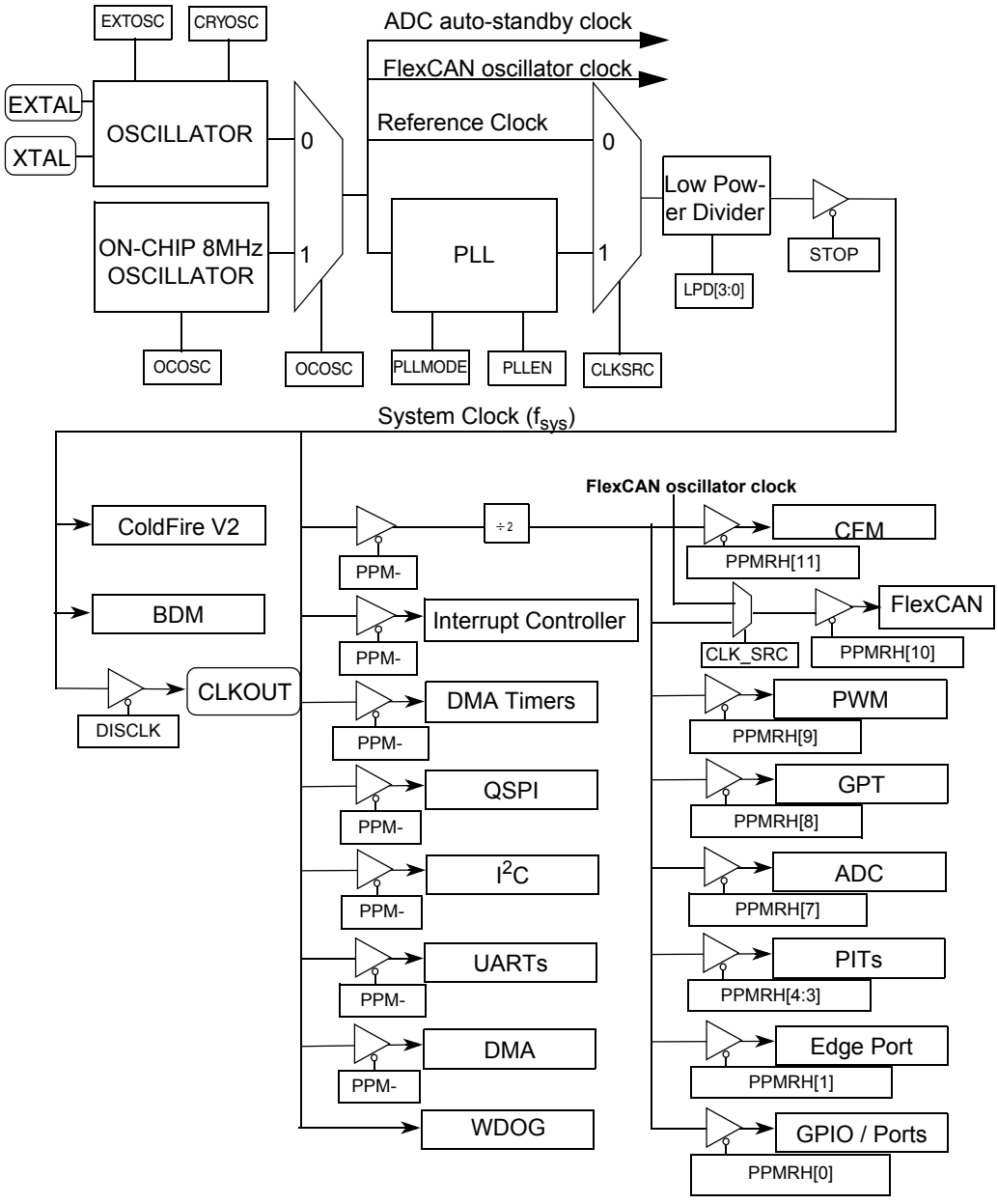
Location	Description
Chapter “Clock Module”/Section “Block Diagram”/Figure “ Clock Module Block Diagram”	Updated the Figure ”Clock Module Block Diagram” by adding a clock mux component controlled by the CANCTRL[CLK_SRC] bit that indicates which clock (system clock/2 or FlexCAN oscillator clock) feeds the FlexCAN module 

Table 1. MCF5213RMAD Reference Manual Rev 5 Errata (continued)

Location	Description
Chapter “FlexCAN” Section “FlexCAN Control Register (CANCTRL)” /Table “CANCTRL Field Descriptions”	Change from: $\text{S clock frequency} = \frac{f_{sys} \text{ or EXTAL}}{\text{PRESDIV} + 1}$ Change to: $\text{S clock frequency} = \frac{f_{sys/2} \text{ or FlexCAN oscillator clock}}{\text{PRESDIV} + 1}$
Chapter “FlexCAN” Section “FlexCAN Control Register (CANCTRL)” /Table “CANCTRL Field Descriptions”	In the Description of field 13 CLK_SRC bit Change from: 0 Clock source is EXTAL 1 Clock source is the internal bus clock, fsys Change to: 0 Clock source is FlexCAN oscillator clock 1 Clock source is the internal bus clock, fsys/2
Chapter “FlexCAN” /Section “Protocol Timing”/Figure “CAN Engine Clocking Scheme”	Change from: $f_{Tq} = \frac{f_{sys} \text{ or EXTAL}}{(\text{PRESDIV} + 1)}$ Change to: $f_{Tq} = \frac{f_{sys/2} \text{ or FlexCAN oscillator clock}}{\text{PRESDIV} + 1}$

2 Errata for Revision 3

Table 2. MCF5213RM Rev 3 Errata

Location	Description
Section 1.4, “Features”/Page 7	In clock generation features: • Replaced “One to 48 MHz crystal, 8 MHz on-chip trimmed relaxation oscillator, or external oscillator reference options” with “Crystal, on-chip relaxation oscillator, or external oscillator reference options”. • Updated “Two to 10 MHz reference frequency for normal PLL mode with a pre-divider programmable from 1 to 8” with “Two to 10 MHz reference frequency for normal PLL mode”.
Section 6.2, “Features”/Page 81	Replaced “1- to 16-MHz crystal, 8-MHz on-chip relaxation oscillator, or external oscillator reference options” with “Crystal, on-chip relaxation oscillator, or external oscillator reference options.”
Throughout	Formatting, layout, spelling, and grammar corrections.
Table 2-1 / Page 2-3	Synchronized the table in the reference manual and the device data sheet.
Section 10.5.4 / Page 10-7	Updated the section to reflect the fact that the CWT does not cause a hardware reset.
Table 10-6 / Page 10-8	In the CWCR[CWRI] field description, changed “The interrupt level for the CWT is programmed in the interrupt control register 7 (ICR7)...” to “The interrupt level for the CWT is programmed in the interrupt control register 8 (ICR8)...”.
Section 12-1 / Page 12-2	Deleted the sentence beginning with “For many peripheral devices...”.
Table 12-2 / Page 12-5	Deleted the entry for the (nonexistent) GSWIACK register.
Section 12.3.8 / Page 12-16	Deleted references to the (nonexistent) GSWIACK register.
Section 14.4 / Page 14-12	Deleted the sentence “BCR*n* decrements when an address transfer write completes for a single-address access (DCR*n*[SAA] = 0), or when SAA equals 1.”
Section 10.7.3.1 / Page 10-14	• Rewrote the introductory text describing the MPR (removing erroneous reference to a fast Ethernet controller). • Corrected the MPR reset value (was 0x11, is 0x1).
Figure 21-6 / Page 21-9	Added a note to clarify the UCSR*n* reset values.
Figure 21-20 / Page 21-20	• Corrected the label of the top signal (was U*n*TXD, is U*n*RXD). • Corrected the text in the footnote (was TXRTS, is RXRTS).
Figure 21-23 / Page 21-23	Corrected the U*n*TXD label (was “Input”, is “Output”).
Figure 21-24 / Page 21-24	• Corrected a label on the bottom row (was UMR1*n*[PT]=2, is UMR1*n*[PT]=1). • Deleted duplicate UMR1*n*[PM]=11 label.
Section 24.3.2.5.1 / Page 24-17	Corrected the numerical values in the left-aligned example.
Section 24.3.2.6.1 / Page 24-19	Corrected the numerical values in the center-aligned example.
Appendix A	Deleted the entry for the (nonexistent) GSWIACK register.
Throughout	Formatting, layout, spelling, and grammar corrections.
Table 1-1 / Page 1-2	Added the following footnote to the MCF5211 FlexCAN entry: “FlexCAN is available on the MCF5211 only in the 64 QFN package.”
Table 2-1 / Page 2-3	Changed the value in the “Pull-up/pull-down” column for $\overline{\text{IRQ2}}$-$\overline{\text{IRQ6}}$ (was “—”, is “pull-up”).

Table 2. MCF5213RM Rev 3 Errata (continued)

Location	Description
Table 3-1 / Page 3-3	• For the PC, changed the reset value (was “Undefined”, is “Contents of Location 0x0000_0004”) and the “Written with MOVEC entry” value (was “Yes”, is “No”). • Changed the reset value for the OTHER_A7 (was “Undefined”, is “Contents of Location 0x0000_0000”). • Changed the reset value for the RAMBAR (was “0x0000_0000”, is “See Section”).
Figure 3-5 / Page 3-5	• Modified the figure to show that Bits 4:0 are read/write. • Changed the access (was “Access: User read-only”, is “Access: User read/write”).
Table 3-2 / Page 3-6	Removed the last sentence in the C bit field description.
Figure 3-7 / Page 3-6	Updated the figure to show that bits 19:0 are read-only.
Figure 3-8 / Page 3-7	Updated the figure to show that bits 4:0 are read/write.
Section 3.4 / Page 3-9	Changed the last sentence in step 2 to “The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address”.
Table 5-1 / Page 5-2	Changed the RAMBAR reset value (was “0x0000_0000”, is “See Section”).
Section 5.2.1 / Page 5-2	• Corrected section to show the proper RAMBAR figure and field description table. • Changed the last bullet to “A reset clears the RAMBAR’s priority, backdoor write-protect, and valid bits, and sets the backdoor enable bit. This enables the backdoor port and invalidates the processor port to the SRAM. (The RAMBAR must be initialized before the core can access the SRAM.) All other bits are unaffected.”.
Table 7-2 / Page 7-2	Deleted superfluous table.
Section 7.2.4.1 / Page 7-9	• Updated LPCR figure and field description table to include correct information about the STPMD (bits 4:3) and LVDSE (bit 1) fields. • Corrected section number (was fourth-level heading, is third-level heading).
Table 8-3 / Page 8-3	Updated the CIR memory map entry to show that the CIR reset value is device-dependent.
Figure 8-3 / Page 8-4	Added a footnote to clarify that the CIR reset value is device-dependent.
Table 10-1 / Page 10-2	Added missing PACR*n* addresses.
Figure 10-4 / Page 10-7	Corrected name of bit 0 (was CWTIC, is CWTIF).
Table 10-12 / Page 10-15	Added an entry for PACR5 and a footnote to clarify the meaning of “—”.
Table 14-4 / Page 14-8	Deleted erroneous reference to nonexistent AT bit.
Figure 15-3 / Page 15-5	Updated the FLASHBAR figure to show that WP is read-only, and added footnote to explain that the value of WP is determined at power-on reset.
Section 18.6.13 / Page 18-12	Deleted erroneous references to nonexistent CF bits in the figure and bit descriptions for the GPTFLG2 register.
Figure 20-1 / Page 20-1	Corrected signal name (was QSPI_CS[:0], is QSPI_CS[3:0]).
Section 21.2 / Page 21-3	Changed "An internal interrupt request signal notifies the interrupt controller..." to "A request signal is provided to notify the interrupt controller...".
Table 21-6 / Page 21-9	Changed “DTIN” to “DT*n*IN” (to maintain consistent signal names throughout chapter).
Section 21.4.5.2 / Page 21-26	Changed "...complete normally without exception processing..." to "...complete normally without an error termination...".

Table 2. MCF5213RM Rev 3 Errata (continued)

Location	Description
Chapter 23	• Reorganized information throughout entire chapter. • Converted register field descriptions to SRS format. • Corrected register mnemonics as necessary to ensure consistent register naming. • Numerous grammar and stylistic corrections.
Chapter 24	Updated chapter to reflect the correct number of PWM channels (was 4, is 8).
Section 24.3.2.5.1 / Page 24-17	Added missing numerical values to the output example.
Section 24.3.2.6.1 / Page 24-19	Added missing numerical values to the output example.
Table 24-1 / Page 24-2	Deleted reference to nonexistent SCMISR register from footnote 2.
Table 26-4 / Page 26-6	Changed the reset values for PBR1, PBR2, and PBR3 (was “Undefined”, is “See Section”).
Table 26-10 / Page 26-16	• Added the following note to the PBR0[Address] field description: **Note:** PBR0[0] should always be loaded with a 0. • Changed the bit range in the Field column (was 31–1, is 31–0).
Figure 26-8 / Page 26-16	Changed the address of PBR3 (was 0x1C, is 0x1B).
Table 26-22 / Page 26-38	Changed the initial state of the CSR (was 0x0, is 0x0090_0000).
Section 26.6.2 / Page 26-42	Added the following note at the end of this section: The debug module requires the use of the internal bus to perform BDM commands. For this processor core, if the processor is executing a tight loop that is contained within a single aligned longword, the processor may never grant the internal bus to the debug module, for example: align4 label1: nop bra.b label1 or align4 label2: bra.w label2 The processor grants the internal bus if these loops are forced across two longwords.
Figure 27-3 / Page 27-5	Updated the IDCODE register figure to indicate that the reset values for both PRN and PIN are device-dependent.
Appendix A	• Corrected PACR*n* addresses. • Added CFMCLKSEL register.

3 Errata for Revision 2

Table 3. MCF5213RM Rev 2 Errata

Location	Description
Throughout	Formatting, layout, spelling, and grammar corrections.
Figure 1-1 / Page 1-3	Corrected signal names to match those in Table 1 in Chapter 2.
Figure 2-1 / Page 2-2	Corrected signal names to match those in Table 1.
Table 1 / Section 2.2	• Changed label to Table 2-1. • Added overbars to names of active-low signals.
Section 3.2.9 / Page 3-7	Added cross-reference to FLASHBAR register.

Table 3. MCF5213RM Rev 2 Errata (continued)

Location	Description
Section 3.4 / Page 3-9	• Changed the last bullet to “Use of separate system stack pointers for user and supervisor modes”. • Deleted the sentences beginning with “Processors implementing ISA_A...” and “As a result, the exception stack frame...”. • Deleted the text “For processors implementing all other ISA revisions and supporting 2 stack pointers”.
Section 3.6.2 / Page 3-12	Added text clarifying address errors occurring on JSR and RTS instructions.
Chapter 4	Content updates and enhancements throughout chapter.
Section 5.1.1 / Page 5-1	Corrected SRAM size.
Section 5.1.2 / Page 5-1	Removed text “...within the 256-MByte address space (0x8000_0000-0x8FFF_FFFF)”.
Table 5-2 / Page 5-2	Removed text “...within the processor’s 256-MByte address space...” and “For proper operation, the base address must be set to between 0x8000_0000 and 0x8FFF-8C000.”.
Table 6-6 / Page 6-7	Added footnote 3 - “Default value out of reset” - to reflect correct reset values of MFD (0b001) and RFD (0b000).
Figure 10-8 / Page 10-13	Marked bits 17-16 as reserved to match the correct description in Table 10-7.
Chapter 11	• Corrected register addresses to include proper offset (IPSBAR+0x10_....). • Updated register figures to SRS standards. • Added descriptive register figure titles and field description tables. • Corrected register mnemonics for the Port *n* pin data/set data registers. • Replaced incorrect Figure 11-25 with correct version (containing only PxPAR1 and PxPAR0). • In section 11.6.5, changed “If multiple pins are configured for the one function, then the rsult is undefined” to “Some signals can be assigned to different pins (see Table 2-1). However, a signal should not be assigned to more than one pin at the same time. If a signal is assigned to two or more pins simultaneously, the result is undefined.”
Chapter 14	• Revised Table 14-1 to reflect the structure of the BCR*n* and DSR*n* registers. • Updated register figures to include proper register names and addresses. • Combined Sections 14.3.4 and 14.3.4.1, and revised text to clarify the structure of the BCR*n* and DSR*n* registers. • Added missing figure and bit descriptions for the DCR*n* registers.
Chapter 15	Updated register figures to include correct register addresses.
Section 15.3 / Page 15-4	Added definition and description of FLASHBAR register.
Table 18-3 / Page 18-5	Deleted entry for nonexistent GPTTST register.
Figure 18-21	Updated figure appearance to match document convention.
Figure 21-6 / Page 21-8	Updated figure with correct register mnemonics (USR0...2).
Equation 21-1 / Page 21-19	Corrected numerator of equation (was $f_{sys/2}$, is f_{sys}).
Chapter 23	Deleted superfluous Table 23-5.
Section 23.5.7 / Page 23-32	Deleted extraneous sentence at end of first paragraph.
Chapter 25	Corrected register addresses throughout.
Figure 25-9 / Page 25-14	Corrected register mnemonic (was CANCTRL, is ERRSTAT).
Chapter 26	Content updates and enhancements throughout chapter.

Table 3. MCF5213RM Rev 2 Errata (continued)

Location	Description
Appendix A	• Deleted entries for CACR, ACR0, and ACR1 registers. • Corrected PPMRH and PPMRL addresses (IPSBAR+0x000C and IPSBAR+0x0018, respectively). • Added leading zeros to addresses as necessary to adhere to four-digit address convention. • Added RAMBAR register. • Corrected misspelling of IPSBAR in address for the ICR034 and GPTACFORC registers. • Changed mnemonic of register ICR45 to ICR045. • Added ICR016 and ICR063 registers. • Added global software and level *n* interrupt acknowledge registers. • Corrected several typos in port pin data / set data register mnemonics. • Corrected addresses of the LPDR, EPDR, EPFR, and GPTAPACNT registers. • Corrected addresses of the DMA controller module registers to match the values in the text. • Corrected general purpose timer register mnemonics (begin with GPT instead of GPTA). • Corrected size of the pulse accumulator counter register (16 bits instead of 8). • Deleted spaces in the mnemonics for the programmable interrupt controller registers. • Added pulse width modulation channel duty and shutdown registers.

4 Revision History

Table 4 provides a revision history for this document.

Table 4. Revision History Table

Rev. Number	Substantive Changes	Date of Release
2	Initial release, incorporating corrections listed in Table 3.	10/2006
3	Various technical and other corrections as described in Table 2.	03/2007
4	• Various technical and other corrections as described in Table 2. • Added missing corrections against the following entities to Table 2: Table 3-1 Figure 3-5 Table 3-2 Figure 3-7 Figure 3-8 Section 3.4 Table 5-1 Section 5.2.1 Table 26-4 Table 26-10 Figure 26-8 Table 26-22 Section 26.6.2 • Added missing corrections against the following entities to Table 3: Section 3.4 Section 3.6.2	04/2010
5	Corrected errors in Chapter “Clock Module” and “FlexCAN”	11/2011

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