Freescale Semiconductor
Addendum

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Rev. 1.2, 05/2009

Errata to MPC8533E PowerQUICC™ III Integrated Host Processor Family Reference Manual, Rev. 1

This errata describes corrections to the *MPC8533E PowerQUICC™ III Integrated Host Processor Family Reference Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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4.3.1.1.2/4-5	In Table 4-5, “CCSRBAR Bit Settings,” added clarification for BASE_ADDR from: “Identifies the16 most-significant address bits of the window” to” “Identifies the16 most-significant address bits of the 36-bit window”
4.4.3.1/4-11	Removed sentence, “There is no default value for this PLL ratio; these signals must be pulled to the desired values.”
4.4.3.1/4-12	In Table 4-9, “CCB Clock PLL Ratio,” in Functional Signals column, removed “no default” designation for System PLL Ratio POR configuration signals. Designated “default (1111).”
4.4.3.2/4-12	Removed sentence, “There is no default value for this PLL ratio; these signals must be pulled to the desired values.”
4.4.3.2/4-12	In Table 4-10, “e500 Core Clock PLL Ratios,” made the following changes: • In Functional Signals column, removed “no default” designation for e500 Core PLL Ratio POR configuration signals. Designated “default (111).” • In the e500 : CCB Clock Ratio column, for the value 010, changed from a 1:1 ratio to "Reserved."
4.4.4.2.1/4-22	Appended the following sentence to the first paragraph and deleted the remainder of the section: “Please refer to the *MPC8533E Integrated Processor Hardware Specifications*, for specific supported frequencies.”
6.10.2/6-26	In Figure 6-33, “Hardware Implementation-Dependent Register 1 (HID1),” changed access from “Supervisor read/write” to “Supervisor mixed.”
7.3/7-9	In Table 7-3, “L2/SRAM Memory-Mapped Registers,” updated (swapped) offsets of L2ERRADDRH and L2ERRADDRL to read as follows... L2ERRADDRL at 0x20E50 L2ERRADDRH at 0x20E54
7.2/7-9, 7-10	Updated reset value of L2CTL from 0x2000_0000 to 0x1000_0000 in Table 7-3, “L2/SRAM Memory-Mapped Registers,” and in Figure 7-7, “L2 Control Register. In particular, L2CTL[L2SIZ] reset value has changed from 10 to 01.
7.3.1.4.2, 7-24	In Figure 7-23, “L2 Error Address Capture Register (L2ERRADDRH),” changed the offset for L2ERRADDRH to 0x2_0E54.
7.3.1.4.2, 7-25	In Figure 7-24, “L2 Error Address Capture Register (L2ERRADDRL),” changed the offset for L2ERRADDRL to 0x2_0E50.
9.3.2.1/9-7	In Table 9-3, “Memory Interface Signals—Detailed Signal Descriptions,” changed signal description of MA[15:0] to the following :

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	"Assertion/Negation—The address lines are only driven when the controller has a command scheduled to issue on the address/CMD bus; otherwise they will be at high-Z. It is valid when a transaction is driven to DRAM (when $\overline{\text{MCS}}n$ is active)."
9.3.2.2/9-9	In Table 9-4, "Clock Signals—Detailed Signal Descriptions," updated MCKE description to added the following : "The MCKE signals should be connected to the same rank of memory as the corresponding MCS and MODT signals. For example, MCKE[0] should be connected to the same rank of memory as MCS[0] and MODT[0]."
9.4.1.7/9-20	In Table 9-12, "DDR_SDRAM_CFG Field Descriptions," in 8_BE field description, updated note as follows: "DDR1 (SDRAM_TYPE = 010) must use 8-beat bursts when using 32-bit bus mode (32_BE = 1) and 4-beat bursts when using 64-bit bus mode; DDR2 (SDRAM_TYPE = 011) must use 4-beat bursts, even when using 32-bit bus mode."
9.4.1.7, 9-21	In Table 9-12, "DDR_SDRAM_CFG Field Descriptions," replaced the description of DDR_SDRAM_CFG[ECC_EN] with the following:

Table 9-12. DDR_SDRAM_CFG Field Descriptions

Bits	Name	Description
2	ECC_EN	ECC enable. Note that uncorrectable read errors may cause the assertion of *core_fault_in*, which causes the core to generate a machine check interrupt unless it is disabled (by clearing HID1[RFXE]). If RFXE is cleared and this error occurs, ERR_DISABLE[MBED] must be cleared and ECC_EN and ERR_INT_EN[MBEE] must be set to ensure that an interrupt is generated. See Section 6.10.2, "Hardware Implementation-Dependent Register 1 (HID1)." 0 No ECC errors are reported. No ECC interrupts are generated. 1 ECC is enabled.

9.4.1.7/9-22	In Table 9-12, "DDR_SDRAM_CFG Field Descriptions," added new programming requirement for DDR_SDRAM_CFG[HSE] such that this bit should not be set if using automatic calibration.
9.4.1.26, 9-37	In Table 9-32, "ERR_DISABLE Field Descriptions," replaced the description of ERR_DISABLE[MBED] with the following:

Table 9-32. ERR_DISABLE Field Descriptions

Bits	Name	Description
28	MBED	Multiple-bit ECC error disable 0 Multiple-bit ECC errors are detected if DDR_SDRAM_CFG[ECC_EN] is set. They are reported if ERR_INT_EN[MBEE] is set. Note that uncorrectable read errors cause the assertion of *core_fault_in*, which causes the core to generate a machine check interrupt, unless it is disabled (by clearing HID1[RFXE]). If RFXE is zero and this error occurs, MBED must be cleared and DDR_SDRAM_CFG[ECC_EN] and ERR_INT_EN[MBEE] must be set to ensure that an interrupt is generated. 1 Multiple-bit ECC errors are not detected or reported.

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9.4.1.26, 9-38 — In Table 9-33, “ERR_INT_EN Field Descriptions,” replaced the description of ERR_INT_EN[MBEE] with the following:

Table 9-32. ERR_DISABLE Field Descriptions

Bits	Name	Description
28	MBEE	Multiple-bit ECC error interrupt enable.Note that uncorrectable read errors may cause the assertion of *core_fault_in*, which causes the core to generate a machine check interrupt, unless it is disabled (by clearing HID1[RFXE]). If RFXE is zero and this error occurs, MBEE and ERR_DISABLE[MBED] must be zero and DDR_SDRAM_CFG[ECC_EN] must be set to ensure that an interrupt is generated. For more information, see Section 6.10.2, “Hardware Implementation-Dependent Register 1 (HID1).” 0 Multiple-bit ECC errors cannot generate interrupts. 1 Multiple-bit ECC errors generate interrupts.

9.5.6/9-59 — After the first paragraph, added the following note clarifying system board requirements when using registered DIMMs:

NOTE

Application system board must assert the reset signal on DDR memory devices until software is able to program the DDR memory controller configuration registers, and must deassert the reset signal on DDR memory devices before DDR_SDRAM_CFG[MEM_EN] is set. This ensures that the DDR memory devices are held in reset until a stable clock is provided and, further, that a stable clock is provided before memory devices are released from reset.

9.5.11/9-65 — Added the following text to the end of the section:

“In 32-bit mode, Table 9-50, “DDR SDRAM ECC Syndrome Encoding,” is split into 2 halves. The first half, consisting of rows 0–31, is used to calculate the ECC bits for the first 32 data bits of any 64-bit granule of data. This always applies to the odd data beats on the DDR data bus. The second half of the table, consisting of rows 32–63, is used to calculate the ECC bits for the second 32 bits of any 64-bit granule of data. This always applies to the even data beats on the DDR data bus.”

10.3.7.6/10-43 — Removed second sentence of first paragraph: “MIDR enables the user to direct the interrupt to either the external interrupt output pin ($\overline{\text{IRQ\_OUT}}$), the core’s critical interrupt input ($\overline{cint}$), or to its normal interrupt input ($\overline{int}$).”

11.3.1.2/11-6, 11-7 — In Figure 11-3, “I^2C Frequency Divider Register (I2CFDR),”changed reset value of I2CFDR to “All zeros,” and in Table 11-5, “I2CFDR Field Descriptions,” revised description of FDR field as follows:

<table>
<tr>
<td>2–7</td>
<td>FDR</td>
<td>Frequency divider ratio. Used to prescale the clock for bit rate selection. The serial bit clock frequency of SCL is either one third or one half the platform (CCB) clock divided by the designated divider, as determined by cfg_sec_freq (see Section 4.4.3.3, “SEC Frequency Ratio Configuration”). Note that the frequency divider value can be changed at any point in a program. The serial bit clock frequency divider selections are described as follows:
<table>
<tr><th>FDR</th><th>Divider (Decimal)</th><th>FDR</th><th>Divider (Decimal)</th><th>FDR</th><th>Divider (Decimal)</th></tr>
<tr><td>0x00</td><td>384</td><td>0x16</td><td>12288</td><td>0x2B</td><td>1024</td></tr>
<tr><td>0x01</td><td>416</td><td>0x17</td><td>15360</td><td>0x2C</td><td>1280</td></tr>
<tr><td>0x02</td><td>480</td><td>0x18</td><td>18432</td><td>0x2D</td><td>1536</td></tr>
<tr><td>0x03</td><td>576</td><td>0x19</td><td>20480</td><td>0x2E</td><td>1792</td></tr>
<tr><td>0x04</td><td>640</td><td>0x1A</td><td>24576</td><td>0x2F</td><td>2048</td></tr>
<tr><td>0x05</td><td>704</td><td>0x1B</td><td>30720</td><td>0x30</td><td>2560</td></tr>
<tr><td>0x06</td><td>832</td><td>0x1C</td><td>36864</td><td>0x31</td><td>3072</td></tr>
<tr><td>0x07</td><td>1024</td><td>0x1D</td><td>40960</td><td>0x32</td><td>3584</td></tr>
<tr><td>0x08</td><td>1152</td><td>0x1E</td><td>49152</td><td>0x33</td><td>4096</td></tr>
<tr><td>0x09</td><td>1280</td><td>0x1F</td><td>61440</td><td>0x34</td><td>5120</td></tr>
<tr><td>0x0A</td><td>1536</td><td>0x20</td><td>256</td><td>0x35</td><td>6144</td></tr>
<tr><td>0x0B</td><td>1920</td><td>0x21</td><td>288</td><td>0x36</td><td>7168</td></tr>
<tr><td>0x0C</td><td>2304</td><td>0x22</td><td>320</td><td>0x37</td><td>8192</td></tr>
<tr><td>0x0D</td><td>2560</td><td>0x23</td><td>352</td><td>0x38</td><td>10240</td></tr>
<tr><td>0x0E</td><td>3072</td><td>0x24</td><td>384</td><td>0x39</td><td>12288</td></tr>
<tr><td>0x0F</td><td>3840</td><td>0x25</td><td>448</td><td>0x3A</td><td>14336</td></tr>
<tr><td>0x10</td><td>4608</td><td>0x26</td><td>512</td><td>0x3B</td><td>16384</td></tr>
<tr><td>0x11</td><td>5120</td><td>0x27</td><td>576</td><td>0x3C</td><td>20480</td></tr>
<tr><td>0x12</td><td>6144</td><td>0x28</td><td>640</td><td>0x3D</td><td>24576</td></tr>
<tr><td>0x13</td><td>7680</td><td>0x29</td><td>768</td><td>0x3E</td><td>28672</td></tr>
<tr><td>0x14</td><td>9216</td><td>0x2A</td><td>896</td><td>0x3F</td><td>32768</td></tr>
<tr><td>0x15</td><td>10240</td><td></td><td></td><td></td><td></td></tr>
</table>
</td>
</tr>
</table>

11.3.1.5/11-10 In Table 11-8, “I2CDR Field Descriptions,” in DATA description, modified last sentence to say, “Note that in both master receive and slave receive modes, the very first read is always a dummy read.”

11.4.5, 11-17 Added detail regarding the inferface frequency in the second sentence of the first paragraph (begins “The boot sequencer accesses...”). The complete paragraph should read as follows:

“If boot sequencer mode is selected on POR (by the settings on the cfg_boot_seq[0:1] reset configuration signals, as described in Section 4.4.3.8, ‘Boot Sequencer Configuration’), the I^2C1 module communicates with one or more EEPROMs through the I^2C interface on IIC1_SCL and IIC1_SDA. The boot sequencer accesses the I^2C1 serial ROM device at a serial bit clock frequency equal to the platform (CCB) clock frequency divided by 3840. The EEPROM(s) can be programmed to initialize one or more configuration registers of this integrated device.”

11.5.4/11-23 In the second paragraph, removed the following sentence: “For 1-byte transfers, a dummy read should be performed by the interrupt service routine.”

Chapter 12 Replaced “CCB clock” with “platform clock,” for consistency throughout the book.

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12.2/12-13	In Table 12-3, “SEC Address Map,”corrected register ranges of AESU context registers and key memory registers in memory map as follows: • Context: 0x3_4100–0x3_4108→0x3_4100–0x3_4137 • Key memory: 0x3_4400–0x3_4408→0x3_4400–0x3_441F
12.4.6.9.2/12-76	Changed last sentence of first paragraph from The value of M is specified by writing to context register 3 as described in .... to The value of M is specified by writing to context register 7 as described in ....
12.4.7/12-90	In Section 12.4.7.14, “KEU Key Data Registers_1 and _2 (Confidentiality Key) (KEUKDn),” and Section 12.4.7.15, “KEU Key Data Registers _3 and _4 (Integrity Key) (KEUKDn),” changed all KEUKD*n* figures to write-only.
13.2/13-3	Consolidated this section to eliminate redundancy. Removed Table 13-1, “DUART Signal Overview,” because it was redundant with the information in the Signals chapter and in Table 13-2, “DUART Signals—Detailed Signal Desriptions.”
14.3.1.15/14-30	In Table 14-21, “LBCR Field Descriptions,” changed the AHD field (bit 10) state description, as follows: 0 During address phases on the local bus, the LALE signal negates one platform clock period prior to the address being invalidated. At 33.3 MHz, this provides 3 ns of additional address hold time at the external address latch. 1 During address phases on the local bus, the LALE signal negates 0.5 platform clock period prior to the address being invalidated. This halves the address hold time, but extends the latch enable duration. This may be necessary for very high frequency designs.
14.4.4/14-58	Added the following statement to end of first paragraph: “A gap of 2 dead LCLK cycles is present on the UPM interface between UPM transactions.”
14.4.4.2/14-62	Added the following RAM word programming guidelines to the end of this section: For proper signalling, the following guidelines must be followed while programming UPM RAM words: For UPM reads, program UTA and LAST in the same or consecutive RAM words. For UPM burst reads, program last UTA and LAST in the same or consecutive RAM words. For UPM writes, program UTA and LAST in the same RAM word. For UPM burst writes, program last UTA and LAST in the same RAM word.
14.4.4.4.1/14-65	In Table 14-28, “RAM Word Field Descriptions,” added the following note for the LOOP and AMX fields: “**Note:** AMX must not change values in any RAM word which begins a loop.”

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14.4.4.4.7/14-70	Added the following note at the end of the section: **NOTE** AMX must not be changed from its previous value in any RAM word which begins a loop.
14.5.3/14-83	Added the following note after the first paragraph: “It may not be possible to write to 16-bit devices on the local bus using 16-bit transactions on one of the external peripheral interfaces. Refer to the chapter describing the specific external interface controller for more information.”
14.5.6.2.2/ 14-105	In paragraph beginning, “The remaining issue is the synchronization of the UPM cycles...” changed parenthetical element in final sentence from (GPL[0:4] are 1 when inactive, GPL5 is 0 when inactive) to (LGPL*n* are 1 when inactive)
15.3/5-4	Modified first bullet, removing specific maximum data clock frequency ratios; referring reader to the device hardware specificiations document for specific maximum frequencies.
15.4/15-6	In Table 15-1, “eTSECn Network Interface Signal Properties,” for RGMII and RTBI protocols, changed description of TSEC*n*_RX_ER from “Unused, output driven low” to “Unused.”
15.4.1/15-9	In Table 15-2, “eTSEC Signals—Detailed Signal Descriptions,” modified TSEC*n*_RX_CLK and TSEC*n*_TX_CLK signal descriptions, removing specific maximum receive clock frequency ratios; referring reader to the device hardware specifications document for specific maximum frequencies.
15.4.1/15-9	In Table 15-2, “eTSEC Signals—Detailed Signal Descriptions,” updated the “State Meaning” description for the TSECn_CRS (formerly referenced TSECn_TX_CLK instead of TSECn_CRS.)
15.5.2/15-14	In Table 15-4, “Module Memory Map,” changed reserved memory map range from “0x2_4034–0x2_404C” to “0x2_4034–0x2_4054.” In addition, updated the access designation for CAR1 and CAR2 registers to be “w1c.” In addition, updated default value of the RQFCR and RQFPR (formerly, “all zeros,” now “undefined.”)
15.5.3.1.3/15-24	In Table 15-7, “EVENT Field Descriptions,” added sub-bullet to third primary bullet in IEVENT register description, defining special function interrupts as MSRO, MMWR, and MMRD. In addition, replaced the second sentence of the CRL field description to say: “The frame is discarded without being transmitted and the queue halts (TSTAT[THLT*n*] set to 1).”
15.5.3.1.6/15-32	In Table 15-10, “ECNTRL Field Descriptions,” made the following changes: • In the RMM field description, replaced “Valid only if FIFM=0 and TBIM=0. RPM and RMM are never set together,”with “RMM must be 0 if RPM = 1.” • In the RMM field description, replaced 0 MII, RGMII, GMII, TBI, or RTBI mode configuration

1 RMII mode
with
0 Non-RMII interface mode
1 RMII interface mode

In addition, added footnote stating that bit TBIM is not supported for parts without TBI support and added footnote stating that bit RMM is not supported for parts without RMII support.

15.5.3.1.6/15-32 In Table 15-11, “eTSEC Interface Configurations”:

- Replaced all “—” with “0” in both “R100M” and “RMM” columns
- Updated ENCTRL[GMIMM] to match settings in Table 15-10, “ECNTRL Field Descriptions”: set for GMII 1 Gbps and cleared for all other values.

15.5.3.1.6/15-33 In Table 15-10, “ECNTRL Field Descriptions,” updated CLRCNT field description to read as follows:

“Clear all statistics counters and carry registers.

0 Allow MIB counters to continue to increment and keep any overflow indicators.

1 Reset all MIB counters and CAR1 and CAR2.

This bit is self-resetting.”

In addition, updated AUTOZ field description to read as follows:

“Automatically zero MIB counter values and carry registers.

0 The user must write the addressed counter zero after a host read.

1 The addressed counter value is automatically cleared to zero after a host read.

This is a steady state signal and must be set prior to enabling the Ethernet controller and must not be changed without proper care.”

15.5.3.1.8/15-36 In Table 15-13, “DMACTRL Field Descriptions,” updated TOD field definition by replacing the “1” state definition with the following:

“1 eTSEC immediately fetches a new TxBD from ring 0.”

15.5.3.2.1/15-38 In Table 15-15, “TCTRL Field Descriptions,” clarified TCTRL[TFC_PAUSE] field description as follows:

“Transmit flow control pause frame. Set this bit to transmit a PAUSE frame. If this bit is set, the MAC stops transmission of data frames after the currently transmitting frame completes. Next, the MAC transmits a pause control frame with the duration value obtained from the PTV register. The TXC event occurs after sending the pause control frame. Finally, the controller clears TFC_PAUSE and resumes transmitting data frames as before. Note that pause control frames can still be transmitted if the Tx controller is stopped due to user assertion of DMACTRL[GTS] or reception of a PAUSE frame.

0 No request for Tx PAUSE frame pending or transmission complete.

1 Software request for Tx PAUSE frame pending.”

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	In addition, changed TXSCHED field description for 01 state to read as follows: “01 Priority scheduling mode. Frames from enabled TxBD rings are serviced in ascending ring index order.”
15.5.3.2.4/15-43	In Table 15-18, “TXIC Field Descriptions,” added footnote to ICCS description stating that the term “system clock” refers to the CCB clock/2.
15.5.3.3.3/15-53	In Table 15-28, “RXIC Field Descriptions” added footnote to ICCS description stating that the term “system clock” refers to the CCB clock/2.
15.5.3.3.5/15-55	In Table 15-30, “RBIFX Field Descriptions,” modified RBIFX[BnCTL]=01 field descriptions to clarify that arbitrary extraction of preamble is not supported in FIFO modes. In addition, changed the definition of the 10 encoding of B*n*CTL as follows: “Byte 0 is located in the received frame at offset B0OFFSET bytes from the byte after the last byte of the layer 2 header, “ and changed the definition of the 11 encoding of B*n*CTL as follows: “Byte 0 is located in the received frame at offset B0OFFSET bytes from the byte after the last byte of the layer 3 header.”
15.5.3.3.5/15-56	In Table 15-30, “RBIFX Field Descriptions,” appended the following sentence to the 01 portion of the field descriptions for RBIFX[B0CTL], RBIFX[B1CTL]. RBIFX[B2CTL] and RBIFX[B3CTL]: “Values of B0OFFSET less than 8 are reserved in FIFO modes.” In addition, added notes stating that the offset cannot exceed the parser depth.
15.5/15-16, 15-57	In Figure 15-28, “Receive Queue Filer Table Control Register,” updated default value of the RQFCR (formerly, “all zeros,” now “undefined.”)
15.5/15-16, 15-58	In Figure 15-29, “Receive Queue Filer Table Property Register,” updated default value of the RQFPR (formerly, “all zeros,” now “undefined”).
15.5.3.5.1/15-67	In Table 15-39, “MACCFG1 Field Descriptions,” added clarification to MACCFG1[Tx Flow] and MACCFG1[Rx Flow] field descriptions: “Must be 0 if MACCFG2[Full Duplex] = 0.” In addition, added the following note to Tx_Flow and Rx_Flown field descriptions: “**Note:** Should not be set when operating in Half-Duplex mode.”
15.5.3.5.2/15-68	In Table 15-40, “MACCFG2 Field Descriptions,” appended the following sentence to the MACCFG2[PreAM RxEN] = 1 field description: “If the preamble is less than 7 bytes, 0’s are prepended to pad it to 7 bytes” as well as the following note: “This bit must be set when in half-duplex mode (MACCFG2[Full Duplex] is cleared).”
15.5.3.5.2/15-70	In Table 15-40, “MACCFG2 Field Descriptions,” updated table in Huge Frame (bit 26) field description, as follows:

Table 15-40. MACCFG2 Field Descriptions

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>26</td><td>Huge Frame</td><td>Huge frame enable. This bit is cleared by default.
0 Limit the length of frames received to less than or equal to the maximum frame length value (MAXFRM[Maximum Frame]) and limit the length of frames transmitted to less than the maximum frame length.
See Section 15.6.7, “Buffer Descriptors,” for further details of buffer descriptor bit updating.
<table>
<tr><th>Frame type</th><th>Frame length</th><th>Packet truncation</th><th>Buffer descriptor updated</th></tr>
<tr><td>Receive or transmit</td><td>> maximum frame length</td><td>yes</td><td>yes</td></tr>
<tr><td>Receive</td><td>= maximum frame length</td><td>no</td><td>no</td></tr>
<tr><td>Transmit</td><td>= maximum frame length</td><td>no</td><td>yes</td></tr>
<tr><td>Receive or transmit</td><td>< maximum frame length</td><td>no</td><td>no</td></tr>
</table>
1 Frames are transmitted and received regardless of their relationship to the maximum frame length. Note that if Huge Frame is cleared, the user must ensure that adequate buffer space is allocated for received frames. See Section 15.5.3.5.5, “Maximum Frame Length Register (MAXFRM),” for further information.</td></tr>
</table>

15.5.3.5.4/15-71 In Figure 15-39, “Half-Duplex Register Definition,” and Table 15-42, “HAFDUP Field Descriptions,” corrected HAFDUP[Collision Window] field size (formerly 22:31, now 26:31).

15.5.3.5.5/15-72 In Table 15-43, “MAXFRM Descriptions,” changed first sentence of field description to read as follows:

“This field is set to 0x0600 (1536 bytes) by default and always must be set to a value greater than or equal to 0x0040 (64 bytes).”

15.5.3.5.5/15-73 In Table 15-43, “MAXFRM Descriptions,” added maximum value limit to Maximum Frame field description by modifying the first sentence to read as follows:

“This field is set to 0x0600 (1536 bytes) by default and always must be set to a value greater than or equal to 0x0040 (64 bytes), but not greater than 0x2580 (9600 bytes).”

15.5.3.5.9/15-74 In Figure 15-44, “MII Mgmt Control Register,” corrected register access to write-only.

15.5.3.6/15-79 Added note stating RMON counters are not able to understand VLAN tagged frames.

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15.5.3.6/15-80 Added the following note to the end of the section, as follows:

NOTE

The transmit and receive frame counters (TR64, TR127, TR 255, TR511, TR1K, TRMAX, adn TRMGV) do not increment for aborted frames (collision retry limit exceeded, late collision, underrun, EBERR, TxFIFO data error, frame truncated due to exceeding MAXFRM, or excessive deferral).

15.5.3.6.25/15-91 In Table 15-79, “TBYT Field Descriptions,” changed second sentence of TBYT field description from

“This count does not include preamble/SFD or jam bytes”

to

“This count does not include preamble/SFD or jam bytes, except for half-duplex flow control (back-pressure triggered by TCTRL[THDF]=1). For THDF, the sum total of ‘phantom’ preamble bytes transmitted for flow control purposes is included in the TBYT increment value of the next frame to be transmitted, up to 65,535 bytes of frame and phantom preamble.”

15.5.3.6.41/15-100 In Table 15-95, “TOVR Field Descriptions,” updated TOVR field description to read as follows:

“Transmit oversize frame counter. Increments each time a frame is transmitted which exceeds 1518 (non VLAN) or 11522 (VLAN) with a correct FCS value.”

15.5.3.6.44/15-102 In Figure 15-95, “Carry Register 1 (CAR1) Register Definition,” updated the access designation for CAR1 to be “w1c.”

15.5.3.6.45/15-104 In Figure 15-96, “Carry Register 2, (CAR1) Register Definition,” updated the access designation for CAR2 to be “w1c.”

15.5.3.8.1/15-108 Modified last sentence of FIFOCFG[IPG] field description in Table 15-105, “FIFOCFG Field Descriptions,” as follows: “The minimum required is 3 cycles if CRCAPP=0 and 7 cycles for 8-bit interfaces if CRCAPP=1.

15.5.3.9.2/15-113 In Table 15-107, “ATTRELI Field Descriptions,” replaced EI field description with the following:

“Extracted index. Points to the first byte, as a multiple of 64 bytes, within the receive frame as sent to memory from which to begin extracting data.”

15.5.3.10.2/15-114 In Figure, “RFBPTR0–RFBPTR7 Register Definition,” updated the register offset designation to read as follows:

“Offset

eTSEC1:0x2_4C44+8×*n*eTSEC3:0x2_6C44+8×*n*”

15.5.4.3.10/15-126 In Table 15-121, “TBICON Field Descriptions,” clarified the asserted state description for the TBICON[Clock Select] field by appending the following to the end of the last sentence of the Clock Select = 1 field description:

“if using a parallel (non-SGMII) Ethernet protocol.”

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15.6.2/15-137	Updated the last bullet item of this section regarding minimum inter-packet gap requirements as follows: "On transmission, the minimum inter-packet gap (set in FIFOCFG[IPG]) is three cycles if CRC is not automatically appended. Each CRC data beat adds to this requirement. For 8-bit FIFO interfaces the minimum is 7 cycles.
15.6.2.1/15-138	Updated second sentence of third paragraph to say the following: "The controller completes any frame in progress before stopping transmission and does not commence counting the pause time until transmit is idle."
15.6.3.10/15-152	Clarified three sub-bullets under first primary bullet, noting that anything other than RXB, RXF, TXB, and TXF is classified as "error, diagnostic, or special interrupts."
15.6.3.11/15-155	Replaced section 15.6.3.11, "Inter-Frame Gap Time," with the following:

15.6.3.11 Inter-Frame Gap Time

If a station must transmit, it waits until the LAN becomes silent for a specified period (inter-frame gap, or IFG). The minimum inter-packet gap (IPG) time for back-to-back transmission is set by IPGIFG[Back-to-Back Inter-Packet-Gap]. The receiver receives back-to-back frames with the minimum interframe gap (IFG) as set in IPGIFG[Minimum IFG Enforcement]. If multiple frames are ready to transmit, the Ethernet controller follows the minimum IPG as long as the following restrictions are met:

- The first TxBD pointer, TBPTR*n*, of any given frame is located at a 16-byte aligned address.
- Each TxBD[Data Length] is greater-than or equal to 64 bytes.

If the first TxBD alignment restriction is not met, the back-to-back IPG may be as many as 32 cycles. If the TxBD size restriction is not met, the back-to-back IPG may be significantly longer.

In half-duplex mode, after a station begins sending, it continually checks for collisions on the LAN. If a collision is detected, the station forces a jam signal (all ones) on its frame and stops transmitting. Collisions usually occur close to the beginning of a packet. The station then waits a random time period (back-off) before attempting to send again. After the back-off completes, the station waits for silence on the LAN (carrier sense negated) and then begins retransmission (retry) on the LAN. Retransmission begins 36 bit times after carrier sense is negated for at least 60 bit times. If the frame is not successfully sent within a specified number of retries, an error is indicated (collision retry limit exceeded).

15.6.3.13/15-156	In Table 15-138, "Reception Errors," removed the following note from the reception errors table entry for parser error: **Note:** Any values in the length/type field between 1500 and 1536 will be treated as a length, however, only illegal packets exist with this length/type since these are not valid lengths and not valid types. These are treated by the MAC logic as out of range. Software must confirm the parser and filer results by checking the type/length field after the packet has been written to memory to see if it falls in this range

15.6.5.1/15-162 Added the following subsection, “Receive Parser,” to Section 15.6, “Quality of Service (QoS) Provision,” as follows:

15.6.5.1 Receive Parser

The receive parser parses the incoming frame data and generates filer properties and frame control block (FCB). The receive parser composes of the Ethernet header parser and L3/L4 parser.

The Ethernet header parser parses only L2 (ethertype) headers. It is enabled by RCTRL[PRSDEP] != 0. It has the following key features:

- Extraction of 48-bit MAC destination and source addresses
- Extraction and recognition of the first 2-byte ethertype field
- Extraction and recognition of the final 2-byte ethertype field
- Extraction of 2-byte VLAN control field
- Walk through MPLS stack and find layer 3 protocol
- Walk through VLAN stack and find layer 3 protocol
- Recognition of the following ethertypes for inner layer parsing
  - LLC and SNAP header
  - JUMBO and SNAP header
  - IPV4
  - IPV6
  - VLAN
  - MPLSU/MPLSM
  - PPPOES

For stack L2 (that is, more than one ethertypes) header, the Ethernet parser traverses through the header until it finds the last valid ethertype or the ethertype is unsupported. Table 15-141 describes what the Ethernet header parser recognizes for stack L2 header.

Table 15-141. Supported Stack L2 Ethernet Headers

Column—Current L2 Ethertype Row—Next Supported L2 Ethertype	LLC/ SNAP	JUMBO/ SNAP	IPV4	IPV6	VLAN	MPLSU	MPLSM	PPOES
LLC/SNAP	N	N	Y	Y	Y	Y	Y	Y
JUMBO/SNAP	N	N	Y	Y	Y	Y	Y	Y
IPV4	N	N	N	N	N	N	N	N
IPV6	N	N	N	N	N	N	N	N
VLAN	Y	Y	Y	Y	Y	Y	Y	Y

Table 15-141. Supported Stack L2 Ethernet Headers (continued)

Column—Current L2 Ethertype Row—Next Supported L2 Ethertype	LLC/ SNAP	JUMBO/ SNAP	IPV4	IPV6	VLAN	MPLSU	MPLSM	PPOES
MPLSU	N	N	Y*	Y*	N	y	Y	N
MPLSM	N	N	Y*	Y*	N	Y	Y	N
PPOES	N	N	Y	Y	N	Y	Y	N
Note: * means that it is the next protocol								

The L3 parser is enabled by RCTRL[PRSDEP] = 10 or 11. It begins when the Ethernet parser ends and a valid IPv4/v6 ethertype is found. The L4 header is enabled by RCTRL[PRSDEP] = 11. It begins when the L3 parser ends and a valid TCP/UDP next protocol is found and no fragment frame is found. The primary functionalities of L3(IPv4/6) and L4(TCP/UDP) parsers are as follows:

- IP recognition (v4/v6, encapsulated protocol)
- IP header checksum verification
- IPv4/6 over IPv4/6 (tunneling)—parse headers and find layer 4 protocol
- IP layer 4 protocol/next header extraction
- Stop parsing on unrecognized next header/protocol
- IPv4 support
  - IPv4 source and destination addresses
  - 8-bit IPv4 type of service
  - IP layer 4 protocol / next header support
    - IPV4
    - IPV4 Fragment. Parser stops after a fragment is found
    - TCP/UDP
- IPv6 support
  - The first 4 bytes of the IPv6 source address extraction
  - The first 4 bytes of the IPv6 destination address extraction
  - IPv6 source address hash for pseudo header calculation
  - IPv6 destination address hash for pseudo header calculation
  - 8-bit IPv6 traffic class field extraction
  - Payload length field extraction
  - IP layer 4 protocol/next header support
    - IPV6
    - IPV6 fragment. Parser stops after a fragment is found
    - IPV6 route
    - IPV6 hop/destination

  - TCP/UDP

- L4 (TCP/UDP) support
  - Extraction of 16-bit source port number extraction
  - Extraction of 16-bit destination port number extraction
  - TCP checksum calculation (including pseudo header)
  - UDP checksum calculation if the checksum field is not zero (including pseudo header)

15.6.5.2.1/15-168 Revised section 15.6.5.2.1, “Priority-Based Queuing (PBQ),” to read as follows:

15.6.5.2.1 Priority-Based Queuing (PBQ)

PBQ is the simplest scheduler decision policy. The enabled TxBD rings are assigned a priority value based on their index. Rings with a lower index have precedence over rings with higher indices, with priority assessed on a frame-by-frame basis. For example, frames in TxBD ring 0 have higher priority than frames in TxBD ring 1, and frames in TxBD ring 1 have higher priority than frames in TxBD ring 2, and so on.

The scheduling decision is then achieved as follows:

```
loop
      # start or S/W clear of TSATn
      ring = 0;
      while ring <= 7 loop
       if enabled(ring) and not ring_empty(ring) then
              transmit_frame(ring);
              ring = 0;
       else
              ring = ring + 1;
       endif
      endloop
endloop
```

15.6.6.2.1, 15-172 Completed last sentence of second paragraph as follows:

“As soon as the hardware consumes a BD (by writing it back to memory), RBPTRn will advance and the free BD count will reflect the correct number of available free BDs.”

15.6.7.3/15-179 In Table 15-147, “Transmit Data Buffer Descriptor (TxBD) Field Descriptions,” updated the data length field description (offset 2–3; bits 0–15). Replaced the following sentence:

“Data length is the number of octets written by the eTSEC into this BD’s data buffer if L is cleared (the value is equal to MRBLR), or, if L is set, the length of the frame including CRC, FCB (if RCTRL[PRSDEP > 00) and any padding (RCTRL[PAL])”

with:

“Data length is the number of octets written by the eTSEC into this BD’s data buffer if L is cleared (the value is equal to MRBLR), or, if L is set, the length of

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	the frame including CRC, FCB (if RCTRL[PRSDEP > 00), preamble (if MACCFG2[PreAmRxEn]=1), and any padding (RCTRL[PAL]).”
16.3.1.1/16-10	In Table 16-5, “MR*n* Field Descriptions,” Appended the following sentence to the MR*n*[CS] field description: “Note that in external control mode, deasserting $\overline{\text{DMA\_DREQ}}$ does NOT clear this bit.”
16.4.1.3/16-30	Appended the following sentence to the third paragraph: “Note that external control cannot cause a channel to enter a paused state.” Appended the following sentence to the $\overline{\text{DMA\_DREQ}}$ bullet of the fifth paragraph: “(Note that negating $\overline{\text{DMA\_DREQ}}$ does NOT clear MR*n*[CS].)”
16.4.1.4/16-31	Appended the following clarifying sentence to second paragraph of this section: “The channel busy (SR*n*[CB]) bit is cleared when the DMA controller reaches EOLND/EOLSD and is set again when it initiates the refetch of the link or list descriptor.”
16.4.2/16-33	Added note that a single DMA transfer in any of the direct or chaining modes must not cross a 16GB (34-bit) address boundary.
16.5/16/16-38	Removed bulleted items because they are also found in Section 16.5.1, “Unusual DMA Scenarios.”
16.4.1.5/16-59	Appended the following clarification to the second paragraph of this section: “The channel busy (SR*n*[CB]) bit is cleared when the DMA controller reaches EOLND/EOLSD and is set again when it initiates the refetch of the link or list descriptor.”
17.3.1/17-17–21	In Section 17.3.1.2, “PCI ATMU Outbound Registers,” and Section 17.3.1.3, “PCI ATMU Inbound Registers,” revised descriptions in translation address (TA) and base address (BA) fields to state that the windows must be aligned to the window size.
18.1.1.1, 18-2	Added the following paragraph at the end of the section: “Note that after reset or when recovering from a link down condition, external transactions should not be attempted until the link has successfully trained. Software can poll the LTSSM state status register (PEX_LTSSM_STAT) to check the status of link training before issuing external requests.”
18.3.2.2/18-10	Added the following sentences at the end of the first paragraph: “Also note that accesses to the little-endian PCI Express configuration space must be properly formatted. See Section 18.4.1.2.1, “Byte Order for Configuration Transactions,” for more information.”
18.3.2.3/18-11	In Table 18-6, “PEX_OTB_CPL_TOR Field Descriptions,” revised description of TC (timeout counter) units for different clock frequencies as follows:

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	Timeout counter. This is the value that is used to load the response counter of the completion timeout. One TC unit is 8× the PCI Express controller clock period; that is, one TC unit is 20 ns at 400 MHz, and 30 ns at 266.66 MHz. The following are examples of timeout periods based on different TC settings: 0x00_0000Reserved 0x10_FFFF22.28 ms at 400 MHz controller clock; 33.34 ms at 266.66 MHz controller clock 0xFF_FFFF335.54 ms at 400 MHz controller clock; 503.31 ms at 266.66 MHz controller clock
18.3.2.4/18-11	In Table 18-7, “PEX_CONF_RTY_TOR Field Descriptions,” clarified description of TC (timeout counter) units for different clock frequencies as follows: Timeout counter. This is the value that is used to load the CRS response counter. One TC unit is 8× the PCI Express controller clock period; that is, one TC unit is 20 ns at 400 MHz and 30 ns at 266.66 MHz. Timeout period based on different TC settings: 0x000_0000Reserved 0x400_FFFF1.34 s at 400 MHz controller clock, 2.02 s at 266.66 MHz controller clock 0xFFF_FFFF5.37 s at 400 MHz controller clock, 8.05 s at 266.66 MHz controller clock
18.3.6.1/18-30	In Table 18-23, “PCI Express Error Detect Register Field Descriptions,” added to PCT bit description a note recommending hot reset after a completion time-out is detected.
18.3.6.5/18-36	Changed the second paragraph from “PEX_ERR_CAP_R0 for the case when the error is caused by an outbound transaction from an internal source (that is, PEX_ERR_CAP_STAT[GSID] ≠ 0h02) is shown in Figure 18-28.” to “PEX_ERR_CAP_R0 for the case when the error is caused by an outbound transaction from an internal source (that is, PEX_ERR_CAP_STAT[GSID] ≠ 0h02) and the error is due to timeout condition or PEX_CONFIG_ADDR/PEX_CONFIG_DATA access, is shown in Figure 18-28.”
18.3.6.6/18-38	In Table 18-29, “PCI Express Error Capture Register 1 Field Descriptions,” changed description for OD0 to the following: “Internal platform transaction information. Reserved for factory debug.”
18.3.6.7/18-40	In Table 18-31, “PCI Express Error Capture Register 2 Field Descriptions,” changed description for OD1 to the following:

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	"Internal platform transaction information. Reserved for factory debug."
18.3.6.8/18-41	In Table 18-33, "PCI Express Error Capture Register 3 Field Descriptions," changed description for OD2 to the following:
	"Internal platform transaction information. Reserved for factory debug."
18.3.7.1/18-42	Added the following sentences at the end of the first paragraph:
	"Also note that accesses to the little-endian PCI Express configuration space must be properly formatted. See Section 18.4.1.2.1, "Byte Order for Configuration Transactions," for more information."
18.3.7.2/18-43	Added statement that the PCI Express Controller Internal CSR registers are not accessible by inbound PCI Express configuration transactions.
18.3.9.11/18-73	In Table 18-84, "PCI Express Link Control Register Field Description," augmented description for RL (bit 5) as follows:
	"Retrain link (Reserved for EP devices). In RC mode, setting this bit initiates link retraining by directing the Physical Layer LTSSM to the Recovery state; reads of this bit always return 0."
18.3.10/18-81	Revised range for internal CSR space in Figure 18-101, "PCI Express Extended Configuration Space," to 0x400–0x6FF.
18.3.10/18-81	Added the following footnote to Figure 18-101, "PCI Express Extended Configuration Space": Note that the PCI Express Controller Internal CSRs are not accessible by inbound PCI Express configuration transactions. Attempts to access these registers returns all 0s.
18.3.10.2/18-82	In Table 18-97, "PCI Express Uncorrectable Error Status Register Field Descriptions," added note to CTO description recommending hot reset after a completion time-out is detected.
18.3.10.5/18-85	In Figure 18-106, "PCI Express Correctable Error Status Register," changed the access from "Read/Write" to "w1c."
18.4.1.7/18-102	Modified the section to say the following:
	"Configuration and I/O writes are serialized by the controller. The logic after issuing a configuration write or IO write will not issue any new transactions until the outstanding configuration or I/O write is finished. This means that an acknowledgement packet from the link partner in the form of a CpL TLP packet must be seen or the transaction has timed out. If the CpL packet contains a CRS status, then the logic will re-issue the configuration write transaction. It will keep retrying the request until either a status other than CRS is returned or the transaction times out. Note that configuration writes originating from the PCI Express configuration access registers (PEX_CONFIG_ADDR/PEX_CONFIG_DATA) are not serialized."

18.4.1.9/18-106 After Section 18.4.1.8.2, “Inbound Messages,” inserted the following Section 18.4.1.10, “Error Handling.”

18.4.1.10 Error Handling

The PCI Express specification classifies errors as correctable and uncorrectable. Correctable errors result in degraded performance, but uncorrectable errors generally result in functional failures. As shown in Figure 18-176, uncorrectable errors can further be classified as fatal or non-fatal.

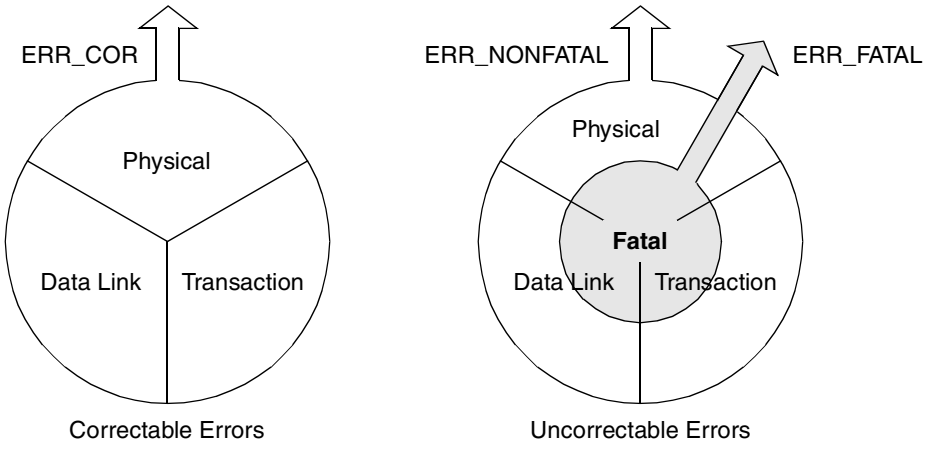

Figure 18-176. PCI Express Error Classification

18.4.1.10.1 PCI Express Error Logging and Signaling

Figure 18-177 shows the PCI Express-defined sequence of operations related to signaling and logging of errors detected by a device. Note that the PCI Express controller on this device supports the advanced error handling capabilities shown within the dotted lines.

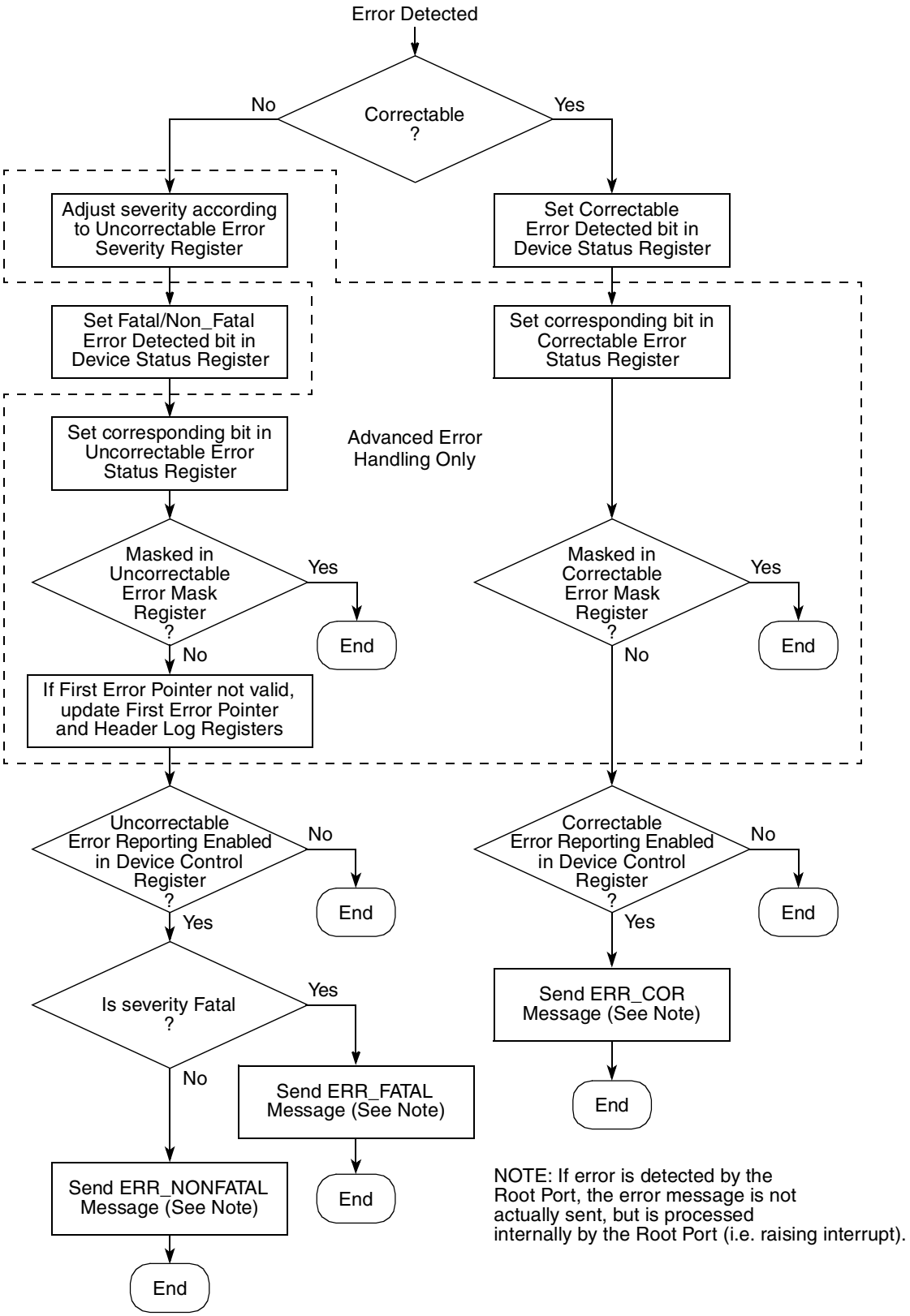

Figure 18-177. PCI Express Device Error Signaling Flowchart

18.4.1.10.2 PCI Express Controller Internal Interrupt Sources

Table 18-163 describes the sources of the PCI Express controller internal interrupt to the PIC and the preconditions for signaling the interrupt.

Table 18-163. PCI Express Internal Controller Interrupt Sources

Status Register Bit	Preconditions
Any bit in PEX_PME_MES_DR set	The corresponding interrupt enable bits must be set in PEX_PME_MES_IER
Any bit in PEX_ERR_DR set	The corresponding interrupt enable bits must be set in PEX_ERR_EN.
PCI Express Root Status Register[16] (PME status) is set	PCI Express Root Control Register [3] (PME interrupt enable) is set
PCI Express Root Error Status Register[6] (fatal error messages received) is set	PCI Express Root Error Command Register [2] (fatal error reporting enable) is set or PCI Express Root Control Register [2] (system error on fatal error enable) is set
PCI Express Root Error Status Register [5] (non-fatal error messages received) is set	PCI Express Root Error Command Register [1] (non-fatal error reporting enable) is set or PCI Express Root Control Register [1] (system error on non-fatal error enable) is set
PCI Express Root Error Status Register[0] (correctable error messages received) is set	PCI Express Root Error Command Register[0] (correctable error reporting enable) is set or PCI Express Root Control Register[0] (system error on correctable error enable) is set.
Any correctable error status bit in PCI Express Correctable Error Status Register is set	The corresponding error mask bit in PCI Express Correctable Error Mask Register is clear and PCI Express Root Error Command Register[0] (correctable error reporting enable) is set
Any fatal uncorrectable error status bit in PCI Express Uncorrectable Error Status Register is set. (The corresponding error is classified as fatal based on the severity setting in PCI Express Uncorrectable Error Severity Register.)	The corresponding error mask bit in PCI Express Uncorrectable Error Mask Register is clear and either PCI Express Device Control Register[2] (fatal error reporting) is set or PCI Express Command Register[8] (SERR) is set.
Any non-fatal uncorrectable error status bit in PCI Express Uncorrectable Error Status Register is set. (The corresponding error is classified as non-fatal based on the severity setting in PCI Express Uncorrectable Error Severity Register.)	The corresponding error mask bit in PCI Express Uncorrectable Error Mask Register is clear and either PCI Express Device Control Register[1] (non-fatal error reporting) is set or PCI Express Command Register[8] (SERR) is set.
PCI Express Secondary Status Register[8] (master data parity error) is set.	PCI Express Secondary Status Interrupt Mask Register[0] (mask master data parity error) is cleared and PCI Express Command Register[6] (parity error response) is set.
PCI Express Secondary Status Register[11] (signaled target abort) is set	PCI Express Secondary Status Interrupt Mask Register[1] (mask signaled target abort) is cleared.
PCI Express Secondary Status Register[12] (received target abort) is set	PCI Express Secondary Status Interrupt Mask Register[2] (mask received target abort) is cleared.

Table 18-163. PCI Express Internal Controller Interrupt Sources (continued)

Status Register Bit	Preconditions
PCI Express Secondary Status Register[13] (received master abort) is set	PCI Express Secondary Status Interrupt Mask Register[3] (mask received master abort) is cleared.
PCI Express Secondary Status Register[14] (signaled system error) is set.	PCI Express Secondary Status Interrupt Mask Register[4] (mask signaled system error) is cleared.
PCI Express Secondary Status Register[15] (detected parity error) is set	PCI Express Secondary Status Interrupt Mask Register[5] (mask detected parity error) is cleared.
PCI Express Slot Status Register[0] (attention button pressed) is set	PCI Express Slot Control Register[0] (attention button pressed enable) is set and PCI Express Slot Control Register[5] (hot plug interrupt enable) is set and either PCI Express PM Control Register[1–0] = 00 (the function power state is D0) or PCI Express PM Control Register[8] (PME enable) is set.
PCI Express Slot Status Register[1] (power fault detected) is set	PCI Express Slot Control Register[1] (power fault detected enable) is set and PCI Express Slot Control Register[5] (hot plug interrupt enable) is set and either PCI Express PM Control Register[1–0] = 00 (the function power state is D0) or PCI Express PM Control Register[8] (PME enable) is set.
PCI Express Slot Status Register[2] (MRL sensor changed) is set	PCI Express Slot Control Register[2] (MRL sensor changed enable) is set and PCI Express Slot Control Register[5] (hot plug interrupt enable) is set and either PCI Express PM Control Register[1–0] = 00 (the function power state is D0) or PCI Express PM Control Register[8] (PME enable) is set.
PCI Express Slot Status Register[3] (presence detect changed) is set	PCI Express Slot Control Register[3] (presence detect changed enable) is set and PCI Express Slot Control Register[5] (hot plug interrupt enable) is set and either PCI Express PM Control Register[1–0] = 00 (the function power state is D0) or PCI Express PM Control Register[8] (PME enable) is set.
PCI Express Slot Status Register[4] (command completed) is set	PCI Express Slot Control Register[4] (command completed interrupt enable) is set and PCI Express Slot Control Register[5] (hot plug interrupt enable) is set.

18.4.1.10.3 Error Conditions

Table 18-164 describes specific error types and the action taken for various transaction types.

Table 18-164. Error Conditions

Transaction Type	Error Type	Action
Inbound response	PEX response time out. This case happens when the internal platform sends a non-posted request that did not get a response back after a specific amount of time specified in the outbound completion timeout register (PEX_OTB_CPL_TOR)	Log error (PEX_ERR_DR[PCT]) and send interrupt to PIC, if enabled.
Inbound response	Unexpected PEX response. This can happen if, after the response times out and the internal queue entry is deallocated, the response comes back.	Log unexpected completion error (PCI Express Uncorrectable Status Register[16]) and send interrupt to PIC, if enabled.
Inbound response	Unsupported request (UR) response status	Depending upon whether the initial internal request was broken up, the error is not sent until all responses come back for all portions of the internal request. Log the error (PEX_ERR_DR[CDNSC] and PCI Express Uncorrectable Status Register[20]) and send interrupt to PIC, if enabled.
Inbound response	Completer abort (CA) response status	Depending upon whether the initial internal request was broken up, the error is not sent until all responses come back for all portions of the internal request. Log the error (PEX_ERR_DR[PCAC, CDNSC] and PCI Express Uncorrectable Status Register[15] and send interrupt to PIC, if enabled.
Inbound response	Poisoned TLP (EP=1)	Depending upon whether the initial internal request was broken up, the error is not sent until all responses come back for all portions of the internal request. Log the error (PCI Express Uncorrectable Status Register[12]) and send interrupt to PIC, if enabled.
Inbound response	ECRC error	Depending upon whether the initial internal request was broken up, the error is not sent until all responses come back for all portions of the internal request. Log the error (PCI Express Uncorrectable Status Register[19]) and send interrupt to PIC, if enabled.
Inbound response	Configuration Request Retry Status (CRS) timeout for a configuration transaction that originates from PEX_CONFIG_ADDR/ PEX_CONFIG_DATA	1.The controller always retries the transaction as soon as possible until a status other than CRS is returned. However, if a CRS status is returned after the configuration retry timeout (PEXCONF_RTY_TOR) timer expires, then the controller aborts the transaction and sends all 1s (0xFFFF_FFFF) data back to requester. 2. Log the error (PEX_ERR_DR[PCT]) and send interrupt to the PIC, if enabled.
Inbound response	UR response for configuration transaction that originates from PEX_CONFIG_ADDR/ PEX_CONFIG_DATA	1. Send back all 1s (0xFFFF_FFFF) data. 2. Log the error (PEX_ERR_DR[CDNSC] and PCI Express Uncorrectable Status Register[20]) and send interrupt to PIC, if enabled.

Table 18-164. Error Conditions (continued)

Transaction Type	Error Type	Action
Inbound response	CA response for Configuration transaction that originates from PEX_CONFIG_ADDR/ PEX_CONFIG_DATA	1. Send back all 1s (0xFFFF_FFFF) data. 2. Log the error (PEX_ERR_DR[PCAC, CDNSC] and PCI Express Uncorrectable Status Register[15]) and send interrupt to PIC, if enabled.
Inbound response	Poisoned TLP (EP=1) response for Configuration transaction that originates from PEX_CONFIG_ADDR/ PEX_CONFIG_DATA	1. Send back all 1s (0xFFFF_FFFF) data. 2. Log the error (PCI Express Uncorrectable Status Register[12]) and send interrupt to PIC, if enabled.
Inbound response	ECRC error response for Configuration transaction that originates from PEX_CONFIG_ADDR/ PEX_CONFIG_DATA	1. Send back all 1s (0xFFFF_FFFF) data. 2. Log the error (PCI Express Uncorrectable Status Register[19]) and send interrupt to PIC, if enabled.
Inbound response	Configuration Request Retry Status (CRS) response for Configuration transaction that originates from ATMU	1.The controller always retries the transaction as soon as possible until a status other than CRS is returned. However, if a CRS status is returned after the configuration retry timeout (PEXCONF_RTY_TOR) timer expires, then the controller aborts the transaction. 2. Log the error (PEX_ERR_DR[CRST]) and send interrupt to the PIC, if enabled.
Inbound response	UR response for Configuration transaction that originates from ATMU	Log the error (PEX_ERR_DR[CDNSC] and PCI Express Uncorrectable Status Register[20]) and send interrupt to PIC, if enabled.
Inbound response	CA response for Configuration transaction that originates from ATMU	Log the error (PEX_ERR_DR[PCAC, CDNSC] and PCI Express Uncorrectable Status Register[15]) and send interrupt to PIC, if enabled.
Inbound response	Malformed TLP response	PCI Express controller does not pass the response back to the core. Therefore, a completion timeout error eventually occurs.
Inbound request	Poisoned TLP (EP=1)	1. If it is a posted transaction, the controller drops it. 2. If it is a non-posted transaction, the controller returns a completion with UR status. 3. Release the proper credits
Inbound request	ECRC error	1. If it is a posted transaction, the controller drops it. 2. If it is a non-posted transaction, the controller returns a completion with UR status. 3. Release the proper credits
Inbound request	PCI Express nullified request	The packet is dropped.
Outbound request	Outbound ATMU crossing	Log the error (PEX_ERR_DR[OAC]). The transaction is not sent out on the link.
Outbound request	Illegal message size	Log the error (PEX_ERR_DR[MIS]). The transaction is not sent out on the link.
Outbound request	Illegal I/O size	Log the error (PEX_ERR_DR[IOIS]). The transaction is not sent out on the link.
Outbound request	Illegal I/O address	Log the error (PEX_ERR_DR[IOIA]). The transaction is not sent out on the link.

Table 18-164. Error Conditions (continued)

Transaction Type	Error Type	Action
Outbound request	Illegal configuration size	Log the error (PEX_ERR_DR[CIS]). The transaction is not sent out on the link.
Outbound response	Internal platform response with error (for example, an ECC error on a DDR read or the transaction maps to unknown address space).	Send poisoned TLP (EP=1) completion(s) for data that are known bad. If the poison data happens in the middle of the packet, the rest of the response packet(s) is also poisoned.

18.4.5/18-109 Added the following section after Section 18.4.5, “Hot Reset”:

18.4.6 Link Down

Typically, a link down condition occurs after a hot reset event; however, it is possible for the link to go down unexpectedly without a hot reset event. When this occurs, a link down condition is detected (PEX_PME_MSG_DR[LDD]=1). Link down is treated similarly to a hot reset condition.

Subsequently, while the link is down, all new posted outbound transactions are discarded. All new non-posted ATMU transactions are errored out. Non-posted configuration transactions issued using PEX_CONFIG_ADDR/PEX_CONFIG_DATA toward the link returns 0xFFFF_FFFF (all 1s). As soon as the link is up again, the sending of transaction resumes.

Note that in EP mode, a link down condition causes the controller to reset all non-sticky bits in its PCI Express configuration registers as if it had been hot reset.

19.4.1.6/19-10 In Figure 19-6, “POR Device Status Register 2 (PORDEVSR2),” changed reset values for bits 24-27 from n101 to n111.

19.4.1.6/19-10 Changed bit position of SEC_CFG from 26 to 24.

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19.4.1.12, 19-14 — Added fields SRDS2 and SRDS1 (bits 28 and 31) to Figure 19-12, “Device Disable Register (DEVDISR)” and Table 9-15, “DEVDISR Field Descriptions.” The register figure and field description table changes should appear as follows:

Offset 0xE_0070 Access: Read/Write

	0	1	2	3	4	5	6	7	8						14	15
R W	PCI	—	PCIE1	—	LBC	PCIE2	PCIE3	SEC	—							DDR
Reset	0	0	*n*[1]	0	0	*n*	*n*	0	0	0	0	0	0	0	0	0

	16	17	18	20	21	22	23	24	25	26	27	28	29	30	31
R W	E500	TB	—		DMA	—		TSEC1	—	TSEC3	—	SRDS2	I2C	DUART	SRDS1
Reset	All zeros														

Figure 19-12. Device Disable Register (DEVDISR)

1 * *n* bits depend on the state of the corresponding POR configuration signals at reset.

Table 19-15. DEVDISR Field Descriptions

Bits	Name	Description
28	SRDS2	SerDes 2 disabled 0 SerDes 2 enabled 1 SerDes 2 disabled
31	SRDS1	SerDes 1 disabled 0 SerDes 1 enabled 1 SerDes 1 disabled

19.4.1.23/19-23 — In Table 19-26, “CLKOCR Field Descriptions,” removed Logic 0 and Logic 1 configuration options from CLKOCR[CLK_SEL] field description.

20.4.7/20-16 — In Table 20-10, “Performance Monitor Events,” clarified that PCI performance monitor event counts are only accurate when the PCI controller is configured in synchronous operation.

Appendix B, B-13 — In Table B-1, “Memory Map,” changed the offsets for L2ERRADDRH and L2ERRADDRL to read as follows:

Table B-1. Memory Map

Offset	Register	Access	Reset	Section/Page
0x2_0E50	L2ERRADDRL—L2 error address capture register low	R	0x0000_0000	7.3.1.8.2/7-51
0x2_0E54	L2ERRADDRH—L2 error address capture register high	R	0x0000_0000	7.3.1.8.2/7-51

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