

# Errata to the MPC855T User's Manual, Rev. 1

This errata document describes corrections to the *MPC855T User's Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided. Items with section and page numbers in bold are new since the last revision of this document.

To locate any published updates for this document, refer to the world-wide web located on the last page of this document.

<b>Section/Page</b>	<b>Changes</b>
12, 12-3	On the top right side of Figure 12-2, replace 'F4-VDDH' with 'F4-VDDL.' Remove 'T14' from the list.
12.5, 12-28	In the second row of Table 12-5, add a footnote at end of sentence that states: At power-on reset, port pin states are not defined in any particular state until CLKOUT is present for two clocks.
<b>15.6.4.7, 15-49</b>	In Table 15-19, "AMA/AMB Definition for DRAM Interface)," add a footnote to "Memory Size" that states the following: "Memory Size takes data bus width into account."
21.2.1, 21-9	In the MODE field (bits 28–31) of Table 21-2, V.14 RAM microcode is not supported. Thereby, mode 0111 should be 'Reserved.'
21.2.1, 21-9	In the MODE field (bits 28–31) of Table 21-2, DDCMP RAM microcode is not supported. Thereby, mode 1001 should be 'Reserved.'
<b>21.2.4, 21-10</b>	In Table 21-3, "TODR Field Descriptions," in TOD field description, change "TOD is cleared automatically after one serial clock..." to say "TOD is cleared automatically after 1 system clock..."

Section, Page No.	Changes
<b>21.2.4, 21-10–21-11</b>	In Figure 21-5, change the TODR register access from R/W to W (write only). Also, in Table 21-3, revise the second sentence of bit setting 1 in the TODR[TOD] description to read “TOD is cleared automatically after one system clock cycle, but...”
<b>21.3, 21-12</b>	Under third bullet point, change “For an RxBD, the value must be even,” to say, “For an RxBD, the value must be mod 4 aligned.”
<b>22, 22-1</b>	The last sentence in the last paragraph should be removed.
<b>22.16, 22-14</b>	In the RZS field (bit 7) of Table 22-9, for selection 1, the second sentence in the paragraph (making reference to V.14 applications) should be removed.
27.8, 27-13	Add superscript number 2 after PADDR1_H, PADDR1_M, and PADDR1_L.
27.8, 27-14	Add superscript number 2 after TADDR_H, TADDR_M and TADDR_L. Add a note 2 at the bottom of Table 27-1 with the statement:  The address should be written in little endian, not Motorola’s big-endian format (that is, physical address 112233445566 should be written PADDR_L = 6655, PADDR_M = 4433, and PADDR_H = 2211. The TADDR should be written in the same way as the PADDR).
27.22, 27-28	Change the last sentence in step 26 to read, “Then write 0x000E to TxBD[Data... .”
<b>30.4.1.2, 30-9</b>	In the last sentence of example 1, change the order of the string for REV = 1 to the following:  first            j_klmn__r_stuv    last
30.4.1.2, 30-10	In the last sentence of example 3, change the order of the string for REV = 1 to the following:  first            r_stuv_ghij_klmn    last
31.4.3, 31-8	Table 31-3, replace the text in the description with the following:  Division ratio 0–7. Specifies the divide ratio of the BRG divider in the I <sup>2</sup> C clock generator. The output of the prescaler is divided by $2 \times (DIV + 3 + (2 \times FLT))$ , and the clock has a 50% duty cycle. The FLT bit is in the I2MOD register. The minimum value for DIV is 3 if the digital filter is disabled (FLT = 0) and 6 if the digital filter is enabled (FLT = 1).
33.1, 33-2	Add a footnote reference number at the end of the statement of the sixth bullet with the following footnote:  At power-on reset, port pin states are not defined in any particular state until CLKOUT is present for two clocks.
43.2.12, 43-10	Change the term ‘60x’ in the first and fourth sentences to ‘external.’
<b>B.3.1, B-4</b>	In Table B-1, the row making reference to SCC in Profibus should be removed.

## How to Reach Us:

### Home Page:

[www.freescale.com](http://www.freescale.com)

### Web Support:

<http://www.freescale.com/support>

### USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
1-800-521-6274 or  
+1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### Japan:

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku  
Tokyo 153-0064  
Japan  
0120 191014 or  
+81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### Asia/Pacific:

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### For Literature Requests Only:

Freescale Semiconductor  
Literature Distribution Center  
1-800 441-2447 or  
+1-303-675-2140  
Fax: +1-303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale, the Freescale logo, and PowerQUICC, are trademarks of Freescale Semiconductor, Inc. Reg. U.S. Pat. & Tm. Off. . All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2010 Freescale Semiconductor, Inc.

Document Number: MPC855TUMAD

Rev. 1.2

06/2010

