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Errata to MPC8572E PowerQUICC™ III Integrated Processor Reference Manual, Rev. 2

This document describes substantive changes to the *MPC8572E PowerQUICC™ III Integrated Host Processor Reference Manual*, revision 2. For convenience, the chapter number and section number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page	Changes
2.4, 2-66	In Table 2-11, “Memory Map,” change reset value for PORDEVSR2 to “see ref.”
3.1, 3-4	Change “TSEC_1588_CLK_IN” to “TSEC_1588_CLK” in Figure 3-2, “MPC8572E Signal Groupings (2/3) (Continued).”
4.3.1.1.2, 4-6	In Table 4-5, “CCSRBAR Bit Settings” add clarification for BASE_ADDR (bits 8–23) field description from: “Identifies the16 most-significant address bits of the window,” to: “Identifies the16 most-significant address bits of the 36-bit window.”
4.4.3.1, 4-13	Remove sentence, “There is no default value for this PLL ratio; these signals must be pulled to the desired values.”
4.4.3.1, 4-13	In Table 4-9, “CCB Clock PLL Ratio,” replace “no default” in Functional Signals column with “default (111).”
4.4.3.2, 4-13	Remove sentence, “There is no default value for this PLL ratio; these signals must be pulled to the desired values.”

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4.4.3.3, 4-14	In Table 4-11, “e500 Core0 Clock PLL Ratios,” and Table 4-12, “e500 Core1 Clock PLL Ratios,” change “010” to “Reserved.”
4.4.3.2, 4-14	In Table 4-10, “DDR Complex Clock PLL Ratio,” replace “no default” in Functional Signals column with “default (111).”
4.4.3.3, 4-14	In Table 4-11, “e500 Core0 Clock Pll Ratios,” and Table 4-12, “e500 Core1 Clock PLL Ratios,” replace “no default” in Functional Signals column with “default (111).”
4.4.3.3, 4-14	Remove sentence, “There is no default value for this PLL ratio; these signals must be pulled to the desired values.”
4.4.4.3.1, 4-32	Add the following sentence to the first paragraph and remove the remainder of the section: “Please refer to the *MPC8572E Integrated Processor Hardware Specifications*, for specific supported frequencies.”
6.10.2, 6-25	In Figure 6-33, “Hardware Implementation-Dependent Register 1 (HID1),” update Access from “Supervisor read/write” to “Supervisor Mixed.”
7.3.1.1, 7-9	In Figure 7-7, “L2 Control Register (L2CTL),” update Access from “Read/Write” to “Mixed.”
9.3.2.1, 9-8	In Table 9-3, “Memory Interface Signals—Detailed Signal Descriptions,” change signal description of MA[15:0] from: “Assertion/Negation—The address is always driven when the memory controller is enabled. It is valid when a transaction is driven to DRAM (when $\overline{\text{MCS}}n$ is active).” to: “Assertion/Negation—The address lines are only driven when the controller has a command scheduled to issue on the address/CMD bus; otherwise they will be at high-Z. It is valid when a transaction is driven to DRAM (when $\overline{\text{MCS}}n$ is active).”
9.4.1.5, 9-20	In Table 9-10, “TIMING_CFG_0 Field Descriptions,” add the following statement to ODT_PD_EXIT] (bits 20–23) field description: “ODT_PD_EXIT must be greater than TIMING_CFG_5[RODT_ON] when using RODT_ON overrides and must be greater than TIMING_CFG_5[WODT_ON] when using WODT_ON overrides.”
9.4.1.9, 9-29	In Table 9-14, “DDR_SDRAM_CFG_2 Field Descriptions,” update DDR_SDRAM_CFG_2[DQS_CFG] field description to designate a value of 0x0 as reserved. (Note that since the default value for this field is reserved, software must configure this field to a valid value during initialization.)
9.4.1.21, 9-42	In Table 9-27, “DDR_WRLVL_CNTL Field Descriptions,” remove the statement “In addition, write leveling is not supported for DDR3 mirrored DIMMs” from description of DDR_WRLVL_CNTL[WRLVL_EN].
9.4.1.24, 9-46	Change the third paragraph to the following: “Hardware DDR driver calibration is enabled by setting DDRCDR_1[DHC_EN].

NOTE

All driver calibration, whether by software or hardware, should be done before the DDR controller is enabled (before DDR_SDRAM_CFG[MEM_EN] is set)."

9.4.1.24/25, 9-48 In Table 9-30, "DDRCDR_1 Field Descriptions," and Table 9-31, "DDRCDR_2 Field Descriptions," update ODT (bits 12–13) field description as follows:

Bits	Name	Description
12–13	ODT	ODT termination value for IOs. This field is combined with DDRCDR_2[ODT] to determine the termination value. Below is the termination based on concatenating these two fields. 000 75 Ω 001 55 Ω 010 60 Ω 011 50 Ω 100 150 Ω 101 43 Ω 110 120 Ω 111 Reserved Note that the order of concatenation is (from left to right) DDRCDR_1[ODT], DDRCDR_2[ODT]

9.5, 9-60 Remove final sentence of first paragraph of section, which reads "However, write leveling is not supported if these DIMMs are used."

9.6.2, 9-83 Add the following parenthetical to the second sentence of the first paragraph of this section: "Note that 200 ms (500 ms for DDR3) must elapse after DRAM clocks are stable..."

9.5.11, 9-83 Add the following text as an introductory paragraph to Table 9-61: "DDR SDRAM ECC Syndrome Encoding, "In 32-bit mode, Table 9-61 is split into 2 halves. The first half, consisting of rows 0–31, is used to calculate the ECC bits for the first 32 data bits of any 64-bit granule of data. This always applies to the odd data beats on the DDR data bus. The second half of the table, consisting of rows 32–63, is used to calculate the ECC bits for the second 32 bits of any 64-bit granule of data. This always applies to the even data beats on the DDR data bus."

9.6.1, 9-88 In Table 9-65, "Programming Differences Between Memory Types," update DDR2 in the DQS_CFG configuration row from "Can be set to either 00 or 01, depending on if differential strobes are used" to "Should be set to 01."

Chapter 10 Remove all references to "RCWL" and "RCWH."
Change "Message Shared," to "Message Signaled."

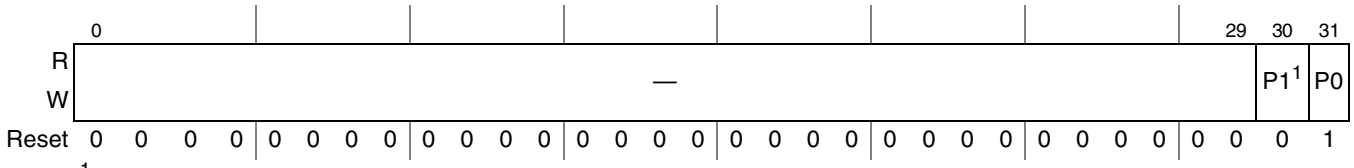
10.3.1, 10-20 Update the Access from "Read/Write" to "Mixed" in the following register figures:

- Figure 10-9, "Interprocessor Interrupt Vector/Priority Register (IPIVPRn)."
- Figure 10-11, "Global Timer Vector/Priority Register (GTVPRxn)."
- Figure 10-34, "Shared Message Signaled Interrupt Vector/Priority Register (MSIVPRs)."

- Figure 10-38, “External Interrupt Vector/Priority Registers (EIVPR0–EIVPR11).”
- Figure 10-40, “Internal Interrupt Vector/Priority Registers (IIVPRs).”
- Figure 10-42, “Messaging Interrupt Vector/Priority Registers (MIVPRn).

10.3.7.6, 10-48 In Figure 10-43, “Messaging Interrupt Destination Registers (MIDR*n*),” and Table 10-43, “MIDR*n* Field Descriptions,” make bits EP, Cl0 and Cl1 reserved, as follows:

Offset MIDR0: 0x1610; MIDR1: 0x1630; MIDR2: 0x1650; MIDR3: 0x1670
MIDR0: 0x1690; MIDR1: 0x16B0; MIDR2: 0x16D0; MIDR3: 0x16F0 Access: Read/Write



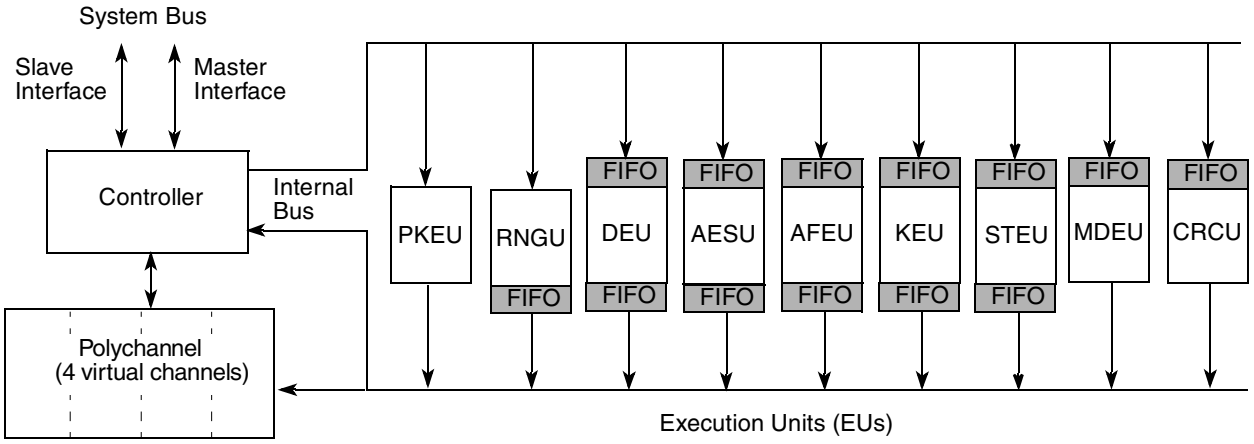
[1] Reserved in single-processor implementations.

Figure 10-43. Messaging Interrupt Destination Registers (MIDR*n*)

Table 10-43. MIDR*n* Field Descriptions

Bits	Name	Description
0–29	—	Reserved, should be cleared.
30	P1	Processor core 1. Indicates whether processor core 1 receives the interrupt through *int.* 0 Processor core 1 does not receive this interrupt. 1 Directs the interrupt to processor core 1 through the assertion of *int1*. **Note:** Reserved in single-processor implementations.
31	P0	Processor core 0. Indicates whether processor core 0 receives the interrupt. 0 Processor core 0 does not receive this interrupt. 1 Directs the interrupt to processor core 0 through the assertion of *int0*. The default destination is for processor core 0 to receive this external interrupt after the PIC is reset.

11.1, 11-4 Replace Figure 11-2, “SEC Functional Modules,” with the following updated figure:



11.4, 11-32 In Figure 11-10, “Descriptor Format Summary,” use the following updated rows for AES-XCBC, AE-CMAC, and KEU f9.

0001_0 common_ no snoop for AES-XCBC, AES-CMAC	Length	reserved	Context In	Key	Main Data In	reserved	Context Out	ICV Out
	Extent	reserved	reserved	reserved	reserved	ICV In	reserved	reserved
0001_0 common_ no snoop for KEU f9	Length	reserved	Context In	Key	Main Data In	reserved	Context Out	ICV Out
	Extent	reserved	reserved	reserved	reserved	reserved	reserved	reserved

11.6.3.1, 11-52 Replace Figure 11-18, “EU Assignment Status Register (EUASR)” with the following:

Offset 0x3_1028 Access: Read only

	0–3	4–7	8–11	12–15	16–19	20–23	24–27	28–31
R	—	AFEU	—	MDEU	—	AESU	—	DEU
W								
Reset	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0

	32–47	48–51	52–55	56–59	60–63
R	—	CRCU	—	PKEU	—	RNG
W						
Reset	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0

Figure 11-18. EU Assignment Status Register (EUASR)

11.6.3.4, 11-58 Add the following paragraph to the Note:

“For this reason, the ICR is ineffective in clearing the RNG Done bit (bit 47) in the ISR. The user should use the IER to mask the RNG Done interrupt. To

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	determine whether a descriptor-based RNG request is complete, the user should rely on Channel Done interrupts.”
11.7.1.1, 11-64	In Table 11-22, “AESU Mode Register Field Descriptions,” update bit 59 field description to use context registers 5–6 in CMAC Cipher Mode description instead of context registers 3–4.
11.7.1.11, 11-75	Add sentence “Context register assignments for cipher modes for confidentiality, data integrity, and combined confidentiality and integrity are described in the following subsections” to the end of section.
11.7.1.11.1, 11-76	Modify the bulleted list to say the following: • Context register 1 holds the most significant bytes of the initialization vector (bytes 1–8). • Context register 2 holds the least significant bytes of the initialization vector (bytes 9–16).
11.7.1.11.1, 11-76	Add section “Context for Confidentiality Cipher Modes,” reading as follows: “The context registers for the different cipher modes which provide confidentiality only are summarized in Table 11-29. The registers are described in more detail in the following subsections.”
11.7.1.11.1, 11-76	Add “Context for ECB Mode ECB does not use any context registers” before “Context for CBC, CBC-RBP, OFP, and CFB128 Cipher Modes.” Remove numbering to make old 11.7.1.11.1–11.7.1.11.3 subsections.
11.7.1.11.6, 11-80	Add the following note:

NOTE

AES-CCM mode does not support zero-length AAD and zero-length payload simultaneously. Either the AAD length or the payload length must be at least 1 byte.

11.7.1.11.7, 11-83 — Replace shaded heading cells in Table 11-33, “GCM Encryption Context,” with the following:

Context Register	GCM Encrypt (Outbound)				
	Mode Register (ECM = 10, AUX0 = 0, CM = 01, ED = 1)				
	AUX1 Value			AUX2 Value	
	Inputs			Outputs	
	AUX1 = 0	AUX1 = 1		AUX2 = 0	AUX2 = 1
		last AAD or text data segment, or MAC only	last IV segment		

11.7.1.11.7, 11-84 Replace shaded heading cells in Table 11-34, “GCM Decryption Context,” with the following:

Context Register	GCM Decrypt (Inbound)				
	Mode Register (ECM = 10, AUX0 = 0 or 1, CM = 01, ED = 0)				
	AUX1 Value			AUX2 Value	
	Inputs			Outputs	
	AUX1 = 0	AUX1 = 1		AUX2 = 0	AUX2 = 1
		last AAD or text data segment, or MAC only	last IV segment		

11.7.1.11.7, 11-85 Replace shaded heading cells in Table 11-35, “GCM w/ICV Context” with the following:

Context Register	GCM with ICV (Inbound)				
	Mode Register (ECM = 11, AUX0 = 0 or 1, CM = 01, ED = 0)				
	AUX1 Value			AUX2 Value	
	Inputs			Outputs	
	AUX1 = 0	AUX1 = 1		AUX2 = 0	AUX2 = 1
		last AAD or text data segment, or MAC only	last IV segment		

11.7.1.11.7, 11-86 Replace shaded heading cells in Table 11-36, “GCM-GHASH Context” with the following:

Context Register	GCM-GHASH (Only GHASH Computed)				
	Mode Register (ECM = 10, AUX0 = 10, CM = 01, ED = 1)				
	AUX1 Value			AUX2 Value	
	Inputs			Outputs	
	AUX1 = 0	AUX1 = 1		AUX2 = 0	AUX2 = 1
		last AAD or text data segment, or MAC only	last IV segment		

11.7.1.11.8, 11-92 Update second sentence of paragraph to read: “Any key data written to bytes beyond the key size (as specified in the key size register) is ignored.”

11.7.1.11.8, 11-92 Add the following figure:

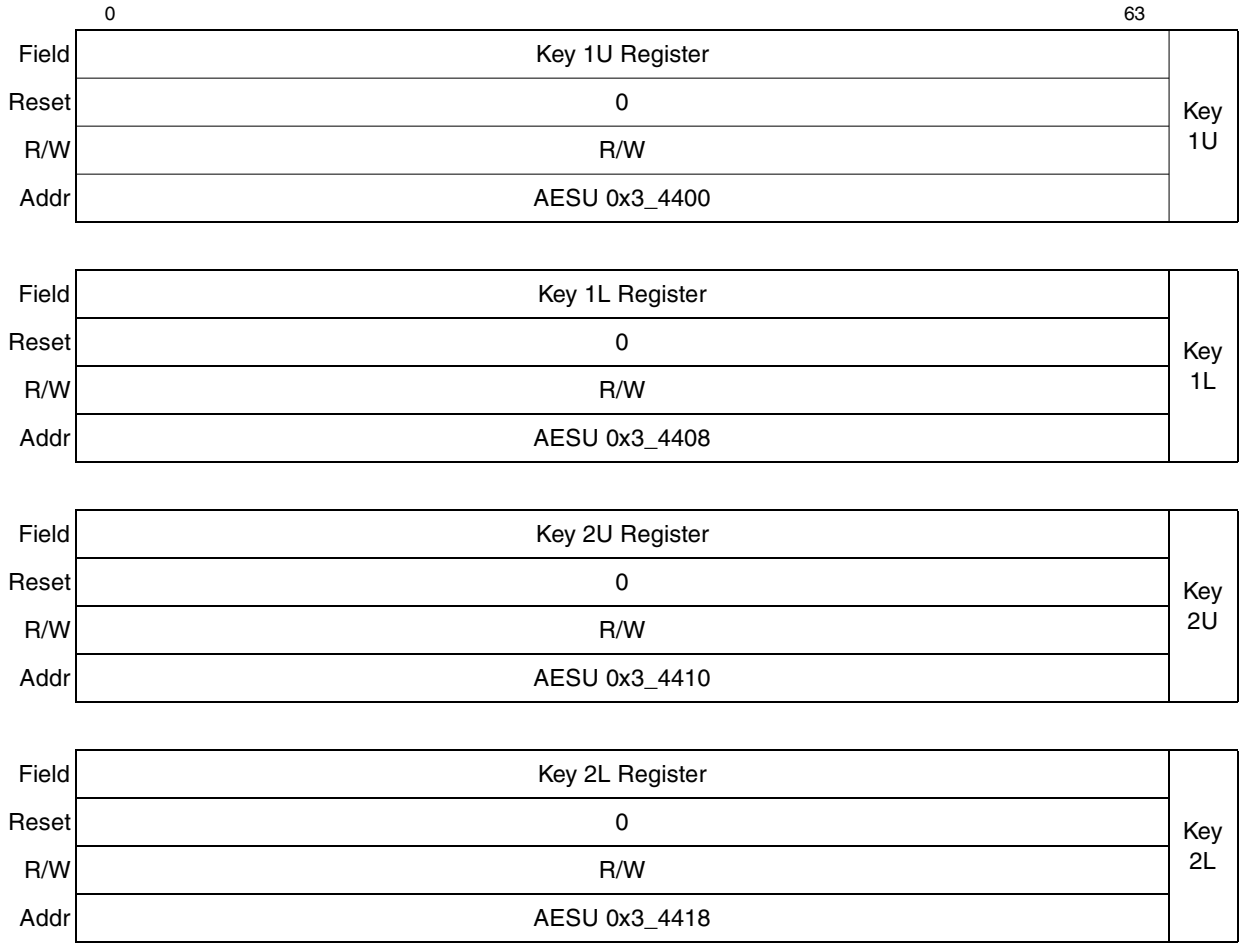

Figure 11-19. AESU Key Registers

11.7.3.6, 11-105 Update bit numbering of Figure 11-47, “CRCU Control Register,” so that the first row reads 0–31 instead of 32–63.

11.7.3.12, 11-110 Remove this section.

11.7.3.13, 11-110 In Figure 11-51, “CRCU Context Register (Write),” change access from “Read/Write” to “Write Only.” In Figure 11-52, “CRCU Context Register (Read-Default Mode),” change access from “Read/Write” to “Read Only.” In Figure 11-53, “CRCU Context Register (Read-Raw Mode),” change access from “Read/Write” to “Read only.”

14.1, 14-1 In Figure 14-1, “Enhanced Local Bus Controller Block Diagram,” update LA signal enumeration to state “LA[27:31].”

14.2, 14-4 In Table 14-1, “Signal Properties—Summary,” update LA signal enumeration to state “LA[27:31].”

14.2, 14-5 In Table 14-2, “Enhanced Local Bus Controller Detailed Signal Descriptions,” update LA signal enumeration to state “LA[27:31].”

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14.3.1.1, 14-11	In Figure 14-2, “Base Registers (BRn),” change reset value of reserved bit 30 from 1 to 0.
14.3.1.14, 14-32	In Table 14-21, “LBCR Field Descriptions,” modify AHD (bit 10) field description, as follows: Address hold disable. Removes part of the hold time for LAD with respect to LALE in order to lengthen the LALE pulse. 0 During address phases on the local bus, the LALE signal negates one platform clock period prior to the address being invalidated. At 33.3 MHz, this provides 3 ns of additional address hold time at the external address latch. 1 During address phases on the local bus, the LALE signal negates 0.5 platform clock period prior to the address being invalidated. This halves the address hold time, but extends the latch enable duration. This may be necessary for very high frequency designs.
14.3.1.14, 14-32	Modify hold time values in description of AHD in Table 14-21, “LBCR Field Descriptions” as follows: 0 During address phases on the local bus, the LALE signal negates 1 platform clock period prior to the address being invalidated. At 533 MHz, this provides 1.8 ns of address hold time at the external address latch. 1 During address phases on the local bus, the LALE signal negates ½ platform clock period prior to the address being invalidated. This halves the address hold time, but extends the latch enable duration. This may be necessary for very high frequency designs.
14.3.1.15, 14-33	In Figure 14-19, “Clock Ratio Register (LCRR),” update final four bits in reset value from “1,0,0,0” to “*n*,*n*,0,0”.
14.4.1.2, 14-42	Update second paragraph to reads as follows: “To ensure adequate hold time on the external address latch, LALE negates earlier than the address changes on LAD during address phases. By default, LALE negates earlier by 1 platform clock period. For example, if the platform clock is operating at 533 MHz, then 1.8 ns of address hold time is introduced. However, at higher frequencies, the duration of the shortened LALE pulse may not meet the minimum latch enable pulse width specifications of some latches. In such cases, setting LBCR[AHD] = 1 increases the LALE pulse width by ½ platform clock cycle, but decreases the address hold time by the same amount. If both longer hold time and longer LALE pulse duration are needed, then the address phase can be extended using the ORn[EAD] and LCRR[EADC] fields, and the LBCR[AHD] bit can be left at 0. However, this will add latency to all address tenures.
14.4.2, 14-47	Update Figure 14-32, “Enhanced Local Bus to GPCM Device Interface,” so that LAD[0:31] of the eLBC connects to the Latch at [12:26] and then connects to A[19:5] in the Memory/Peripheral.

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14.4.2.5, 14-56	In Table 14-32, “Boot Bank field Values after Reset for GPCM as Boot Controller,” update SCY reset default value from “1111” to “From por_cfg_scy[1:3].”
14.4.4.4.1, 14-81	Add the following note to fields LAST and UTA in Table 14-39, “RAM Word Field Descriptions”: “In case of UPM writes, program UTA and LAST in same RAM word. In case of UPM reads, program UTA and LAST in consecutive or same RAM words.”
14.4.4.4.9, 14-86	Add the following paragraph to “LGPL[0:5] Signal Negation (LAST)”: “In case of UPM writes, program UTA and LAST in same RAM word. In case of UPM reads, program UTA and LAST in consecutive or same RAM words.”
14.5.4, 14-95	In first paragraph of sections 14.5.4.4, 14.5.4.5, and 14.5.4.6, change FMR[OP]=01 to FMR[OP]=11.
15.2, 15.4	Change the last bullet to say the following: “Hardware assist for 1588-compliant timestamping (1588 not supported in conjunction with SGMII 10/100).”
15.4, 15-8	In Table 15-1, “eTSEC*n* Network Interface Signal Properties,” modify statement in the signal descriptions for TSEC*n*_TXD[7:4] and TSEC*n*_TXD[3:0] from “unused, output driven zero” to “unused.”
15.5.2, 15-16	In Table 15-4, “Module Memory Map update reset values of RQFCR and RQFPR from “all zeros” to “undefined.”
15.5.2, 15-23	In Table 15-4, “Module Memory Map,” change the access for CAR1 and CAR2 registers from R/W to w1c.
15.5.2, 15-25	In Table 15-4, “Module Memory Map,” change the access of TMR_TEVENT from R/W to w1c.
15.5.3.1.3, 15-29	Add fifth bullet reading, “Special function interrupts are: FGPI, MSRO, MMRD, and MMRW,” to item number three in the numbered item list.
15.5.3.1.3, 15-30	In Table 15-7, “IEVENT Field Descriptions,” change the second sentence of the CRL (bit 14) field description to say the following: “The frame is discarded without being transmitted and the queue halts (TSTAT[THLTn] set to 1).”
15.5.3.1.6, 15-36	In Table 15-10, “ECNTRL Field Descriptions,” update CLRCNT (bit 17) field description to read as follows: “Clear all statistics counters and carry registers. 0 Allow MIB counters to continue to increment and keep any overflow indicators. 1 Reset all MIB counters and CAR1 and CAR2. This bit is self-resetting.”
15.5.3.1.6, 15-36	In Table 15-10, “ECNTRL Field Descriptions,” update AUTOZ (bit 18) field description to read as follows: “Automatically zero MIB counter values and carry registers.

0 The user must write the addressed counter zero after a host read.

1 The addressed counter value is automatically cleared to zero after a host read.

This is a steady state signal and must be set prior to enabling the Ethernet controller and must not be changed without proper care."

15.5.3.1.6, 15-36 In Table 15-10, "ECNTRL Field Descriptions," update GMIIM (bit 25) field description to say the following:

"GMII interface mode. If this bit is set, a PHY with a GMII interface is expected to be connected. If cleared, a PHY with an MII or RMII or RGMII interface is expected. The user should then set MACCFG2[I/F Mode] accordingly. The state of this status bit is defined during power-on reset. See Section 4.4.3, "Power-On Reset Configuration."

0 MII or RMII or RGMII mode interface expected

1 GMII mode interface expected"

15.5.3.1.6, 15-36 In Table 15-10, "ECNTRL Field Descriptions," add the following note to ECNTRL[R100M] bit description: "This bit must be cleared for 1-Gbps SGMII operation."

15.5.3.1.6, 15-37 In Table 15-11, "eTSEC Interface Configurations," update GMIIM column so that GMIIM is set for GMII 1 Gbps and cleared for all other values.

15.5.3.1.8, 15-39 In Table 15-13, "DMACTRL Field Descriptions," change TOD field definition, as follows:

"1 eTSEC immediately fetches a new TxBD from ring 0."

15.5.3.2.1, 15-42 In Table 15-15, "TCTRL Field Description," change TXSCHED field description for 01 state to read as follows: "01 Priority scheduling mode. Frames from enabled TxBD rings are serviced in ascending ring index order."

15.5.3.3.7, 15-64 In Figure 15-30, "Receive Queue Filer Table Control Register Definition," update reset value from "all zeros" to "undefined."

15.5.3.3.8, 15-65 In 15-31, "Receive Queue Filer Table Property IDs 0, 2—15 Register Definition," update reset value from "all zeros" to "undefined."

15.5.3.5.1, 15-75 In Table 15-42, "MACCFG1 Field Descriptions," update MACCFG1[Tx Flow] and MACCFG1[Rx Flow] field descriptions, to include sentence "Must be 0 if MACCFG2[Full Duplex] = 0."

15.5.3.5.1, 15-75 In Table 15-42, "MACCFG1 Field Descriptions," add the following note to Tx_Flow and Rx_Flow: "**Note**: Should not be set when operating in Half-Duplex mode."

15.5.3.5.2, 15-77 In Table 15-43, “MACCFG2 Field Descriptions,” update “Huge Frame” (bit 26) field description, as follows:

Table 15-43. MACCFG2 Field Descriptions

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>26</td><td>Huge Frame</td><td>Huge frame enable. This bit is cleared by default.
0 Limit the length of frames received to less than or equal to the maximum frame length value (MAXFRM[Maximum Frame]) and limit the length of frames transmitted to less than the maximum frame length.
See Section 15.6.8, “Buffer Descriptors,” for further details of buffer descriptor bit updating.
<table>
<tr><th>Frame type</th><th>Frame length</th><th>Packet truncation</th><th>Buffer descriptor updated</th></tr>
<tr><td>Receive or transmit</td><td>> maximum frame length</td><td>yes</td><td>yes</td></tr>
<tr><td>Receive</td><td>= maximum frame length</td><td>no</td><td>no</td></tr>
<tr><td>Transmit</td><td>= maximum frame length</td><td>no</td><td>yes</td></tr>
<tr><td>Receive or transmit</td><td>< maximum frame length</td><td>no</td><td>no</td></tr>
</table>
1 Frames are transmitted and received regardless of their relationship to the maximum frame length. Note that if Huge Frame is cleared, the user must ensure that adequate buffer space is allocated for received frames. See Section 16.5.3.6.5, “Maximum Frame Length Register (MAXFRM),” for further information.</td></tr>
</table>

15.5.3.5.2, 15-78 In Table 15-43, “MACCFG2 Field Descriptions,” modify MPEN (bit 28) field description to say the following:

“Magic packet enable for Ethernet modes. This bit is cleared by default. MPEN should be enabled only after GRACEFUL RECEIVE STOP and GRACEFUL TRANSMIT STOP are completed successfully (in other words, transmission and reception have stopped).

0 Normal receive behavior on receive, or Magic Packet mode has exited with reception of a valid Magic Packet.

1 Commence Magic Packet detection by the MAC provided that frame reception is enabled in MACCFG1. In this mode the MAC ignores all received frames until the specific Magic Packet frame is received, at which point this bit is cleared by the eTSEC, and a maskable interrupt through IEVENT[MAG] occurs.”

15.5.3.5.4, 15-79 In Figure 15-42, “Half-Duplex Register Definition,” and Table 15-45, “HAFDUP Field Descriptions,” update HAFDUP[collision window] field size from 22:31 to 26:31.

15.5.3.5.6, 15-81 In Figure 15-44, “MII Management Configuration Register Definition,” modify offset by adding instantiation for eTSEC3, as follows:

eTSEC1:0x2_4520
eTSEC3:0x2_6520

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15.5.3.5.7, 15-82	In Figure 15-45, “MIIMCOM Register Definition,” modify offset by adding instantiation for eTSEC3, as follows: eTSEC1:0x2_4524 eTSEC3:0x2_6524
15.5.3.5.8, 15-82	In Figure 15-46,“MIIMADD Register Definition,” modify offset by adding instantiation for eTSEC3, as follows: eTSEC1:0x2_4528 eTSEC3:0x2_6528
15.5.3.5.9. 15-83	In Figure 15-47, “MII Mgmt Control Register Definition,” modify offset by adding instantiation for eTSEC3, as follows: eTSEC1:0x2_452C eTSEC3:0x2_652C
15.5.3.5.10, 15-83	In Figure 15-48. MIIMSTAT Register Definition,” modify offset by adding instantiation for eTSEC3, as follows: eTSEC1:0x2_4530 eTSEC3:0x2_6530
15.5.3.5.9, 15-83	Replace Figure 15-47, “MII Mgmt Control Register Definition,” with the following figure that has been updated to show write-only access:

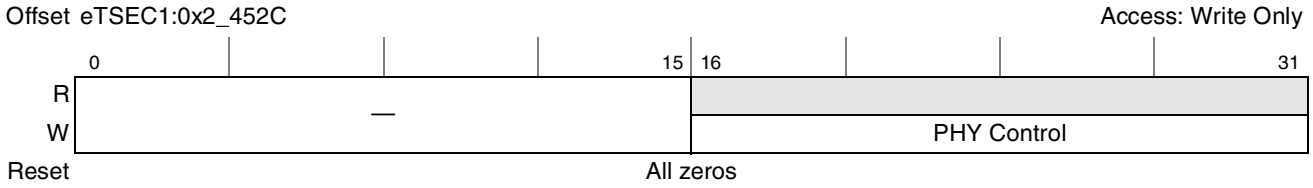

Figure 15-47. MII Mgmt Control Register Definition

15.5.3.5.11, 15-84	In Figure 15-49, “MII Mgmt Indicator Register Definition,” modify offset by adding instantiation for eTSEC3, as follows: eTSEC1:0x2_4534 eTSEC3:0x2_6534
15.5.3.6, 15-88	Add the following note before the TR64 register:

NOTE

The transmit and receive frame counters (TR64, TR127, TR 255, TR511, TR1K, TRMAX, and TRMGV) do not increment for aborted frames (collision retry limit exceeded, late collision, underrun, EBERR, TxFIFO data error, frame truncated due to exceeding MAXFRM, or excessive deferral).

15.5.3.6.17, 15-96	In Table 15-74, “RFLR Field Descriptions,” add the following text to the RFLR (bits 16–31) field description:

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	"Frames tagged with a single VLAN tag are checked for valid length based on bytes 17–18 (rather than 13–14). Frames tagged (stacked) with multiple VLAN tags are not checked for valid length."
15.5.3.6.25, 15-100	In Table 15-82, "TBYT Field Descriptions, update second sentence of the TBYT description to read "This count does not include preamble/SFD or jam bytes, except for half-duplex flow control (back-pressure triggered by TCTRL[THDF] = 1). For THDF, the sum total of 'phantom' preamble bytes transmitted for flow control purposes is included in the TBYT increment value of the next frame to be transmitted, up to 65,535 bytes of frame and phantom preamble."
15.5.3.6.41, 15-108	In Table 15-98, "TOVR Field Descriptions," update field description to read as follows: "Transmit oversize frame counter. Increments each time a frame is transmitted which exceeds 1518 (non VLAN) or 11522 (VLAN) with a correct FCS value."
15.5.3.6.44, 15-110	In Figure 15-98, "Carry Register 1 (CAR1) Register Definition," change access from Read/Write to w1c.
15.5.3.6.45, 15-111	In Figure 15-99, "Carry Register 2 (CAR2) Register Definition," change access from Read/Write to w1c.
15.5.3.9.2, 15-120	In Table 15-110, "ATTRELI Field Descriptions," replace EI (bits 18–25) field description with the following: "Extracted index. Points to the first byte, as a multiple of 64 bytes, within the receive frame as sent to memory from which to begin extracting data."
115.5.3.10.2, 15-122	In Figure 15-109, "RFBPTR0–RFBPTR7 Register Definition," change offset to: "eTSEC1:0x2_4C44+8×*n*; eTSEC2:0x2_5C44+8×*n*; eTSEC3:0x2_6C44+8×*n*; eTSEC4:0x2_7C44+8×*n*"
15.5.3.11, 15-122	Change section name from "Hardware Assist for IEEE 1588 Compatible Timestamping," to "IEEE 1588-Compatible Timestamping Registers."
5.5.3.11.1, 15-123	In Table 15-113, "TMR_CTRL Register Field Descriptions" modify the CIPH (bit 25) field description to say the following: "Oscillator input clock phase. 0 non-inverted timer input clock 1 inverted timer input clock (NOTE: this setting is reserved if CKSEL=01.)"
15.5.3.11.2, 15-124	Change access in Figure 15-111. TMR_TEVENT Register Definition," from Read/Write" to "w1c."
15.5.3.11.9, 15-130	In Figure 15-116, "TMR_ACC Register Definition," modify access from "Read only" to "Read/Write."
15.5.3.11.12, 15-131	In Figure 15-119, "TMR_ALARM1-2_H/L Register Definition," update access from "Mixed" to "Read/Write."
15.5.3.11.13, 15-133	In Figure 15-120, "TMR_FIPERn Register Definition," update access from "Mixed" to "Read/Write."

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15.6.2, 15-157	Replace first bullet under “The following restrictions apply in any of the FIFO modes” with the following: • Transferred packets must by no more than 9600 bytes in length. • If RCTRL[PRSFM]=0, received packets must be a minimum of 10 bytes. If RCTRL[PRSFM]=1, received packets must be a minimum of 14 bytes. • Transmitted packets with L2 headers must be a minimum of 14 bytes. Transmitted packets without L2 headers must be a minimum of 10 bytes.
15.6.2.1, 19-159	Update second sentence of third paragraph to say, “The controller completes any frame in progress before stopping transmission and does not commence counting the pause time until transmit is idle.”
15.6.3.8, 15-175	Modify first paragraph to read as follows: “eTSEC implements the AMD Magic Packet™ specification for LAN-initiated power management. This mode is normally entered with the rest of the system in a low-power doze or nap mode. Software must enable normal receive function in the Ethernet MAC, and then finally set the MACCFG2[MPEN] bit to enable Magic Packet detection before the system enters a reduced mode. While the rest of the system is operating in low-power mode, the enabled eTSEC continues to receive Ethernet frames, but discards them immediately. Upon receipt of any frame whose contents contain the valid Magic Packet sequence, the eTSEC exits out of Magic Packet mode, thus clearing MACCFG2[MPEN], and raises an error/diagnostic interrupt through IEVENT[MAG], which causes the surrounding system to wake-up. Frames received after Magic Packet mode has exited are received into software buffers as usual. Software can abort Magic Packet mode by writing 0 to MACCFG2[MPEN] at any time.”
15.6.3.10, 15-176	Replace three subbullets under first bullet with the following: — Receive data frame interrupts, when bits RXB or RXF in IEVENT are set — Transmit data frame interrupts, when bits TXB or TXF in IEVENT are set — Error, diagnostic, and special interrupts (all bits in IEVENT other than RXB, RXF, TXB, or TXF)
15.6.5.1, 15-186	Add Section 15.6.5.1, “Receive Parser,” as follows:

15.6.5.1 Receive Parser

The receive parser parses the incoming frame data and generates filer properties and frame control block (FCB). The receive parser composes of the Ethernet header parser and L3/L4 parser.

The Ethernet header parser parses only L2 (ethertype) headers. It is enabled by RCTRL[PRSDEP] != 0. It has the following key features:

- Extraction of 48-bit MAC destination and source addresses
- Extraction and recognition of the first 2-byte ethertype field
- Extraction and recognition of the final 2-byte ethertype field
- Extraction of 2-byte VLAN control field

- Walk through MPLS stack and find layer 3 protocol
- Walk through VLAN stack and find layer 3 protocol
- Recognition of the following ethertypes for inner layer parsing
  - LLC and SNAP header
  - JUMBO and SNAP header
  - IPV4
  - IPV6
  - VLAN
  - MPLSU/MPLSM
  - PPPOES
  - ARP

For stack L2 (that is, more than one ethertypes) header, the Ethernet parser traverses through the header until it finds the last valid ethertype or the ethertype is unsupported. Table 15-44 describes what the Ethernet header parser recognizes for stack L2 header.

Table 15-44. Supported Stack L2 Ethernet Headers

Column—Current L2 Ethertype Row—Next Supported L2 Ethertype	LLC/ SNAP	JUMBO/ SNAP	IPV4	IPV6	VLAN	MPLSU	MPLSM	PPOES	ARP
LLC/SNAP	N	N	Y	Y	Y	Y	Y	Y	Y
JUMBO/SNAP	N	N	Y	Y	Y	Y	Y	Y	Y
IPV4	N	N	N	N	N	N	N	N	N
IPV6	N	N	N	N	N	N	N	N	N
VLAN	Y	Y	Y	Y	Y	Y	Y	Y	Y
MPLSU	N	N	Y*	Y*	N	y	Y	N	N
MPLSM	N	N	Y*	Y*	N	Y	Y	N	N
PPOES	N	N	Y	Y	N	Y	Y	N	N
ARP	N	N	N	N	N	N	N	N	N

Note: * means that it is the next protocol

The L3 parser is enabled by RCTRL[PRSDEP] = 10 or 11. It begins when the Ethernet parser ends and a valid IPv4/v6 ethertype is found. The L4 header is enabled by RCTRL[PRSDEP] = 11. It begins when the L3 parser ends and a valid TCP/UDP next protocol is found and no fragment frame is found. The primary functionalities of L3(IPv4/6) and L4(TCP/UDP) parsers are as follows:

- IP recognition (v4/v6, ARP, encapsulated protocol)
- IP header checksum verification

- IPv4/6 over IPv4/6 (tunneling)—parse headers and find layer 4 protocol
- IP layer 4 protocol/next header extraction
- Stop parsing on unrecognized next header/protocol
- IPv4 support
  - IPv4 source and destination addresses
  - 8-bit IPv4 type of service
  - IP layer 4 protocol / next header support
    - IPV4
    - IPV4 Fragment. Parser stops after a fragment is found
    - TCP/UDP
- IPv6 support
  - The first 4 bytes of the IPv6 source address extraction
  - The first 4 bytes of the IPv6 destination address extraction
  - IPv6 source address hash for pseudo header calculation
  - IPv6 destination address hash for pseudo header calculation
  - 8-bit IPv6 traffic class field extraction
  - Payload length field extraction
  - IP layer 4 protocol/next header support
    - IPV6
    - IPV6 fragment. Parser stops after a fragment is found
    - IPV6 route
    - IPV6 hop/destination
    - TCP/UDP
- L4 (TCP/UDP) support
  - Extraction of 16-bit source port number extraction
  - Extraction of 16-bit destination port number extraction
  - TCP checksum calculation (including pseudo header)
  - UDP checksum calculation if the checksum field is not zero (including pseudo header)

15.6.5.2.1, 15-193 Replace Section 15.6.5.2.1, “Priority-Based Queuing (PBQ),” with the following:

“PBQ is the simplest scheduler decision policy. The enabled TxBD rings are assigned a priority value based on their index. Rings with a lower index have precedence over rings with higher indices, with priority assessed on a frame-by-frame basis. For example, frames in TxBD ring 0 have higher priority than frames in TxBD ring 1, and frames in TxBD ring 1 have higher priority than frames in TxBD ring 2, and so on.

The scheduling decision is then achieved as follows:

```
loop
```

```
        # start or S/W clear of TSATn
        ring = 0;
        while ring <= 7 loop
         if enabled(ring) and not ring_empty(ring) then
                transmit_frame(ring);
                ring = 0;
         else
                ring = ring + 1;
         endif
        endloop
endloop
```

15.6.7, 15-197 Add the following note after the third paragraph:

NOTE

IEEE 1588 timestamping is not supported in conjunction with the SGMII 10/100 interface mode.“

15.6.7.2, 15-198 Remove Parser/Data Extraction Logic box and label from figure.

15.6.8.3, 15-207 In Table 15-170, “Receive Buffer Descriptor Field Descriptions,” update Data Length (offset 2–3, bits 0–15) field description, as follows:

“Data length, written by the eTSEC.

Data length is the number of octets written by the eTSEC into this BD’s data buffer if L is cleared (the value is equal to MRBLR), or, if L is set, the length of the frame including CRC, FCB (if RCTRL[PRSDEP > 00), preamble (if MACCFG2[PreAmRxEn]=1), timestamp (if RCTRL[TS]=1) and any padding (RCTRL[PAL]).”

15.7.1.9, 15-238 Add the following note before Table 15-195:

NOTE

SGMII mode utilizes the internal TBI PHY. The internal TBI PHY only auto-negotiates at 1 Gbps. However, 10 Mbps and 100 Mbps speeds are supported in SGMII mode. It is recommended that the external PHY inform the MAC if the desired link speed is not 1 Gbps. Software can perform MII management cycles to determine the external PHY link speed and program ECNTRL and MACCFG2 accordingly.

16.5.3.6.5, 16-41 In Table 15-43, “MAXFRM Descriptions,” modify the first paragraph of “Maximum Frame” (bits 16–31) field description, as follows:

“This field is set to 0x0600 (1536 bytes) by default and always must be set to a value greater than or equal to 0x0040 (64 bytes), but not greater than 0x2580 (9600 bytes).It sets the maximum Ethernet frame size in both the transmit and receive directions. (Refer to MACCFG2[Huge Frame].) It does not affect the size of packets sent or received via the FIFO packet interface.

19.2.1, 19-5 In Figure 19-3, “DMA Signal Summary,” change “$\overline{\text{DMA2\_DREQ1}}$” to “$\overline{\text{DMA2\_DREQ2}}$”.

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19.3.1.4, 19-15 — Replace Figure 19-9, “Source Attributes Registers (SATR*n*),” with the following:

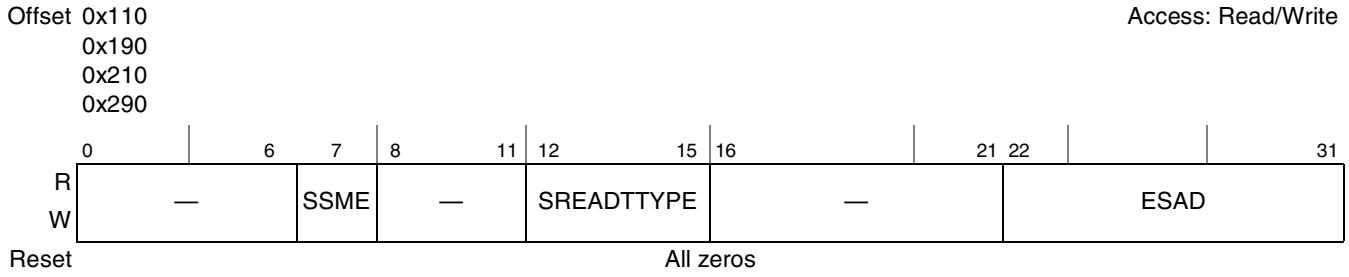

Figure 19-9. Source Attributes Registers (SATR*n*)

19.3.1.4, 19-15 — In Table 19-9, “SATR*n* Field Descriptions,” update 0–6 to show Reserved, remove entries for 3–6 (Reserved, STFLOWLVL, and SPCIORDER), and update 8–11 to show Reserved.

9.4.1.4, 9-18 — In Table 9-9, “TIMING_CFG_3 Field Descriptions,” modify descriptions for 001 and 010 in CNTL_ADJ (bits 29–31) field description, as follows:

“001 MODT[0:3], $\overline{\text{MCS}}$[0:3], and MCKE[0:3] are launched 1/4 DRAM cycle later than the other DRAM address and control signals.

010 MODT[0:3], $\overline{\text{MCS}}$[0:3], and MCKE[0:3] are launched 1/2 DRAM cycle later than the other DRAM address and control signals.”

19.3.1.6, 19-18 — Replace Figure 19-12, “Destination Attributes Registers (DATR*n*) with the following:

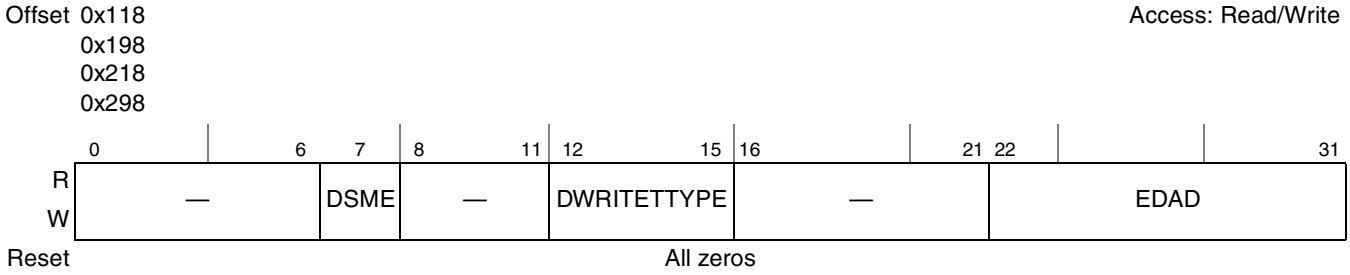

Figure 19-12. Destination Attributes Registers (DATR*n*)

19.4.1.3, 19-18 — Update Table 19-12, “DATR*n* Field Descriptions,” so that bits 0–6 and 8–11 show Reserved.

19.4.1.1.4, 19-29 — Revise first sentence of Step 1 to say, “Set MRn[CDSM/SWSM] and MRn[XFE] and clear MRn[CTM] to indicate extended chaining and single-write start mode.”

9.4.1.19, 9-39 — In Table 9-25, “TIMING_CFG_5 Field Descriptions,” modify the last sentence in RODT_ON (bits 3–7) and WODT_ON (bits 15–19) field descriptions to say the following: “If 2T/3T timing is used, one/two extra cycle(s) is/are automatically added to the value selected in this field.”

9.4.1.24, 9-47 — Modify text concerning legal impedance that follow the numbered list as follows:

“Note that the legal impedance values (from lowest impedance to highest impedance) for DDR2 (1.8 V) are as follows:

- 0000
- 0001
- 0011
- 0010
- 0110
- 0111
- 0101
- 0100
- 1100
- 1101
- 1111 (used for half-strength mode when driver calibration is not used)
- 1110
- 1010 (default full-strength impedance)
- 1011
- 1001

Note that the legal impedance values (from highest impedance to lowest impedance) for DDR3 (1.5 V) are as follows:

- 0000
- 0001
- 0011
- 0010
- 0110
- 0111 (used for half-strength mode when driver calibration is not used)
- 0101
- 0100
- 1100
- 1101
- 1110
- 1010
- 1011 (default full-strength impedance)
- 1001

Note that the drivers may either be calibrated to full-strength or half-strength.”

20.2, 20-1	Remove references to unsupported CRF (critical request flow) functionality throughout section.
20.6.1.5, 20-13	Remove references to unsupported CRF (critical request flow) functionality throughout section.

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20.6.5.2, 20-43	In Table 20-41, “Error/Port-Write Interrupt Status Register (EPWISR),” add the following sentence to the PINT (bit 0) field description: “This bit is also set for outbound doorbell packet response time-out (PRT) errors.”
20.6.5.7, 20-45	In the first paragraph, replace the sentence reading, “The reset value is the maximum time-out interval” with “By default, this time-out value is disabled (all zeros).”
20.6.7.5, 20-54	Remove references to unsupported CRF (critical request flow) functionality throughout section.
20.6.7.6, 20-56	Remove references to unsupported CRF (critical request flow) functionality throughout section.
20.6.7.7, 20-58	Add the following sentence to the end of the first paragraph: “Note that the LCSBA1CSR register (see Section 20.6.1.11, “Local Configuration Space Base Address 1 Command and Status Register (LCSBA1CSR)”) has priority over all ATMU windows if both are configured for the same address space.”
20.7.1.7, 20-69	Remove references to unsupported CRF (critical request flow) functionality throughout section.
20.7.3.4, 20-80	Remove references to unsupported CRF (critical request flow) functionality throughout section.
20.7.4.3, 20-85	In Table 20-92, “IDQDPAR Field Descriptions,” and Table 20-94, “IDQEPAR Field Descriptions,” add the following note to the field descriptions of DQEPA and DQDPA: “Note that this base address must be queue-size aligned.”
20.8.2, 20-91	Remove references to unsupported CRF (critical request flow) functionality in Table 20-103, “RapidIO Small Transport Field Packet Format.”
20.8.12.1, 20-103	Add the following sentences to the end of the third paragraph: “Note that to prevent processor stalls the LOPTTLCR register must be initialized to a non-zero value. See Section 20.6.5.7, ‘Logical Outbound Packet Time-to-Live Configuration Register (LOPTTLCR).’”
20.8.12.3.1, 20-106	Remove references to unsupported CRF (critical request flow) functionality in Table 20-112, “Hardware Errors For Maintenance Response Transactions,”–Table 20-114, “Hardware Errors For DMA Message Response Transactions,” and Table 20-118, “Hardware Errors For Doorbell Response Transactions.”
20.9.4.1.1, 20-142	Replace this section with the following: The outbound doorbell controller interrupt is generated after the completion of a doorbell (done, error, packet response time-out or retry limit exceeded) if this interrupt event is enabled (ODDATR[EODIE] is a 1). The event that caused this interrupt is indicated by ODSR[EODI]. The interrupt is held until the ODSR[EODI] bit has been cleared by writing a 1.
20.9.4.1.8, 20-144	Remove references to unsupported CRF (critical request flow) functionality in Table 20-123, “Outbound Message Direct Mode Hardware Errors.”
20.10.2.1.2, 20-170	Remove second bullet.

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20.10.2.1, 20-170	Modify the subsections of Section 20.10.2.1, “Outbound Doorbell Controller,” as follows:

20.10.2.1.1 Interrupts

The “SRIO outbound doorbell” controller interrupt is generated after the completion of a doorbell (done, error, packet response time-out or retry limit exceeded) if this interrupt event is enabled (ODDATR[EODIE] is a 1). The event that caused this interrupt is indicated by ODSR[EODI]. The interrupt is held until the ODSR[EODI] bit has been cleared by writing a 1.

The “SRIO error/port-write” interrupt can be generated for the following reasons:

- RapidIO error response. An interrupt is generated after a RapidIO error response is received and this interrupt event is enabled (LTLEECSR[MER])
- Packet response time-out. An interrupt is generated after a packet response time-out occurs and this interrupt event is enabled (LTLEECSR[PRT])
- Retry error threshold exceeded. An interrupt is generated after a retry threshold exceeded error occurs and this interrupt event is enabled (LTLEECSR[RETE])

20.10.2.1.2 Error Response Errors

When a RapidIO error response is received by the doorbell controller the following occurs:

- The doorbell controller sets the message error response status bits (ODSR[MER] and LTLEDCSR[MER])
- If LTLEECSR[MER] is set, the interrupt “SRIO error/port-write” is generated.
- After the doorbell operation completes (indicated by ODSR[DUB]) the doorbell controller stops.

20.10.2.1.3 Packet Response Time-Out Errors

When a packet response time-out occurs for a doorbell the following occurs:

- The doorbell controller sets the packet response time-out status bits (ODSR[PRT] and LTLEDCSR[PRT])
- If LTLEECSR[PRT] is set, the interrupt “SRIO error/port-write” is generated and EPWISR[PINT] is set.
- After the doorbell operation completes (indicated by ODSR[DUB]) the doorbell controller stops.

20.10.2.1.4 Retry Error Threshold Exceeded Errors

When a retry error threshold exceeded error occurs for a doorbell the following occurs:

- The doorbell controller sets the retry threshold exceed status bits (ODSR[RETE] and LTLEDCSR[RETE])
- If LTLEECSR[RETE] is set, the interrupt “SRIO error/port-write” is generated.
- After the doorbell operation completes (indicated by ODSR[DUB]) the doorbell controller stops.

20.10.2.1.5 Error Handling

When an error occurs and the “SRIO error/port-write” interrupt is generated, the following occurs:

- Software determines the cause of the interrupt and processes the error
  - LTLEDCSR and ODSR capture the error condition for outbound doorbells
  - EPWISR[PINT] is set for PRT error since it is detected by the SRIO controller
  - Note that LTLEDCSR is a capture once register, so ODSR should be examined to make sure an outbound doorbell error did not occur immediately after another captured error
- Software verifies the doorbell controller has stopped operation by polling ODSR[DUB]
- Software disables the doorbell controller by clearing ODMR[DUS]
- Software clears the error by writing a 1 to the corresponding outbound doorbell status bits (ODSR[PRT], ODSR[PRT], and/or ODSR[RETE] as well as LTLEDCSR)

When an error occurs and the “SRIO error/port-write” interrupt is not enabled, the following occurs:

- Software determines that an error has occurred by polling the status bits (ODSR[MER], ODSR[PRT], and/or ODSR[RETE])
- Software verifies the doorbell controller has stopped operation by polling ODSR[DUB]
- Software disables the doorbell controller by clearing ODMR[DUS]
- Software clears the error by writing a 1 to the corresponding status bits (ODSR[MER], ODSR[PRT], and/or ODSR[RETE])

20.10.2.1.3, 20-171	Remove second bullet.
20.10.2.1.4, 20-171	Remove second bullet.
20.10.2.1.5, 20-171	Remove this section.
20.10.2.1.7, 20-171	Remove references to unsupported CRF (critical request flow) functionality in Table 20-130, “Outbound Doorbell Hardware Errors.”

20.10.2.1.7, 20-172 Update Table 20-130, “Outbound Doorbell Hardware Errors,” as follows:

Table 20-45. Outbound Doorbell Hardware Errors

Transaction	Error	Error Checking Level	Interrupt Generated	Status Bit Set	Doorbell Sent	Logical/Transport Layer Capture Register	Comments
Undefined Packet	Reserved ftype encoding[1]	1	SRIO error/port-write if LTLEECSR[UT] set	Unsupported transaction in the Logical/Transport Layer Error Detect CSR LTLEDCSR[UT]	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	Reserved tt encoding[1]	1	SRIO error/port-write if LTLEECSR[TSE] set	Transport size error in the Logical/Transport Layer Error Detect CSR LTLEDCSR[TSE.	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	Large transport size when operating in small transport size or small transport size when operating in large transport size[1]	1	SRIO error/port-write if LTLEECSR[TSE] set	Transport size error in the Logical/Transport Layer Error Detect CSR LTLEDCSR[TSE.	Yes	Updated with the packet[2]	Packet is ignored and discarded. An error or illegal transaction target error response is not generated.
Doorbell Response	Illegal Destination ID[1]	1	SRIO error/port-write if LTLEECSR[ITTE] set	Illegal transaction target in the Logical/Transport Layer Error Detect CSR LTLEDCSR[ITTE]	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	doorbell not outstanding[1]	1	SRIO error/port-write if LTLEECSR[UR] set	Unsolicited response in the Logical/Transport Layer Error Detect CSR LTLEDCSR[UR]	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	ttype (transaction field) is not doorbell response[1]	1	SRIO error/port-write if LTLEECSR[ITD] set	Illegal transaction decode in the Logical/Transport Layer Error Detect CSR LTLEDCSR[ITD]	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	RapidIO priority is less than or equal to outbound request[1]	2	SRIO error/port-write if LTLEECSR[ITD] set	Illegal transaction decode in the Logical/Transport Layer Error Detect CSR LTLEDCSR[ITD]	Yes	Updated with the packet[2]	Packet is ignored and discarded.

Table 20-45. Outbound Doorbell Hardware Errors (continued)

Transaction	Error	Error Checking Level	Interrupt Generated	Status Bit Set	Doorbell Sent	Logical/Transport Layer Capture Register	Comments
Doorbell Response	Incorrect Source ID[1]	2	SRIO error/port-write if LTLEECSR [ITD] set	Illegal transaction decode in the Logical/Transport Layer Error Detect CSR LTLEDCSR[ITD]	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	reserved response status [1]	2	SRIO error/port-write if LTLEECSR [ITD] set	Illegal transaction decode in the Logical/Transport Layer Error Detect CSR LTLEDCSR[ITD]	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	doorbell response packet size is incorrect[1]	2	SRIO error/port-write if LTLEECSR [MFE] set	Message Format error in the Logical/Transport Layer Error Detect CSR LTLEDCSR[MFE]	Yes	Updated with the packet[2]	Packet is ignored and discarded.
Doorbell Response	error response	3	SRIO error/port-write if LTLEECSR [MER] set.	Message error response in the Logical/Transport Layer Error Detect CSR LTLEDCSR[MER]. ODSR[MER] bit set	Yes	Updated with the corresponding doorbell request packet[2]	doorbell transfer complete
Doorbell Response	number of retries exceeds limit	3	SRIO error/port-write if LTLEECSR [RETE] set.	Retry limit exceeded in the Logical/Transport Layer Error Detect CSR LTLEDCSR[RETE] ODSR[RETE] bit set.	Yes	Updated with the corresponding doorbell request packet[2]	doorbell transfer complete
Doorbell Response	packet response time-out[1]	unrelated	SRIO error/port-write if LTLEECSR [PRT] set.	Packet response time-out in the logical/transport layer error detect CSR LTLEDCSR[PRT] in RapidIO endpoint. ODSR[PRT] bit set.	Yes	Updated with the doorbell request packet in the RapidIO endpoint[2]	doorbell transfer complete. Note that the RapidIO endpoint sends special priority 3 pkt indicating doorbell time-out.

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21.3.1, 21-8	In Table 21-3, “PCI Express Memory-Mapped Register Map,” update reset value for PEXOWAR3 to “0x0000_0000.”
21.3.5.1.4, 21-23	Replace Figure 21-18, “PCI Express Outbound Window Attributes Registers 1–4 (PEXOWAR*n*),” with the two following register figures:

Offset Window 1: 0xC30
Window 2: 0xC50
Window 4: 0xC90

Access: Read/Write

	0	1	2	3	4	5–7	8–10	11	12–15	16–19	20–25	26–31
R W	EN	—		ROE	NS		TC		RTT	WTT	—	OWS
Reset	0	0	0	0	0	0 0 0	0 0 0	0	0 1 0 0	0 1 0 0	0 0 0 0 0 0	1 0 0 0 1 1

Figure 20-18. PCI Express Outbound Window Attributes Registers 1, 2, 4 (PEXOWAR*n*)

Offset Window 3: 0xC70

Access: Read/Write

	0	1	2	3	4	5–7	8–10	11	12–15	16–19	20–25	26–31
R W	EN	—		ROE	NS		TC		RTT	WTT	—	OWS
Reset[1]	All zeros											

Figure 20-19. PCI Express Outbound Window Attributes Register 3 (PEXOWAR3)

[1] If the device is configured to use the alternate boot vector (cfg_boot_vec = 0), the reset value for PCI controller 1 PEXOWAR3 is 0x8004_400F. If the device is not configured to use the alternate boot vector (cfg_boot_vec = 1), the reset value for PCI controller 1 PEXOWAR3 is 0x0000_0000.

21.3.5.1.4, 21-23	Add the following footnote to Figure 21-18, “PCI Express Outbound Window Attributes Register 1–4 (PEXOWARn): “The reset value for PCI controller 1 PEXOWAR3 is 0x0000_0000.”
21.3.7.2, 21-45	Replace this section with the following paragraphs: “When the PCI Express controller is configured as an EP device it responds to remote host generated configuration cycles. This is indicated by decoding the configuration command along with type 0 access in the packet. A remote host can access all of the PCI Express configuration area except the PCI Express Controller Internal CSR registers in the extended PCI Express configuration space at offsets 0x400–0x6FF. The PCI Express Controller Internal CSR registers are not accessible by inbound PCI Express configuration transactions. Attempts to access these registers return all zeros. While in EP mode, the PCI Express controller does not support generating configuration accesses as a master. All accesses to PEX_CONFIG_ADDR/PEX_CONFIG_DATA cause the device to access the internal configuration registers regardless of the targeted bus number or targeted device number programmed in the PEX_CONFIG_ADDR register. There is no configuration mechanism supported in EP mode using the ATMU window. If the outbound ATMU window is configured to issue a configuration transaction, all posted transactions hitting this window are ignored and all non-posted transactions get a response with an error.”

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21.3.8.1.4, 21-48	Modify the access in Figure 21-40, “PCI Express Status Register,” from “w1c” to “Mixed.”
21.3.9.3, 21-71	Modify the access in Figure 21-81, “PCI Express Power Management Status and Control Register,” from “w1c” to “Mixed.”
21.3.9.9, 21-74	Modify the access in Figure 21-87, “PCI Express Device Status Register,” from “w1c” to “Mixed.”
21.3.9.15, 21-78	Modify the access in Figure 21-93, “PCI Express Slot Status Register,” from “w1c” to “Mixed.”
21.3.10.5, 21-87	Modify the access in Figure 21-106, “PCI Express Correctable Error Status Register,” from “Read/Write” to “w1c.”
21.3.10.10, 21-90	Modify the access in Figure 21-111, “PCI Express Root Error Status Register,” from “w1c” to “Mixed.”
21.4.1.8, 21-104	Revise first paragraph by removing “originating from the PCI Express outbound ATMUs,” from the first sentence. In addition, remove the last sentence that states, “Note that configuration writes originating from the PCI Express configuration access registers (PEX_CONFIG_ADDR/PEX_CONFIG_DATA) are not serialized.”
23.4, 23-4	In Table 23-3, “Global Utilities Block Register Summary,” change reset value for PORDEVSR2 to “see ref.”
23.4.1.1, 23-5	In Figure 23-1, “POR PLL Status Register (PORPLLSR),” update DDR_Ratio (bits 18–22) field description, as follows:

Table 23-1. POR PLL Status Register (PORPLLSR)

Bits	Name	Description
18–22	DDR_Ratio	Clock ratio between the DDR Complex clock and DDRCLK. Patterns not shown are reserved. 00011 3:1 01010 10:1 00100 4:1 01100 12:1 00110 6:1 01110 14:1 01000 8:1 00111 Synchronous Mode-DDR Complex Clocked by CCB clock

23.4.1.6, 23-12	Update the reset value for Figure 23-6, “POR Device Status Register 2 (PORDEVSR2),” as follows:

Offset 0xE_0014 Access: Read only

	0	16	17	18	19	24	25	26	27	28	29	30	31
R	—		SRDS_SGMII_EN	SRDS_SGMII_REFCLK	—		ENG_USE	FCM_ECC	—		SRDS1_EN	—	
W													
Reset	1 0 0 0 1 1 1 1 0 0 0 0	0 0 0 0	1	*n*	*n*	0	0 0 0 0	0	*n*	*n*	1	1	*n*	0 0

Figure 23-6. POR Device Status Register 2 (PORDEVSR2)

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23.4.1.9, 23-19	Update access from “Mixed” to “Read/Write” in Figure 23-9, “Device Disable Register (DEVDISR).”
23.4.1.14, 23-21	Update access from “w1c” to “Mixed” in Figure 23-14, “Checkstop Status and Control Register (AUTORSTSR).”
23.4.1.20, 23-26	In Table 23-23, “CLKOCR Field Descriptions,” update 10x111 in the CLK_SEL description from “Logic 0” to “Reserved.”
24.3.2.2, 24-8	In Table 24-4, “PMLCA1—PMLCA11 Field Descriptions,” remove the note beginning “Note that with counter specific events...” from EVENT field description.
24.4.7, 24-16	Replace the L2 Cache/SRAM Events section of Table 24-10, “Performance Monitor Events” with the following:

L2 Cache/SRAM Events		
Core instruction accesses to L2 that hit	C2:123	—
Core instruction accesses to L2 that miss	Ref:23	—
Core data accesses to L2 that hit	C4:121	—
Core data accesses to L2 that miss	C5:115	—
Non-core burst write to L2 (cache external write or SRAM)	C6:120	—
Non-core non-burst write to L2	C7:116	—
Noncore write misses cache external write window and SRAM memory range	Ref:24	—
Non-core read hit in L2	C1:118	—
Non-core read miss in L2	Ref:25	—
L2 allocates, from any source	C2:124	—
L2 retries due to full write queue	C3:122	—
L2 retries due to address collision	C4:122	—
L2 failed lock attempts due to full set	C5:116	—
L2 victimizations of valid lines	C6:121	—
L2 invalidations of lines	C7:117	—
L2 clearing of locks	Ref:22	—

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