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Errata to MPC862 PowerQUICC Integrated Communications Family Reference Manual, Rev. 3

Supports MPC862P, MPC862T, MPC857T, and MPC857DSL

This errata describes corrections to the *MPC862 PowerQUICC Integrated Communications Family Reference Manual*, Revision 3. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page	Changes
18.7, 18-14	Beneath Table 18-11, add the following: Note: Locations 0x3cac/0x3dac contain a 16-bit internal DPRAM offset to the actual I2C/SPI parameter RAM. Either they must be left alone after a CPM reset or can be initialized to point to a 32-byte aligned parameter area containing the I2C/SPI parameter areas to allow I2C/SPI parameter relocation in case of a parameter RAM conflict.
21.2.4, 20-11	In Table 21-4, “TODR Field Descriptions,” in TOD field description, change “TOD is cleared automatically after one serial clock...” to say “TOD is cleared automatically after 1 system clock...”
21.3, 21-12	Under third bullet point, change “For an RxBD, the value must be even,” to say, “For an RxBD, the value must be mod 4 aligned.”
28.7, 28-7	In Table 28-5, change the third sentence in the Transmitter Underrun description to read as follows: Underrun in transparent mode occurs when the CPM or SDMA is experiencing a latency issue and cannot keep up with the transmission rate.

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Section, Page No.	Changes
32.8, 32-20	Add a note to beginning of section, as follows: “PIP in transparent mode is not supported.”
41.2.7, 41-7	Add the following to procedure step number 4: The utopia serial clock domain is fed from the UtpClk external pin. Even in internal clock mode, the Utopia clock is driven to the output pad and fed back from pad input beffer to the utopia block. When the PDPAR[UT] bit is set (regardless of whether utopia module is actually being used, or just for the purpose of using MII-MDC in muxed mode operation), PDPAR[utpclk] needs to be set to provide clock to the utopia module regardless of UTMODE[TCLK] setting as input or output.

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