AH1401

Application Hints - Dual high speed CAN transceiver TJA1059

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Document information

Info	Content
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Summary

The intention of this application hints document is to provide the necessary information for hardware and software designers for creation of automotive applications using the dual high speed CAN transceiver TJA1059.

Revision history

Rev	Date	Description
1.0	2014-01-09	Initial version

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Contents

1. Introduction

The TJA1051, TJA1042, TJA1043, TJA1048, TJA1059 and TJA1049 and their variants TJA1042/3, TJA1051/3, TJA1051/E, TJA1049/3 are 3rd generation standalone high speed CAN transceivers from NXP Semiconductors and a step up from high speed CAN transceivers TJA1040, TJA1041A and TJA1050 (see Fig 1).

All transceivers provide the physical link between the protocol controller and the physical transmission medium according to the ISO11898 ([2], [3]) and SAE J2284 [4]. This ensures full interoperability with other ISO11898 compliant transceiver products.

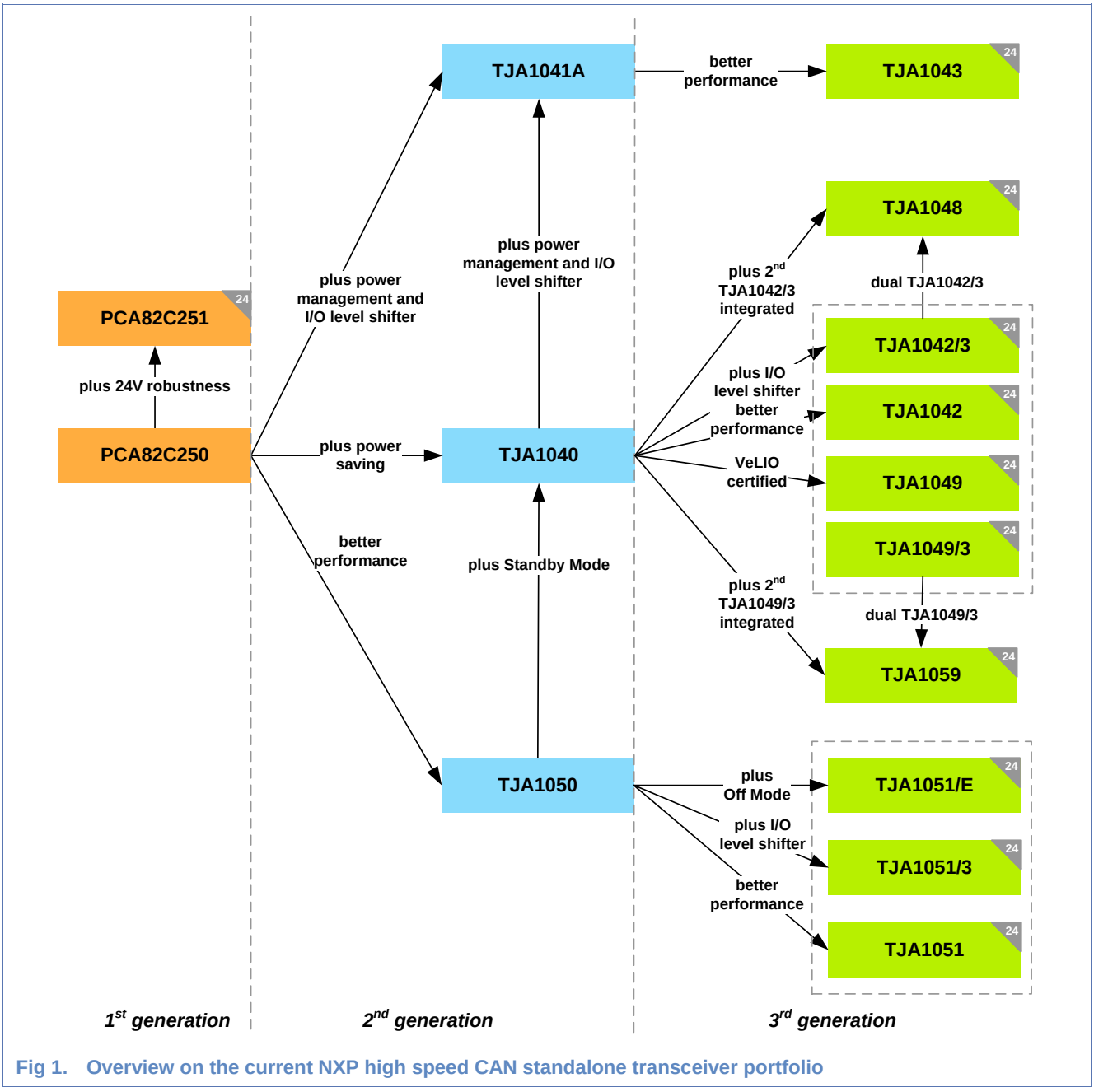


Fig 1. Overview on the current NXP high speed CAN standalone transceiver portfolio

The TJA1049/3, TJA1042/3 and TJA1051/3 allow interfacing to 3V microcontrollers via pin V_{IO}. The TJA1051/E offers a dedicated Off mode to completely disable the transceiver. The dual high speed CAN standalone transceiver TJA1048 offers two integrated TJA1042/3 blocks. The dual high speed CAN standalone transceiver TJA1059 offers two integrated TJA1049/3 blocks.

Compared to their functional predecessors the 3rd generation high speed CAN transceivers from NXP Semiconductors offer

- a significantly improved ESD robustness,
- a further reduction in electromagnetic emission (EME)
- beside an improved electromagnetic immunity (EMI),
- a higher voltage robustness in order to full support 24V applications
- and a predictable undervoltage behavior at all supply conditions.

With the extended portfolio of high speed CAN transceivers NXP Semiconductors enables ECU designers to find the best application fitting standalone transceiver product in order to cover all main application specific requirements (Fig 2).

			Modes					Fail-safe features						Wake-up			
HSCAN device	No. of pins	No. of CAN channels	Normal	Listen-only	Standby	Sleep	Off	TXD dominant timer	Bus dominant timer	Undervoltage detection	Short circuit protection	Temperature protection	Error detection	Remote via CAN	Local via WAKE	Host Interface	SPLIT pin
TJA1051	8	1	√	√				√		√	√	√				5V	
TJA1051/3	8	1	√	√				√		√	√	√				3-5V	
TJA1051/E	8	1	√	√			√	√		√	√	√				5V	
TJA1042	8	1	√		√			√	√	√	√	√		√		5V	√
TJA1042/3	8	1	√		√			√	√	√	√	√		√		3-5V	
TJA1049[1]	8	1	√		√			√	√	√	√	√		√		5V	√
TJA1049/3[1]	8	1	√		√			√	√	√	√	√		√		3-5V	
TJA1048	14	2	√		√			√		√	√	√		√		3-5V	
TJA1059[1, 2]	14	2	√		√			√		√	√	√		√		3-5V	
TJA1043	14	1	√	√	√	√		√		√	√	√	√	√	√	3-5V	√

[1] VeLIO certified

[2] Comply with all global OEM requirements; allows a one-fits-all approach

Fig 2. Feature overview of 3rd generation high speed CAN standalone transceiver portfolio

2. Basics of high speed CAN applications

The protocol controller outputs a serial transmit data stream to the TXD input of the CAN transceiver. An internal pull-up function sets the TXD input to logic HIGH, which means that the bus output driver stays recessive in the case of a TXD open circuit condition. In the recessive state (Fig 3) the CANH and CANL pins are biased to a voltage level of V_{CC} divided by 2. If a logic LOW level is applied to TXD, the output stage is activated, generating a dominant state on the bus line Fig 3.

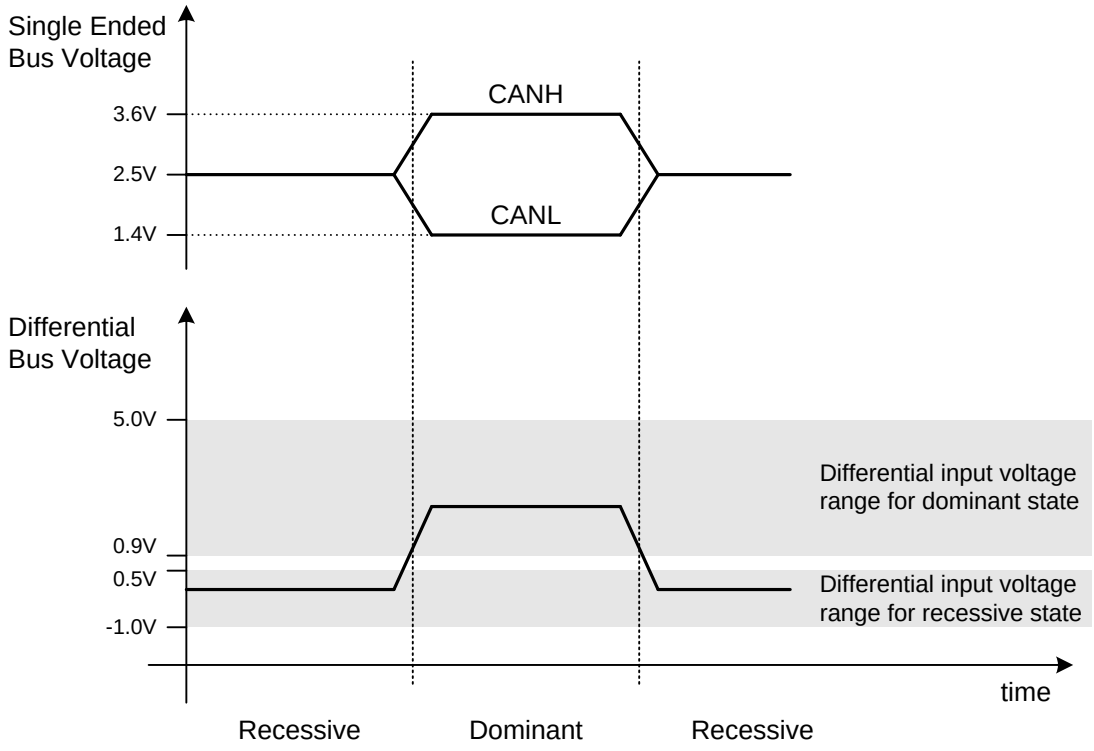


Fig 3. Nominal bus levels according to ISO11898

If no bus node transmits a dominant bit, the bus stays in recessive state. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal to a logic level signal, which is output at RXD. The serial receive data stream is provided to the bus protocol controller for decoding. The internal receiver comparator is always active. It monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.

Details about high speed CAN applications in general are explained in the NXP application hints document [5] — Rules and recommendations for in-vehicle CAN networks.

3. The TJA1059 – Dual high speed CAN transceiver with Standby Mode

3.1 Main features

The TJA1059 is a dual high-speed CAN transceiver from NXP Semiconductors providing two independent CAN channels with a low power mode (called Standby mode) besides a Normal mode. The TJA1059 can be interfaced directly to microcontrollers with supply voltages from 3V to 5V [1].

The TJA1059 is the excellent choice for all types of HS-CAN networks containing more than one HS-CAN interface that require a low-power mode with wake-up capability via the CAN bus, especially for Body Control and Gateway units.

Due to the compliance with all global OEM requirements the TJA1059 allows a one-fits-all approach.

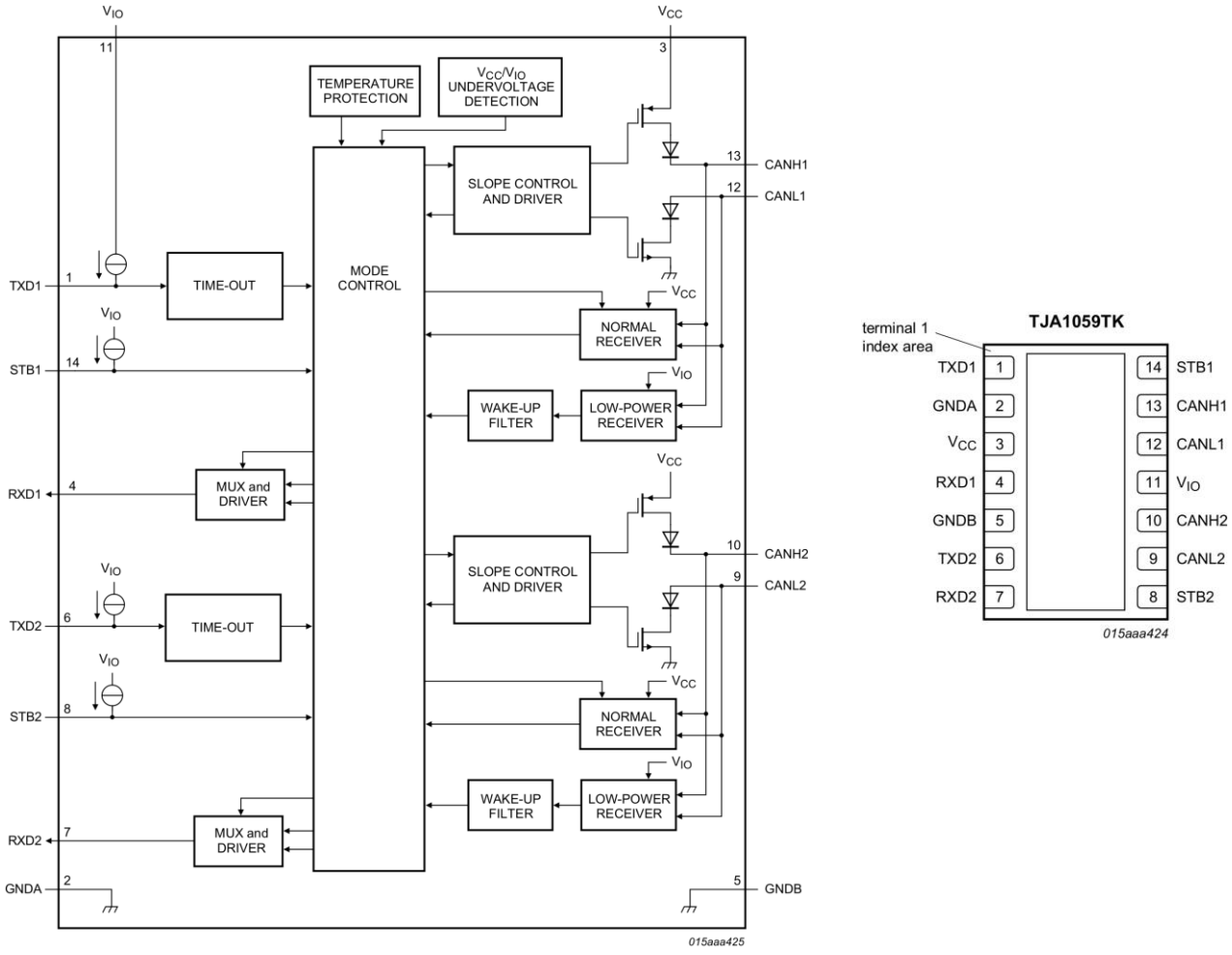


Fig 4. Block diagram and pinning of the TJA1059

3.2 Operating modes

The TJA1059 offers 2 different power modes, Normal mode and Standby mode which are directly selectable for each CAN channel. Taking into account the V_{IO} undervoltage condition a third power mode can be entered; the so-called OFF mode, selected generally for both CAN channels. Fig 5 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.

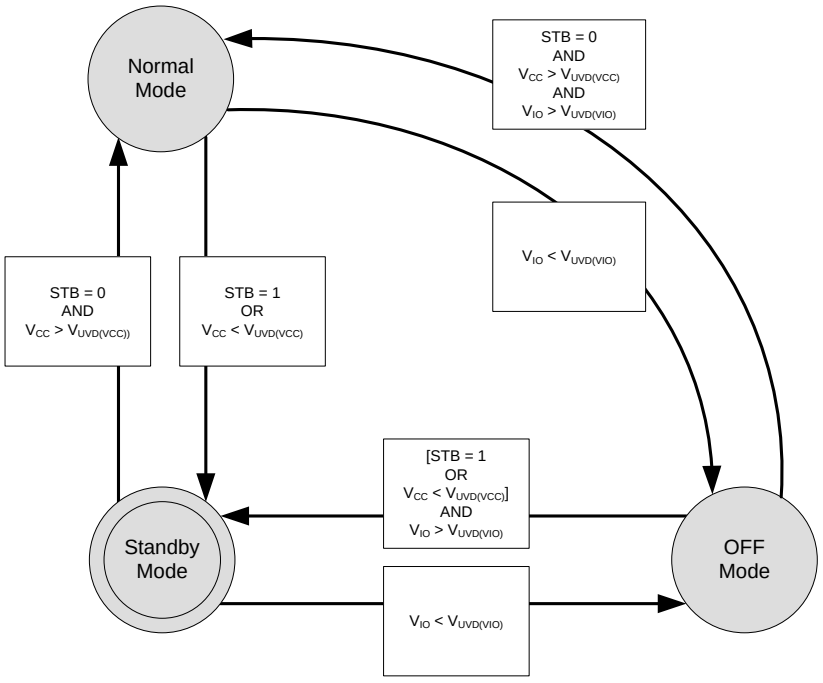


Fig 5. State diagram TJA1059

3.2.1 Normal Mode

In Normal mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{CC}/2$ in recessive state and the transmitter is enabled. The Normal mode is entered setting STB1 or STB2 to LOW. Switching into Normal mode is CAN channel independently.

In Normal mode the transceiver provides the following functions:

- The CAN transmitter is active.
- The normal CAN receiver is active.
- The low power CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- Pin RXD reflects the normal CAN Receiver.
- V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.

3.2.2 Standby Mode

The Standby mode is used to reduce the power consumption of the TJA1059 significantly. In Standby mode the specific CAN channel is not capable of transmitting and receiving regular CAN messages, but it monitors the bus for CAN messages. After passing the wake-up filter the bus signal is transferred to RXD with an additional time delay $t_{fltr(wake)bus}$. To reduce the current consumption as far as possible the bus is terminated to GND rather than biased to $V_{CC}/2$ as in Normal mode. The Standby mode is selected setting STB1 or STB2 to HIGH channel independently or by undervoltage detection on V_{CC} for both channels at the same time. Due to an internal pull-up function on the pins STB1 and STB2 it is the default mode if the pins are unconnected.

In Standby mode the transceiver provides the following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is active.
- CANH and CANL are biased to GND.
- Pin RXD reflects the low power CAN receiver.
- V_{IO} undervoltage detector is active for undervoltage detection.
- V_{CC} undervoltage detector may be disabled.

3.2.3 OFF Mode

The non-operation Off mode is introduced offering total passive behaviour the to bus system. The OFF mode is entered by undervoltage detection on V_{IO}. Entering and leaving OFF Mode is done for both channels at the same time, thus not independently. In OFF mode the transceiver provides the following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- V_{IO} undervoltage detector is active for undervoltage detection.
- V_{CC} undervoltage detector may be disabled.

Table 1. Characteristics of the different modes

Ch1 Op. mode	Ch2 Op. mode	STB1 pin	STB2 pin	V_{CC} underv.	V_{IO} underv.	RXD1 pin		Bus1 bias	RXD2 pin		Bus2 bias
						Low	High		Low	High	
Normal	Normal	0	0	no	no	Bus dom.	Bus rec.	$V_{CC}/2$	Bus dom.	Bus rec.	$V_{CC}/2$
Standby	Normal	1	0	no	no	Wake-up detected	No wake-up detected	GND	Bus dom.	Bus rec.	$V_{CC}/2$
Normal	Standby	0	1	no	no	Bus dom.	Bus rec.	$V_{CC}/2$	Wake-up detected	No wake-up detected	GND
Standby	Standby	1	1	no	no	Wake-up detected	No wake-up detected	GND	Wake-up detected	No wake-up detected	GND
Standby	Standby	X	X	yes	no	Wake-up detected	No wake-up detected	GND	Wake-up detected	No wake-up detected	GND
OFF	OFF	X	X	X	yes	-	-	float	-	-	float

3.3 Remote Wake-up (via CAN bus)

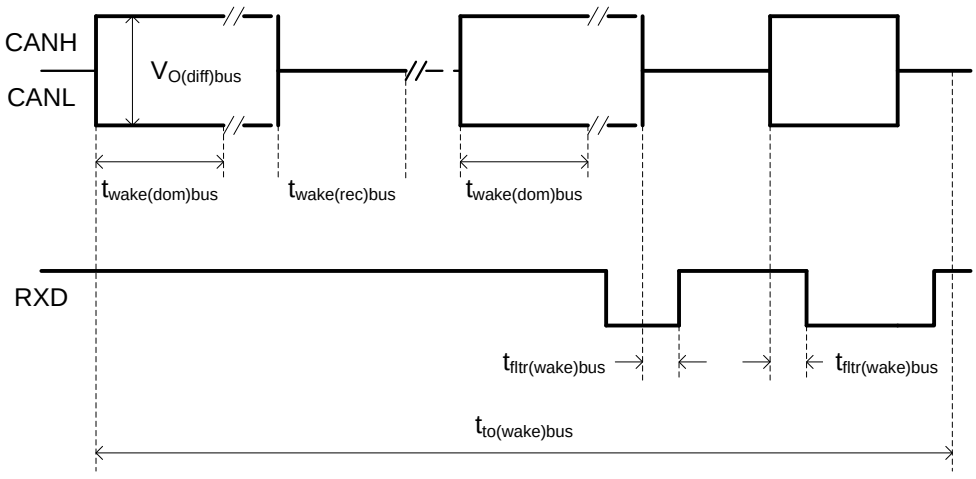
In comparison to the TJA1049 the TJA1059 offers a slightly enhanced remote wake-up procedure. The TJA1049 in Standby mode transfers the bus signal to RXD with an additional time delay $t_{fltr(wake)bus}$ in oder to filter noise and spikes.

A dedicated wake-up sequence (specified in ISO11898-5) must be received to wake-up the TJA1059 from Standby mode [1]. This filtering improves the robustness against spurious wake-up events due to a dominant clamped CAN bus or dominant phases caused by noise or spikes on the bus.

The wake-up pattern consists of:

- A dominant phase of at least $t_{wake(busdom)}$ followed by
- A recessive phase of at least $t_{wake(busrec)}$ followed by
- A dominant phase of at least $t_{wake(busdom)}$

The complete dominant-recessive-dominant pattern must be completed within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Fig 6). Otherwise the internal wake-up logic gets reset and the complete wake-up pattern needs to be re-applied to the low power receiver of CAN1 or CAN2 before generating a proper remote wake-up. Pins RXD1 and RXD2 will remain high until the wake-up event has been triggered.



$t_{to(wake)bus}$ = 0.5ms to 5ms

$t_{fltr(wake)bus}$ = 0.5µs to 5µs

$t_{wake(busdom)}$ = $t_{wake(busrec)}$ = 0.5µs to 5µs

Fig 6. Wake-up timings and behaviour

After the wake-up sequence has been detected, the TJA1059 behaves equal to the TJA1049 and will remain in Standby mode with the bus signals reflected on RXD1/RXD2. Note that dominant or recessive phases less than $t_{fltr(wake)bus}$ will not be detected by the low power differential receiver and will not be reflected on RXD1/RXD2 in Standby mode.

A wake-up event will not be registered if any of the following events occurs while a wake-up sequence is being received:

- The TJA1059 switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{IO} undervoltage was detected ($V_{IO} < V_{uvd(VIO)}$)

If any of these events occurs while a wake-up sequence is being received, the internal wake-up logic will be reset and the complete wake-up sequence will have to be re-transmitted to trigger a wake-up event.

3.4 System fail-safe features

3.4.1 TXD dominant clamping detection in Normal Mode

The TXD dominant clamping detection prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TXD signal.

After a maximum allowable TXD dominant time $t_{to(dom)TXD}$ the transmitter is disabled (see Fig 7). According to the CAN protocol only a maximum of eleven successive dominant bits are allowed on TXD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TXD dominant time, this limits the minimum bit rate to 40 kbit/s.

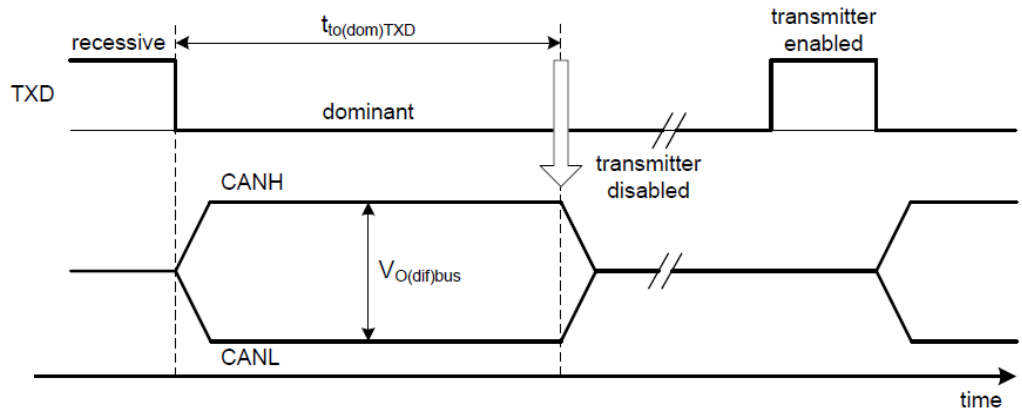


Fig 7. TXD dominant clamping in Normal mode

3.4.2 Bus dominant clamping prevention at entering Normal Mode

The TJA1059 provides bus dominant clamping prevention at entering Normal mode. The TXD pin needs to be set HIGH before transmitting its first dominant bit to the bus in Normal mode. This prevents the transceiver clamping the entire bus when starting up with not well defined TXD.

3.4.3 Bus dominant clamping detection in Standby Mode

The extended wake-up filter allows a system enter the Standby mode even with a permanently dominant clamped bus (see also chapter 3.3). Because the first wake-up sequence will not be passed. In this case the RXD pin keeps high. For same reasons the RXD keeps high if the dominant clamped bus occurs in Standby mode. If the wake-up filter is passed for certain reasons and the bus keeps clamped dominat the RXD becomes low and keeps this state as long as the failure is present.

3.4.4 Undervoltage detection & recovery

The TJA1059 provides two supply pins, V_{CC} and V_{IO}. The V_{CC} voltage is needed for the CAN physical interface. V_{CC} provides the current needed for the CAN transmitter and receiver in Normal mode. Pin V_{IO} should be connected to the microcontroller supply voltage. This will adjust the signal levels of pins TXD1, TXD2, RXD1, RXD2, STB1 and STB2 to the I/O levels of the microcontroller. Pin V_{IO} also provides the internal supply voltage for the low power differential receiver of each integrated transceiver. For applications running in low power, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}.

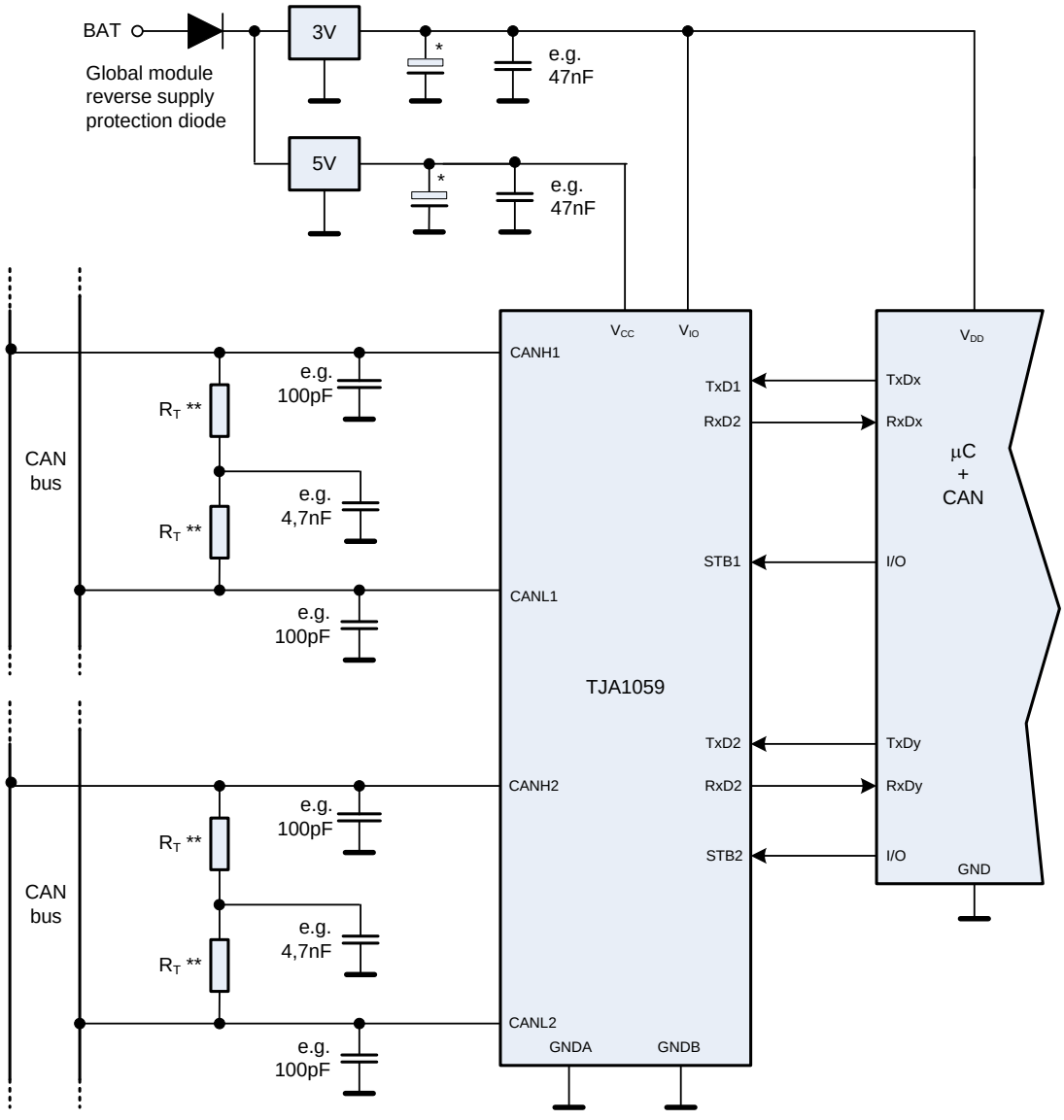
Both voltages are independent from each other. An undervoltage detection circuitry at V_{CC} and V_{IO} indicates either a V_{CC} or V_{IO} undervoltage condition that is used for mode control. A V_{CC} undervoltage condition forces both CAN channels of the TJA1059 to enter Standby mode. The logic state of pins STB1 and STB2 will be ignored until V_{CC} has recovered. This allows saving current in case of switching off the supply voltage or faulty behaviour of host electronic control unit. As long as V_{IO} keeps present the TJA1059 offers the full wake-up capability. A V_{IO} undervoltage condition forces both CAN channels of the TJA1059 to switch off (OFF mode) and to disengage from the bus (zero loads) until V_{IO} has recovered. In OFF mode both CAN transceivers behave passive to the bus. Table 2 gives an overview of the undervoltage behaviour. As long as no undervoltage is detected the TJA1059 keeps fully operational.

Table 2. Device behaviour in different power conditions

Undervoltage condition		Operating mode	CAN1 / CAN2 biasing	Bus wake-up capability
V_{CC}	V_{IO}			
no	no	Normal or Standby	$V_{CC}/2$ or GND	yes
yes	no	Standby	GND	yes
no	yes	OFF	float	no
yes	yes	OFF	float	no

3.5 Hardware application

Fig 8 shows how to integrate the TJA1059 within a typical application. The application example assumes a 3V supplied host microcontroller. There is a dedicated 5V regulator supplying the TJA1059 transceiver on its V_{CC} supply pin (necessary for proper CAN transmit capability).



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kΩ ...4,7kΩ can be foreseen, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 8. Application diagram TJA1059

Note: For detailed hardware application guidance please refer to next chapters explaining how the pins of the TJA1059 are properly connected in an application environment.

3.5.1 V_{CC} pin

The V_{CC} supply provides the current needed for the transmitter and receiver of the high speed CAN transceiver. The V_{CC} supply must be able to deliver current of 90 mA in average for the transceiver (see chapter 3.5.1.1).

Typically a capacitor between 47nF and 100nF is recommended being connected between V_{CC} and GND close to the transceiver. This capacitor buffers the supply voltage during the transition from recessive to dominant, when there is a sharp rise in current demand.

Using a linear voltage regulator, it is recommended to stabilize the output voltage with an additional bypass capacitor (see chapter 3.5.1.2) that is usually placed at the output of the voltage regulator. Its purpose is to buffer disturbances on the battery line and to buffer extra supply current demand in the case of bus failures. The calculation of the bypass capacitor value is shown in chapter 3.5.1.2, while in chapter 3.5.1.1 the average V_{CC} supply current is calculated for thermal load considerations of the V_{CC} voltage regulator. This can be done in absence and in presence of bus short-circuit conditions.

3.5.1.1 Thermal load consideration for the V_{CC} voltage regulator

The averages V_{CC} supply current can be calculated in absence and in presence of bus short-circuit conditions (see Table 3). Assuming a transmit duty cycle of 50% on pin TXD the maximum average supply current in absence of bus failures calculates to:

$$I_{CC\_norm\_avg} = 0.5 \bullet (I_{CC\_REC\_MAX} + I_{CC\_DOM\_MAX})$$

Table 3. Maximum V_{CC} supply current in recessive and dominant state

Device	$I_{CC\_REC\_MAX}$ [mA]	$I_{CC\_DOM\_MAX}$ [mA]
TJA1059	20 (both channel recessive)	140 (both channel dominant)

This results in an average supply current of $I_{CC\_norm\_avg}$ = 80mA.

In presence of bus failures the V_{CC} supply current for the transceiver can increase significantly (see Table 4). The maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ flows in the case of an applied short circuit between CANH to GND. Along with the CANH short circuit output current $I_{O(dom)MAX}$ = 100mA the maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ calculates to about 220mA.

$$I_{CC\_DOM\_SC\_MAX} = (I_{CC\_REC\_MAX} + I_{O(dom)MAX})$$

This results in an average supply current of 110mA in worst case of a short circuit from CANH to GND. The V_{CC} voltage regulator must be able to handle this average supply current.

Table 4. Average V_{CC} supply current

Device	$I_{CC\_norm\_avg}$ [mA]	$I_{CC\_AVG\_SC\_MAX}$ [mA]
TJA1059	80 (both channels transmitting)	220 (both channels shorted)

3.5.1.2 Dimensioning the bypass capacitor of the voltage regulator

Depending on the power supply concept, the required worst-case bypass capacitor and the extra current demand in the case of bus failures can be calculated.

$$C_{BUFF} = \frac{\Delta I_{CC\_\max\_sc} \cdot t_{dom\_\max}}{\Delta V_{\max}}$$

Dimensioning the capacitor gets very important with a shared voltage supply between transceiver and microcontroller. Here, extra current demand with bus failures may not lead to an unstable supply for the microcontroller. This input is used to determine the bypass capacitor needed to keep the voltage supply stable under the assumption that all the extra current demand has to be delivered from the bypass capacitor.

The quiescent current delivered from the voltage regulator to the transceiver is determined by the recessive V_{CC} supply current I_{CC_REC}.

In absence of bus failures the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max} = (I_{CC\_DOM\_MAX} - I_{CC\_REC\_MIN})$$

In presence of bus failures the maximum extra supply current may be significantly higher.

Considering the worst case of a short circuit from CANH to GND the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max\_sc} = (I_{CC\_DOM\_SC\_MAX} - I_{CC\_REC\_MIN})$$

Example:

With $I_{CC\_dom\_sc\_max}$ = 220 mA (estimated) and $I_{CC\_rec\_min}$ = 4 mA the maximum extra supply current calculates to

$$\Delta I_{CC\_max\_sc} = 216 \text{ mA}$$

In the case of a short circuit from CANH to GND, the bus is clamped to the recessive state, and according to the CAN protocol the uC transmits 17 subsequent dominant bits on TXD. That would mean the above calculated maximum extra supply current has to be delivered for at least 17 bit times. The reason for the 17 bit times is that at the moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to RXD and forces an error frame due to the bit failure condition. The first bit of the error frame again is not reflected at RXD and forces the next error frame (TX Error Counter +8). Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the V_{CC} supply current becomes reduced to the recessive one.

Assuming that the complete extra supply current during the 17 bit times has to be buffered by the bypass capacitor, the worst-case bypass capacitor calculates to:

$$C_{BUFF} = \frac{\Delta I_{CC\_\max\_sc} \cdot t_{dom\_\max}}{\Delta V_{\max}}$$

Whereas ΔV_{max} is the maximum allowed voltage drop at pin V_{CC} and t_{dom_max} is the dominant time of 17 bit times at 500kbit/s.

Table 5. Average V_{CC} supply current (assuming 500kbit/s)

Device	$\Delta I_{CC\_max\_sc}$	t_{dom_max}	ΔV_{max}	C_{BuFF}
TJA1048	216mA	34µs	0,25V	≈ 30µF

Of course, depending on the regulation capabilities of the used voltage regulator the bypass capacitor may be much smaller.

3.5.2 V_{IO} pin

Pin V_{IO} is connected to the microcontroller supply voltage to provide the proper voltage reference for the input threshold of digital input pins and for the HIGH voltage of digital outputs. It defines the ratiometric digital input threshold from as 2.85V to 5.25V.for interface pins like TXD1, TXD2, STB1 and STB2 and the HIGH-level output voltage for RXD1 and RXD2.

Also for the TJA1059 the low-power differential receiver is supplied out of pin V_{IO}. This allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}. This allows applications with even less quiescent current because the 5V regulator can be switched off entirely keeping bus wake-ups still possible. If there is detected an undervoltage condition the transceiver will switch into OFF mode and both CAN channels will be invisible onto the bus.

3.5.3 TXD pin

The transceiver receives the digital bit stream to be transmitted onto the bus via the pin TXD. When applied signals at TXD show very fast slopes, it may cause a degradation of the EMC performance. Depending on the OEM an optinal series resistor of up to 1kΩ within the TXD line between transceiver and microcontroller might be useful. Along with pin capacitance this would help to smooth the edges for some degree. For high bus speeds (close to 1 Mbit/s) the additional delay within TXD has to be taken into account. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

3.5.4 RXD pin

The analog bit stream received from the bus is output at pin RXD for further processing within the CAN-controller. As with pin TXD a series resistor of up to 1 kΩ can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1 Mbit/s are used. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

3.6 STB1 & STB2 pins

These input pins are mode pins and used for mode control. They are typically directly connected to an output port pin of a microcontroller.

3.7 Bus Pins CANH / CANL

The transceiver is connected to the bus via pin CANH/L. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Instead of a one-resistor termination it is highly recommended using the so-called Split Termination (for details refer to [5]). EMC measurements have shown that the Split Termination is able to improve significantly the signal symmetry between CANH and CANL, thus reducing emission. Basically each of the two termination resistors is split into two resistors of equal value, i.e. two resistors of 60Ω (or 62Ω) instead of one resistor of 120Ω. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. The recommended value for this capacitor is in the range of 4,7nF to 47nF.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: <1%).

Additionally it is recommended to load the CANH and CANL pin each with a capacitor of about 100pF close to the connector of the ECU. The main reason is to increase the robustness to automotive transients and ESD. The matching tolerance of the two capacitors should be as low as possible.

OEMs might have dedicated circuits prescribed in their specifications. Please refer to the corresponding OEM specifications for individual details.

Details about high speed CAN applications in general are explained in the NXP application hints document [5] — Rules and recommendations for in-vehicle CAN networks.

4. Appendix

4.1 Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations, when dedicated pins of the 3rd generation HS-CAN transceivers are short-circuited to supply voltages like V_{BAT}, V_{CC}, GND or to neighbored pins or simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 6.

Table 6. Classification of failure effects

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node excluded from communication
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

Table 7. TJA1059 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD1	A	Limiting value exceeded	C	TXD1 clamped recessive
(2) GNDA	C	Node is left unpowered	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD1	A	Limiting value exceeded	C	RXD1 clamped recessive; Channel 1 bus communication may be disturbed
(5) GNDB	C	Node is left unpowered	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
(6) TXD2	A	Limiting value exceeded	C	TXD2 clamped recessive
(7) RXD2	A	Limiting value exceeded	C	RXD2 clamped recessive; Channel 2 bus communication may be disturbed
(8) STB2	A	Limiting value exceeded	D	Channel 2 Normal Mode not selectable
(9) CANL2	B	No bus communication	B	Channel 2 no bus communication
(10) CANH2	D	Degration of EMC; Bit timing violation possible	D	Channel 2 degration of EMC; Bit timing violation possible
(11) V_{IO}	A	Limiting value exceeded	C	uC may be damaged, if $V_{CC} > V_{IO}$
(12) CANL1	B	No bus communication	B	Channel 1 no bus communication
(13) CANH1	D	Degration of EMC; Bit timing violation possible	D	Channel 1 degration of EMC; Bit timing violation possible
(14) STB1	A	Limiting value exceeded	D	Channel 1 Normal Mode not selectable

Table 8. TJA1059 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD1	C	TXD1 dominant clamping; Transmitter is disabled	C	TXD1 clamped recessive
(2) GNDA	-	-	C	Undervoltage detected; Both TRXs enter Off Mode and behave passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
(4) RXD1	C	RXD1 clamped dominant	C	Node may produce error frames on channel 1 until bus-off is entered
(5) GNDB	-	-	C	Undervoltage detected; Both TRX enter Off Mode and behave passive to the bus
(6) TXD2	C	TXD2 dominant clamping; Transmitter is disabled	C	TXD2 clamped recessive
(7) RXD2	C	RXD2 clamped dominant	C	Node may produce error frames on channel 2 until bus-off is entered
(8) STB2	C	Channel 2 Standby Mode not selectable	C	Channel 2 Normal Mode not selectable
(9) CANL2	D	Channel 2 degration of EMC; Bit timing violation possible	C	Channel 2 transmission not possible
(10) CANH2	B	Channel 2 no bus communication	C	Channel 2 transmission not possible
(11) V_{IO}	C	V_{IO} undervoltage detected; Both TRX enter Off Mode and behave passive to the bus	C	V_{IO} undervoltage detected; Both TRX enter Off Mode and behave passive to the bus
(12) CANL1	D	Channel 1 degration of EMC; Bit timing violation possible	C	Channel 1 transmission not possible
(13) CANH1	B	Channel 1 no bus communication	C	Channel 1 transmission not possible
(14) STB1	C	Channel 1 Standby Mode not selectable	C	Channel 1 Normal Mode not selectable

Table 9. TJA1059 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD1 - GNDA	C	Transmitter 1 disabled after TXD dominant timeout
GNDA - V_{CC}	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
V_{CC} - RXD1	C	RXD 1 clamped recessive
RXD1 - GNDB	C	RXD 1 clamped dominant
GNDB - TXD2	C	Transmitter 2 disabled after TXD dominant timeout
TXD2 - RXD2	B	Temporary channel 2 bus blocking possible; Bus 2 is released after TXD dominant timeout
STBN2 - CANL2	D	TRX 2 enters Standby Mode if the bus is recessive and enters Normal mode if the bus is driven dominant
CANL2 - CANH2	B	No bus communication on channel 2
CANH2 - V_{IO}	D	Degration of EMC; Bit timing violation possible
V_{IO} - CANL1	B	No bus communication on channel 1
CANL1 - CANH1	B	No bus communication on channel 1
CANH1 - STB1	D	TRX 1 is not able to enter Normal Mode if the bus is recessive or driven dominant

5. Abbreviations

Table 10. Abbreviations

Acronym	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (when ignition key is on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
DLC	Data Link Control
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
ESD	Electrostatic Discharge
FMEA	Failure Mode and Effects Analysis
LIN	Local Interconnect Network
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board

6. References

[1] Product data sheet TJA1059, Dual high-speed CAN transceiver with Standby Mode – NXP Semiconductors, Rev. 0.7, 2013 Jan 3

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[5] Application Hints, Rules and recommendations for in-vehicle CAN networks, TR1135 – NXP Semiconductors, Rev. 00.01, 24 September 2012

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