MC13783

Power Management and Audio Circuit User's Guide

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About This Book

This document presents information on the MC13783 power management and audio circuit device. The MC13783 is a highly integrated power management, audio and user interface component dedicated to handset and portable applications covering GSM, GPRS, EDGE and UMTS standards. This device implements high-performance audio functions suited to high-end applications, such as smartphones and UMTS handsets.

Audience

This document is intended for the:

- Hardware validation team
- Engineer software design team
- Phone product engineering team
- PMP product engineering team

Organization

This document contains the following chapters:

Chapter 1	Introduction
Chapter 2	General Description
Chapter 3	Programmability
Chapter 4	Clock Generation and Real Time Clock
Chapter 5	Power Control System
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Chapter 8	Battery Interface and Control
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Chapter 13	SPI Bitmap

Revision History

The following table summarizes changes to the technical content of this document since the previous release (Rev. 3.7).

Revision History

Location	Revision
Throughout document	Grammar, style, and formatting changes throughout for clarity and readablity, no technical content changes.

Suggested Reading

External Component Recommendations for the MC13783 Reference Design Application Note (order number AN3295)

MC13783 Buck and Boost Inductor Sizing Application Note, Document Number (order number AN3294)

Interfacing the MC13783 Power Management IC with i.MX31 Applications Processors Application Note (order number AN3276)

MC13783 Recommended Audio Output SPI Sequences Application Note (order number AN3261)

Voltage Drop Compensation on the MC13783 Switchers Line Application Note (order number AN3249)

Battery Management for the MC13783 Application Note (order number AN3155)

Definitions, Acronyms, and Abbreviations

PMIC	Power Management Integrated Circuit
ADC	Analog to Digital Converters
DAC	Digital to Analog Converter
SSI	Serial Standard Interface
SPI	Serial Peripheral Interface
RTC	Real Time Clock
GPO	General Purpose Outputs
PWM	Pulse Width Modulation
PFM	Pulse Frequency Modulation
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
ESR	Equivalent Serial Resistance

References

The following sources were referenced to produce this book:

MC13783 Detailed Technical Specification (DTS), Rev. 3.5, 10/2006, Freescale Semiconductor

Chapter 1
Introduction

The MC13783 is a highly integrated power management, audio and user interface component dedicated to handset and portable applications covering GSM, GPRS, EDGE and UMTS standards. This device implements high-performance audio functions suited to high-end applications, such as smartphones and UMTS handsets.

1.1 Features

The following features indicate the wide functionality of the MC13783:

- Battery charger interface for wall charging and USB charging
- 10-bit ADC for battery monitoring and other readout functions
- Buck switchers for direct supply of the processor cores
- Boost switcher for backlights and USB on the go supply
- Regulators with internal and external pass devices
- Transmit amplifiers for two handset microphones and a headset microphone
- Receive amplifiers for ear piece, loudspeaker, headset and line out
- 13-bit voice CODEC with dual ADC channel and both narrow and wide band sampling
- 13-bit stereo recording from an analog input source such as FM radio
- 16-bit stereo DAC supporting multiple sample rates
- Dual SSI audio bus with network mode for connection to multiple devices
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry
- Dual SPI control bus with arbitration mechanism
- Multiple backlight drivers and LED control including funlight support
- USB/RS232 transceiver with USB Carkit support
- Touchscreen interface

This document provides a detailed overview of each of these functions of the MC13783.

1.2 Block Diagram

A high level block diagram of the MC13783 is presented Figure 1-1 on page 1-2.

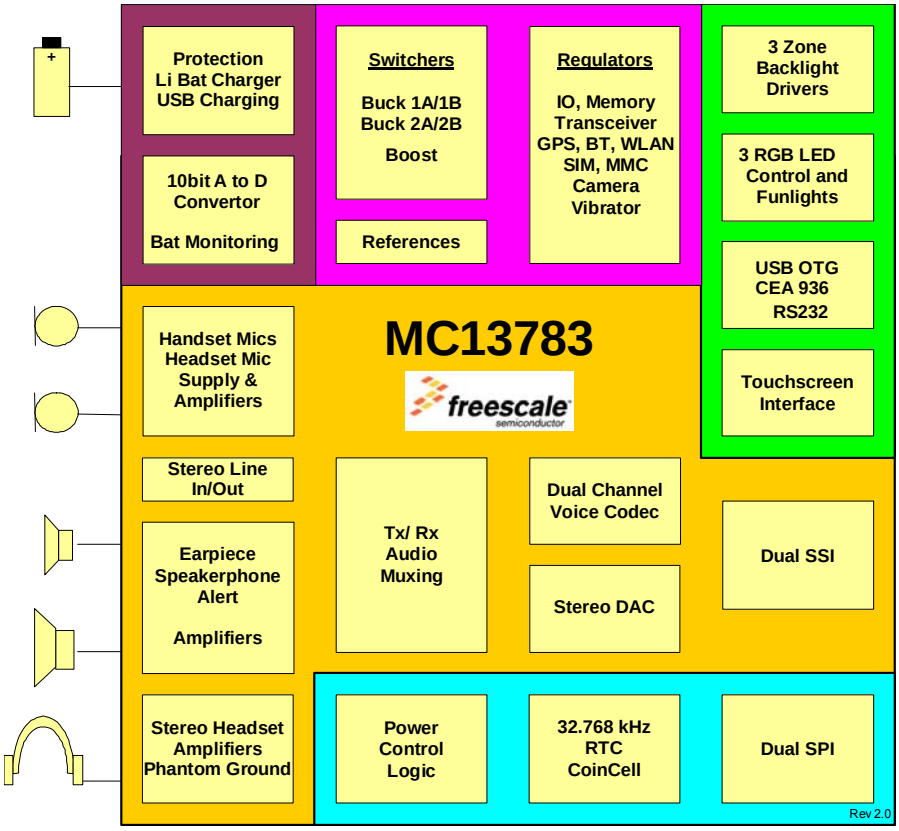


Figure 1-1. MC13783 High Level Block Diagram

Chapter 2
General Description

2.1 Detailed Block Diagram

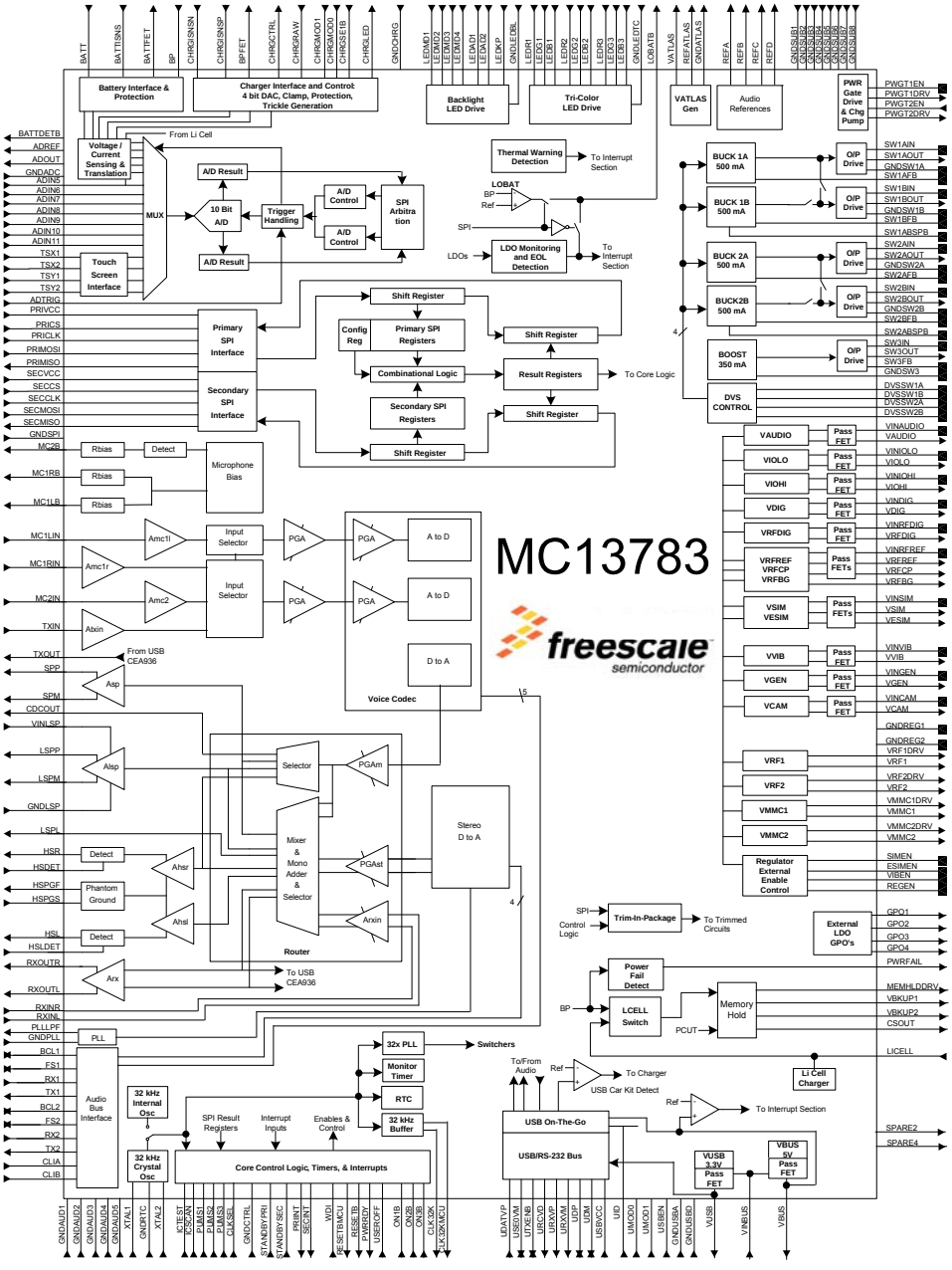


Figure 2-1. MC13783 Detailed Block Diagram

2.2 Main Functions

This section provides an overview of the primary functions of the MC13783 which are illustrated in the detailed block diagram in Figure 2-1.

2.2.1 Audio

The audio of the MC13783 is composed of microphone and speaker amplifiers, a voice CODEC, and a stereo DAC.

Three microphone amplifiers are available for amplification of two handset microphones and of the headset microphone. The feedback networks are fully integrated for a current input arrangement. A line input buffer amplifier is provided for connecting external sources. All microphones have their own stabilized supply with an integrated microphone sensitivity setting. The microphone supplies can be disabled. The headset microphone supply has a fully integrated microphone detection.

Several speaker amplifiers are provided. A bridged ear piece amplifier is available to drive an ear piece. Also a battery supplied bridged amplifier with thermal protection is included to drive a low ohmic speaker for speakerphone and alert functionality. The performance of this amplifier allows it to be used as well for ear piece drive to support applications with a single transducer combining ear piece, speakerphone and alert functionality, thus avoiding the use of multiple transducers.

A left audio out is provided which in combination with a discrete power amplifier and the integrated speaker amplifier allows for a stereo speaker application. Two single ended amplifiers are included for the stereo headset drive including headset detection. The stereo headset return path is connected to a phantom ground which avoids the use of large DC decoupling capacitors. The additional stereo receive signal outputs can be used for connection to external accessories like a car kit. Via a stereo line in, external sources such as an FM radio or standalone midi ringer can be applied to the receive path.

A voice CODEC with a dual path ADC is implemented following GSM audio requirements. Both narrow band and wide band voice is supported. The dual path ADC allows for conversion of two microphone signal sources at the same time for noise cancellation or stereo applications as well as for stereo recording from sources like FM radio. A 16bit stereo DAC is available which supports multi clock modes. An on board PLL ensures proper clock generation. The voice CODEC and the stereo DAC can be operated at the same time via two interchangeable busses supporting master and slave mode, network mode, as well as the different protocols like I2S.

Volume control is included in both transmit and receive paths. The latter also includes a balance control for stereo. The mono adder in the receive path allows for listening to a stereo source on a mono transducer. The receive paths for stereo and mono are separated to allow the two sources to be played back simultaneously on different outputs. The different sources can be analog mixed and two sources on the SSI configured in network mode can be mixed as well.

2.2.2 Switchers and Regulators

The MC13783 provides most of the telephone reference and supply voltages.

Four down converters and an up converter are included. The down, or buck, converters provide the supply to the processors and to other low voltage circuits such as I/O and memory. The four down converters can be combined into two higher power converters. Dynamic voltage scaling is provided on each of the down converters. This allows under close processor control to adapt the output voltage of the converters to minimize processor current drain. The up, or boost, converter supplies the white backlight LEDs and the regulators for the USB transceiver. The boost converter output has a backlight headroom tracking option to reduce overall power consumption.

The regulators are directly supplied from the battery or from the switchers and include supplies for I/O and peripherals, audio, camera, multi media cards, SIM cards, memory and the transceivers. Enables for external discrete regulators are included as well as a vibrator motor regulator. A dedicated preamplifier audio output is available for multifunction vibrating transducers.

Drivers for power gating with external NMOS transistors are provided including a fully integrated charge pump. This will allow to power down parts of the processor to reduce leakage current.

2.2.3 Battery Management

The MC13783 supports different charging and supply schemes including single path and serial path charging. In single path charging the phone is always supplied from the battery and therefore always has to be present and valid. In a serial path charging scheme the phone can operate directly from the charger while the battery is removed or deeply discharged.

The charger interface provides linear operation via an integrated DAC and unregulated operation like used for pulsed charging. It incorporates a standalone trickle charge mode in case of a dead battery with LED indicator driver. Over voltage, short circuit and under voltage detectors are included as well as charger detection and removal. The charger includes the necessary circuitry to allow for USB charging and for reverse supply to an external accessory. The battery management is completed by a battery presence detector and an A to D converter that serves for measuring the charge current, battery and other supply voltages as well as for measuring the battery thermistor and die temperature.

2.2.4 Logic

The MC13783 is fully programmable via SPI bus. Additional communication is provided by direct logic interfacing. Default startup of the device is selectable by hard wiring the Power Up Mode Select pins.

Both the call processor and the applications processor have full access to the MC13783 resources via two independent SPI busses. The primary SPI bus is able to allow the secondary SPI bus to control all or some of the registers. On top of this an arbitration mechanism is built in for the audio, the power and ADC functions. This together will avoid programming conflicts in case of a dual processor type of application.

The power cycling of the phone is driven by the MC13783. It has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures the supply of the memory and other circuits from the coin cell in case of brief power failures. A charger for the coin cell is included as well. Several pre-selectable power modes are provided such as SDRAM self refresh mode and user off mode.

The MC13783 provides the timekeeping based on an integrated low-power oscillator running with a standard watch crystal. This oscillator is used for internal clocking, the control logic, and as a reference for the switcher PLL. The timekeeping includes time of day, calendar and alarm. The clock is put out to the processors for reference and deep sleep mode clocking.

2.2.5 Miscellaneous Functions

The drivers and comparators for a USB On the Go and a CEA-936-A compatible USB carkit including audio routing, as well as RS232 interfaces are provided. Special precautions are taken to allow for specific booting and accessory detection modes.

Current sources are provided to drive tricolored funlights and signaling LEDs. The funlights have pre-programmed lighting patterns. The wide programmability of the tricolored LED drivers allows for applications such as audio modulation. Three backlight drivers with auto dimming are included as well for keypad and dual display backlighting.

A dedicated interface in combination with the A to D converter allow for precise resistive touch screen reading. Pen touch wake up is included.

2.3 Typical Application

Figure 2-2 gives a typical application diagram of the MC13783 together with its functional components. For details on component references and additional components such as filters please refer to the individual chapters.

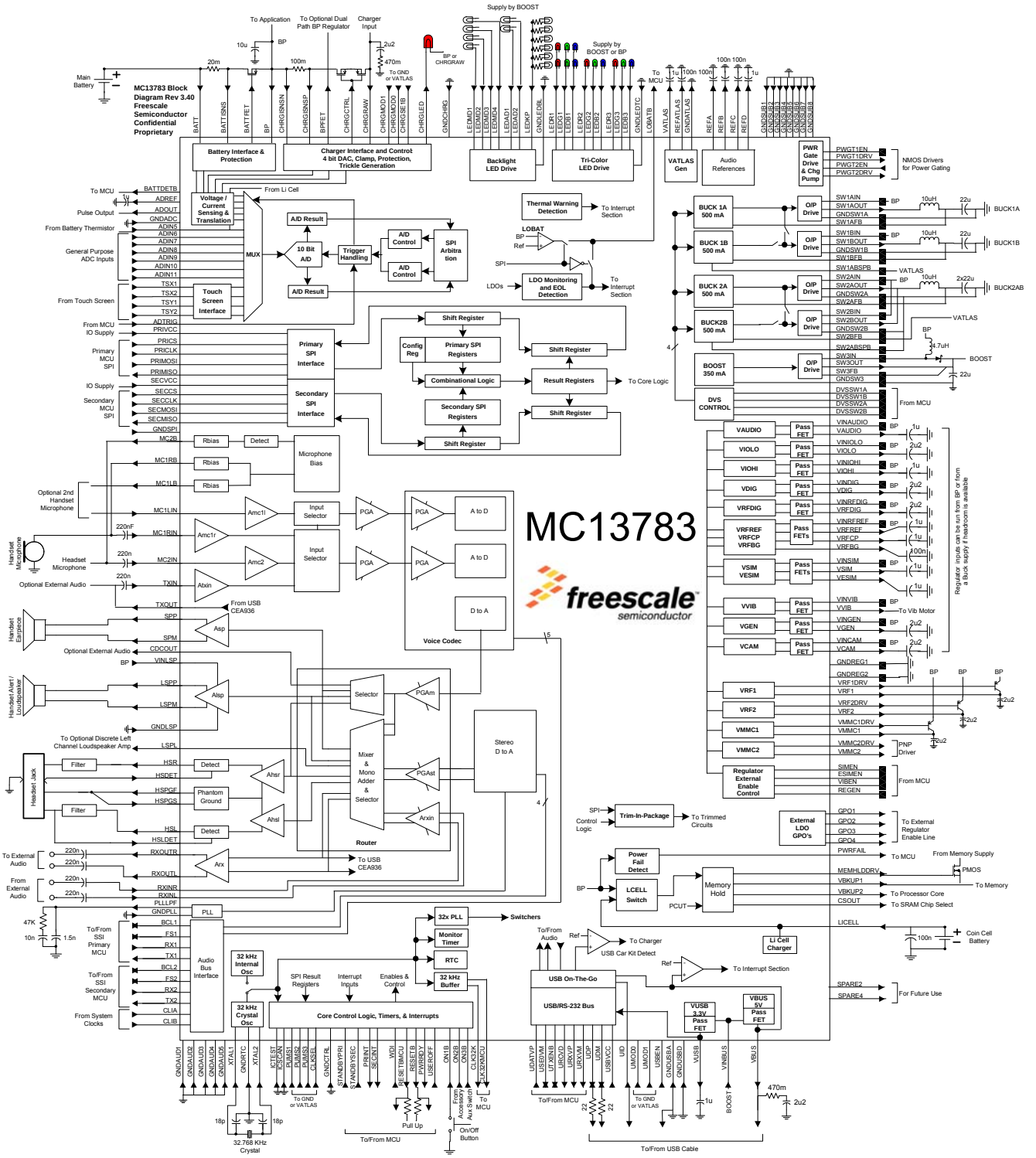


Figure 2-2. Typical Application Diagram

2.4 Maximum Ratings and Operating Input Voltage

2.4.1 Absolute Maximum Ratings

Table 2-1 gives the maximum allowed voltages, current and temperature ratings which can be applied to the IC. Exceeding these ratings can damage the circuit.

Table 2-1. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Charger Input Voltage	-0.3		+20	V
USB Input Voltage if Common to Charger	-0.3		+20	V
USB Input Voltage if Separate from Charger	-0.3		+5.50	V
Battery Voltage	-0.3		+4.65	V
Coincell Voltage	-0.3		+4.65	V
Ambient Operating Temperature Range	-30		+85	°C
Operating Junction Temperature Range	-30		+125	°C
Storage Temperature Range	-65		+150	°C
ESD Protection Human Body Model	2.0			kV

The detailed maximum voltage rating per pin can be found in the pin list which is included in chapter 12.

2.4.2 Power Dissipation

During operation, the temperature of the die must not exceed the maximum junction temperature. Depending on the operating ambient temperature and the total dissipation on the circuit this limit can be exceeded.

To optimize the thermal management scheme and avoid overheating, the MC13783 provides a thermal management system. The thermal protection uses the temperature dependency of the voltage of a forward biased junction. This junction voltage can be read out via the ADC for precise temperature readouts, Chapter 9, “ADC Subsystem”.

Internally this voltage is monitored by means of a comparator and an interrupt THWARNLI and THWARNHI will be generated when respectively crossing, in either direction, the lower and higher thermal warning thresholds. The temperature range can be determined by reading the THWARNLS and THWARNHS bits.

A thermal protection is integrated which will power off the MC13783 in case of over dissipation. This thermal protection will act above the maximum junction temperature to avoid any unwanted power downs. The protection is debounced by one period of the 32 kHz clock in order to suppress any (thermal) noise. Consider this protection as a fail-safe mechanism and therefore the phone design must not be dimensioned such that this protection is tripped under normal conditions. The temperature thresholds and the sense bit assignment are listed in Table 2-2 and Table 2-3.

Table 2-2. Thermal Protection Thresholds

Parameter	Min	Typ	Max	Units
Thermal Warning Lower Threshold (Twl)	95	100	105	°C
Thermal Warning Higher Threshold (Twh)	115	120	125	°C
Thermal Warning Hysteresis[1]	2		4	°C
Thermal Protection Threshold	130	140	150	°C

[1] Equivalent to approximately 50 mW min., 100 mW max.

Table 2-3. Thermal Warning Sense Bits

Temperature	THWARNHS	THWARNLS
T < Twl	0	0
Twl < T < Twh	0	1
Twh < T	1	1

Because the speakerphone amplifier is the only single block on the MC13783 which can consume significant power on itself, this block has an additional thermal protection, see Chapter 7, “Audio”. The thermal characteristics of the package are listed in detail in Chapter 12, “Pinout and Package”.

2.4.3 Current Consumption

The current consumption of the individual blocks is described in detail throughout this specification. For convenience, Table 2-4 is included with the main characteristics.

NOTE

The external loads are not taken into account.

Table 2-4. Summary of Current Consumption

Mode	Description	Typ	Max	Unit
RTC	All blocks disabled, no main battery attached, coincell is attached to LICELL: MC13783 core and RTC module	4	6	uA
OFF	All blocks disabled except for MC13783 core and RTC module supplied from BATT	30	45	uA
Power Cut	All blocks disabled, no main battery attached, coincell is attached and valid: MC13783 core and RTC module Trimmed references low-power 2 backup regulators Total	 5 20 10 35	 6 30 16 52	uA
User OFF	All blocks disabled except for: MC13783 core and RTC module Trimmed references low-power 2 backup regulators Total	 30 20 10 60	 45 30 16 91	uA

Table 2-4. Summary of Current Consumption (continued)

Mode	Description	Typ	Max	Unit
ON Standby	Low-power mode:			
	MC13783 core and RTC module	30	45	
	Trimmed references	40	50	
	Power gating, comparators and I/O	10	15	uA
	2 switchers in low-power mode	30	60	
	5 regulators in low-power mode including 1 with external pass device	25	50	
	Total	135	220	
ON Mode	Typical ‘power only’ use case:			
	MC13783 core and RTC module	30	45	
	Trimmed references	40	50	
	Power gating, comparators and I/O	10	15	uA
	Switcher core and 2 buck switchers In pulse skipping mode	280	500	
	10 Regulators internal pass device	200	300	
	2 Regulators external pass device	60	90	
	Total	620	1000	
ON Audio Call	ON Mode with:	0.6	1.0	
	Voice CODEC	3.0	4.0	
	Audio Bias	0.2	0.3	
	Microphone Bias, Amplifier, PGA	0.6	0.9	mA
	Receive Channel Mono	0.6	0.9	
	Ear piece Amplifier	2.3	2.8	
	Total	7.3	9.9	
ON Stereo Playback	ON Mode with:	0.6	1.0	
	Stereo DAC	6.0	7.0	
	Audio Bias	0.2	0.3	
	Receive Channel Stereo	1.2	1.8	mA
	Headset Amplifier	1.5	2.0	
	Total	9.5	12.1	

2.4.4 Operational Input Voltage Range

Table 5 provides the recommended operational input voltage range of the MC13783.

Table 5. Operational Input Voltage Range

Parameter	Minimum	Maximum	Units
Operational input voltage range (connected to BP node)	+2.6	+4.65	V

2.5 I/O Characteristics

The characteristics of the logic inputs and outputs are described in detail throughout this specification. For convenience, Table 2-6 is included with the main characteristics.

Table 2-6. Summary of I/O Characteristics

Pin Name	Internal Termination[1]	Parameter	Load Condition	Min	Max[2]	Unit
ON1B, ON2B, ON3B	Pull up[3]	Input Low Input High	47 kOhm 1 MOhm	0 0.7 * VATLAS	0.3 * VATLAS VATLAS	V
CHRGSE1B	Pull up[4]	Input Low Input High	—	0 0.7 * VATLAS	0.3 * VATLAS VATLAS	V
STANDBYPRI, STANDBYSEC, WDI[5], ADTRIG	Weak Pull Down	Input Low Input High	—	0 0.7 * VIOLO	0.3 * VIOLO 3.1	V
USEROFF	Weak Pull Down	Input Low Input High	—	0 0.7 * VBKUP1	0.3 * VBKUP1 3.1	V
LOBATB, CLK32K, PWRRDY, BATTDETB	CMOS	Output Low Output High	-100 uA 100 uA	0 VIOLO - 0.2	0.2 VIOLO	V
CLK32KMCU[6], PWRFAIL	CMOS	Output Low Output High	-100 uA 100 uA	0 VBKUP1 - 0.2	0.2 VBKUP1	V
ADOUT	CMOS	Output Low Output High	-1 mA 1 mA	0 VIOHI - 0.2	0.2 VIOHI	V
RESETB, RESETBMCU[7]	Open Drain	Output Low Output High	-2 mA Open Drain	0 0	0.4 3.1	V
DVSSW1A, DVSSW1B, DVSSW2A, DVSSW2B	Weak Pull Down	Input Low Input High	—	0 0.7 * VIOLO	0.3 * VIOLO 3.1	V
PWGT1EN, PWGT2EN	Weak Pull Down	Input Low Input High	—	0 0.7 * VIOLO	0.3 * VIOLO 3.1	V
SIMEN, ESIMEN, VIBEN, REGEN	Weak Pull Down	Input Low Input High	—	0 0.7 * VIOLO	0.3 * VIOLO 3.1	V
GPO1, GPO2, GPO3, GPO4	CMOS	Output Low Output High	-100 uA 100 uA	0 VIOHI - 0.2	0.2 VIOHI	V
PRICS, PRICLK, PRIMOSI	—	Input Low Input High	—	0 0.7 * PRIVCC	0.3 * PRIVCC PRIVCC + 0.5	V
PRIMISO, PRIINT	CMOS	Output Low Output High	-100 uA 100 uA	0 PRIVCC - 0.2	0.2 PRIVCC	V
SECCS, SECCLK, SECMOSI	—	Input Low Input High	—	0 0.7 * SECVCC	0.3 * SECVCC SECVCC + 0.5	V
SECMISO, SECINT	CMOS	Output Low Output High	-100 uA 100 uA	0 SECVCC - 0.2	0.2 SECVCC	V
BCL1, FS1, RX1	—	Input Low Input High	—	0 0.7 * PRIVCC	0.3 * PRIVCC PRIVCC + 0.5	V
BCL1, FS1, TX1	CMOS	Output Low Output High	-100 uA 100 uA	0 PRIVCC - 0.2	0.2 PRIVCC	V

Table 2-6. Summary of I/O Characteristics (continued)

Pin Name	Internal Termination[1]	Parameter	Load Condition	Min	Max[2]	Unit
BCL2, FS2, RX2	—	Input Low Input High	—	0 0.7 * SECVCC	0.3 * SECVCC SECVCC + 0.5	V
BCL2, FS2, TX2	CMOS	Output Low Output High	-100 uA 100 uA	0 SECVCC - 0.2	0.2 SECVCC	V
CLIA, CLIB	AC Coupled	Peak to peak input	—	0.3	VAUDIO + 0.3	V
UDATVP, USE0VM, UTXENB	Weak Pull Down	Input Low Input High	—	0 0.7 * USBVCC	0.3 * USBVCC 3.1	V
URXVP, URXVM, URCVD, UDATVP, USE0VM, UTXENB	CMOS	Output Low Output High	-400 uA 400 uA	0 USBVCC – 0.4	0.4 USBVCC	V
USBEN	Weak Pull Down	Input Low Input High	—	0 1.3	0.5 3.1	V
PUMS1, PUMS2, PUMS3, UMOD0	[8]	Input Low Input Mid Input High	±100 uA	0 0.45 * VATLAS 0.7 * VATLAS	0.3 * VATLAS 0.55 * VATLAS 3.1	V
SW1ABSPB, SW2ABSPB	[9] Weak Pull Down	Input Low Input High	—	0 0.7 * VATLAS	0.3 * VATLAS 3.1	V
CHRGMOD0, CHRGMOD1	[9]	Input Low Input Mid Input High	±100 uA	0 0.45 * VATLAS 0.7 * VATLAS	0.3 * VATLAS 0.55 * VATLAS 3.1	V
UMOD1	[8]	Input Low Input High	—	0 0.7 * VATLAS	0.3 * VATLAS 3.1	V
ICTEST, ICSCAN, CLKSEL	[9]	Input Low Input High	—	0 0.7 * VATLAS	0.3 * VATLAS 3.1	V
VATLAS	—	—	—	2.50	2.86	V
VAUDIO	—	—	—	2.69	2.86	V
VIOLO	—	—	—	1.15	1.86	V
VIOHI	—	—	—	2.69	2.86	V
VBKUP1	—	—	—	0.95	1.85	V
PRIVCC, SECVCC	—	—	—	1.74	3.10	V
USBVCC	—	—	—	1.74	3.10	V

1 A weak pull down represents a nominal internal pull down of 100nA unless otherwise noted.

2 The maximum must never exceed the maximum rating of the pin as given in Chapter 12, “Pinout and Package”.

3 Input has internal pull up to VATLAS equivalent to 200 kOhm.

4 Input has internal pull up to VATLAS equivalent to 100 kOhm.

5 VIOLO needs to remain enabled for proper detection of WDI High to avoid involuntary shutdown.

6 During non power cut operation the VBKUP1 regulator can be inactive while an external supply is applied to the VBKUP1 pin.

7 RESETB and RESETBMCU are open drain outputs, an external pull up is required.

8 Input state is latched in first phase of cold start.

9 Input state is not latched.

Chapter 3
Programmability

3.1 SPI Interface

The MC13783 IC contains two SPI interface ports which allow parallel access by both the call processor and the applications processor to the MC13783 register set. Via these registers the MC13783 resources can be controlled. The registers also provide status information about how the MC13783 IC is operating as well as information on external signals. The SPI interface is comprised of the signals listed in Table 3-1.

Table 3-1. SPI Interface Pin Description

SPI Interface Pin	Description
SPI Bus	
PRICLK	Primary processor clock input line, data shifting occurs at the rising edge
PRIMOSI	Primary processor serial data input line
PRIMISO	Primary processor serial data output line
PRICS	Primary processor clock enable line, active high
SECCLK	Secondary processor clock input line, data shifting occurs at the rising edge
SECMOSI	Secondary processor serial data input line
SECMISO	Secondary processor serial data output line
SECCS	Secondary processor clock enable line, active high
Interrupt	
PRIINT	Primary processor interrupt
SECINT	Secondary processor interrupt
Supply	
PRIVCC	Primary processor SPI bus supply
SECVCC	Secondary processor SPI bus supply

Both SPI ports are configured to utilize 32-bit serial data words, using 1 read/write bit, 6 address bits, 1 null bit, and 24 data bits. The SPI ports' 64 registers correspond to the 6 address bits.

3.2 Register Set

The register set is given in Table 3-2. A more detailed overview of the SPI bits, the arbitration and the register assignment is given in Chapter 13, "SPI Bitmap".

Table 3-2. Register Set

Register		Register		Register		Register	
0	Interrupt Status 0	16	Regen Assignment	32	Regulator Mode 0	48	Charger
1	Interrupt Mask 0	17	Control Spare	33	Regulator Mode 1	49	USB 0
2	Interrupt Sense 0	18	Memory A	34	Power Miscellaneous	50	Charger USB 1
3	Interrupt Status 1	19	Memory B	35	Power Spare	51	LED Control 0
4	Interrupt Mask 1	20	RTC Time	36	Audio Rx 0	52	LED Control 1
5	Interrupt Sense 1	21	RTC Alarm	37	Audio Rx 1	53	LED Control 2
6	Power Up Mode Sense	22	RTC Day	38	Audio Tx	54	LED Control 3
7	Identification	23	RTC Day Alarm	39	SSI Network	55	LED Control 4
8	Semaphore	24	Switchers 0	40	Audio CODEC	56	LED Control 5
9	Arbitration Peripheral Audio	25	Switchers 1	41	Audio Stereo DAC	57	Spare
10	Arbitration Switchers	26	Switchers 2	42	Audio Spare	58	Trim 0
11	Arbitration Regulators 0	27	Switchers 3	43	ADC 0	59	Trim 1
12	Arbitration Regulators 1	28	Switchers 4	44	ADC 1	60	Test 0
13	Power Control 0	29	Switchers 5	45	ADC 2	61	Test 1
14	Power Control 1	30	Regulator Setting 0	46	ADC 3	62	Test 2
15	Power Control 2	31	Regulator Setting 1	47	ADC 4	63	Test 3

3.3 Dual SPI Resource Sharing

3.3.1 General Description

In single processor configurations the MC13783 SPI resources do not have to be shared and access control is not required. In that case the processor has to communicate via the PRISPI bus where it has direct access to the register base. In dual processor configurations, all the MC13783 SPI resources can be shared between the primary and secondary SPI interfaces. The MC13783 provides a method for controlling the sharing of its resources so that both processors access the resources they need.

At startup, all resources, (bits or bit vectors within a SPI register) are readable and writable via the primary SPI interface while in general the secondary SPI bus has a read access only. Via the primary SPI interface, most resources can be assigned to be controlled from the secondary SPI interface.

3.3.2 Supply Arbitration

The switchers and regulators can be controlled by both SPI busses. The assignment and shared control of switchers and regulators is done via the SEL bits as indicated in Table 3-3. See Chapter 5, "Power Control System" and Chapter 6, "Supplies" for more details on the arbitration.

Table 3-3. Supply Arbitration Control

Bit	State	Description	Standby Mode Control
SWxySEL	0	Primary SPI has sole control	STANDBYPRI if SWxSTBYAND=0. Logic AND of STANDBYPRI and STANDBYSEC if SWxySTBYAND=1.
	1	Secondary SPI has sole control	STANDBYSEC if SWxSTBYAND=0. Logic AND of STANDBYPRI and STANDBYSEC if SWxySTBYAND=1.
VxSEL[1:0]	00	Primary SPI has sole control	STANDBYPRI
SW3SEL[1:0]	01	Only primary SPI can set the voltage level, both SPIs can control the operating mode	STANDBYPRI for primary SPI. STANDBYSEC for secondary SPI. The highest power mode out of the two requested by both SPIs is selected.
	10	Only secondary SPI can set the voltage level, both SPIs can control the operating mode	STANDBYPRI for primary SPI. STANDBYSEC for secondary SPI. The highest power mode out of the two requested by both SPIs is selected.
	11	Primary SPI has sole control	Logic AND of STANDBYPRI and STANDBYSEC.
GPOzSEL[1:0]	00	Primary SPI has sole control	STANDBYPRI
	01	Both SPIs can control the operating mode	STANDBYPRI for primary SPI. STANDBYSEC for secondary SPI. The highest power mode out of the two requested by both SPIs is selected.
	10	—	—
	11	Primary SPI has sole control	Logic AND of STANDBYPRI and STANDBYSEC.
PWGTnSEL	0	Primary SPI has sole control	—
PLLSEL	1	Secondary SPI has sole control	—
Note: xy Stands for all switchers (1A, 1B, 2A, and 2B), x for all regulators (IOHI, DIG, etc.), z for all GPO outputs (1, 2, 3, and 4), and n for all PWGT drivers (1 and 2).			

The VxSEL, SW3SEL, GPOzSEL and PWGTnSEL assigned registers and bits are always readable by both SPI busses independent on which bus has control. Both busses will read back the actual state of the regulator, switcher, etc. see Chapter 5, "Power Control System". This is not valid for the registers and bits determined by SWxySEL and PLLSEL. Here the SPI bus which does not have control can still write, but this will have no effect on the operation of the IC, while it will read back its own written data.

3.3.3 Audio Resource Sharing

The sharing of audio resources between the primary and secondary SPI interfaces allow both processors to, for example, enable or disable audio amplifiers or control audio gains if programmed and read back the actual state of the amplifiers. This is true for the bits assigned by AUDIOTXSEL, AUDIORXSEL and BIASSEL. The other bits are only controllable and readable by the SPI which has control. The SPI bus which does not have control can still write, but this will have no effect on the operation of the IC. The non controlling SPI will read its own written data.

Table 3-4. Audio Arbitration Control

Bits	Description	Bits Concerned
AUDIOTXSEL[1:0]	Transmit audio amplifiers assignment 00 = Primary SPI only 01 = Secondary SPI only 10 = OR-ing of both SPIs 11 = AND-ing of both SPIs	Reg 38, bits 0-13
TXGAINSEL	Transmit gain assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 38, bits 14-23
AUDIORXSEL[1:0]	Receive audio amplifiers assignment 00 = Primary SPI only 01 = Secondary SPI only 10 = OR-ing of both SPIs 11 = AND-ing of both SPIs	Reg 36, bits 3-23
RXGAINSEL	Receive gain assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 37, bits 0-21
AUDIOCDCSEL	CODEC assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 40, bits 0-20 Reg 39, bits 0-11
AUDIOSTDCSEL	Stereo DAC assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 41, bits 0-20 Reg 39, bits 12-21
BIASSEL[1:0]	Audio bias assignment 00 = Primary SPI only 01 = Secondary SPI only 10 = OR-ing of both SPIs 11 = AND-ing of both SPIs	Reg 36, bits 0-2

See Chapter 7, “Audio” for more details.

3.3.4 ADC Resource Sharing and Arbitration

The ADC convertor and its control is based on a single ADC convertor core with the possibility to store two requests and their results. There are 3 main operating modes for the arbitration control which are set via the ADCSEL[1:0] bits, see Table 3-5. These bits are located in the “Arbitration Peripheral Audio” register which is only accessible via the primary SPI. These bits are set at startup and are not to be re-configured dynamically during phone operation.

Table 3-5. ADC Arbitration Control

ADCSEL1	ADCSEL0	Arbitration Control
0	0	Primary SPI can queue a single ADC conversion request. Secondary SPI can queue a single ADC conversion request.
0	1	Primary SPI can queue two ADC conversion requests. Secondary SPI has no ADC access.
1	0	Primary SPI has no ADC access. Secondary SPI can queue two ADC conversion requests.
1	1	Will give same operating mode as for ADCSEL[1:0]=00.

See Chapter 9, "ADC Subsystem" for more details.

3.3.5 Peripheral Resource Sharing

The Charger, USB transceiver, RTC and LED drivers are by default controlled by the primary SPI but can be assigned by the primary SPI to the secondary SPI via the CHRGSEL, USBSEL, RTCSEL and the BLLEDSEL, TCLEDSEL and ADAPTSEL bits. Only the RTC registers TIME and DAY will always provide read access to both SPI busses, all other listed registers provide write and read for only one of the two SPI busses. The SPI bus which does not have control can still write, but this will have no effect on the operation of the IC. The non controlling SPI will read its own written data.

Table 3-6. Peripheral Arbitration Control

Bit	Description	Bits Concerned
RTCSEL	0 = Primary SPI has write access only, both SPIs have read access 1 = Secondary SPI has write access only, both SPIs have read access	Reg 20, 21, 22, 23
USBSEL		Reg 49 Reg 50, bits 0-8
CHRGSEL		Reg 48
BLLEDSEL		Reg 51, bits 0-9 Reg 53
TCLEDSEL		Reg 51, bits 17-23 Reg 52, 54, 55, 56
ADAPTSEL		Reg 51, bits 10-16

3.3.6 Semaphore Bits

The MC13783 provides a semaphore register through which the processors can communicate with each other via their respective SPI busses without using the inter processor communication bus. An interrupt mechanism is added to this to allow for selective interrupts based on the contents of the semaphore register.

The semaphore registers for the primary and secondary SPI are set up according to Table 3-7.

Table 3-7. Semaphore Bits

Primary SPI	Secondary SPI	Description
SEM1CTRLA	SEM2CTRLA	Control bit for semaphore word A
SEM1CTRLB	SEM2CTRLB	Control bit for semaphore word B
SEM1WRTA[3:0]	SEM2WRTA[3:0]	Writable semaphore word A
SEM1WRTB[5:0]	SEM2WRTB[5:0]	Writable semaphore word B
SEM2RDA[3:0]	SEM1RDA[3:0]	Readable semaphore word A of the other SPI
SEM2RDB[5:0]	SEM1RDB[5:0]	Readable semaphore word B of the other SPI

Via each SPI a processor can write to the SEMxWRTy semaphore words while it can read on its own SPI bus via the SEMxRDy words the contents of the semaphore words as written by the other SPI to its SEMxWRTy words. An interrupt bit SEMAFI is set and the processor is interrupted based on the comparison of the data in the semaphore words. The comparison mechanism is set via the SEMxCTRLy bits. If the SEMAFM bit is set, the interrupt is not generated. There is no semaphore sense bit.

There are two modes of comparison possible via the SEMxCTRLy bit setting. If set to 0 then the contents of words are compared and an interrupt is generated when both words become identical or if they were identical but become different. If set to 1 then a mask is applied for a bit to bit comparison and an interrupt is generated when one of the bits change state. The comparison modes for the A and B words can be set the same or differently.

Word comparison example: Suppose the processor at the secondary SPI writes to SEM2WRTA[3:0] its internal state during startup. Starting from 0000 it goes up to 1011. When reaching an intermediate state 0111 the primary processor has to take a specific action so that the secondary processor can continue its startup procedure. To do so, the processor at the primary SPI sets SEM1CTRLA=0 and programs the comparison word to SEM1WRTA[3:0]=0111. At the moment the secondary SPI writes SEM2WRTA[3:0]=0111 an interrupt is generated. The primary SPI can read SEM2RDA[3:0] to verify this is true and take the specific action.

Bit comparison example: Suppose the processor at the secondary SPI needs to know if one out of five shared resources is being used by the other processor and cannot go through the inter processor communication bus for that. To do so, the processor at the secondary SPI sets SEM2CTRLB=1 and programs the comparison word to SEM2WRTB[5:0]=011111, with SEM2WRTB0 stands for the resource one, SEM2WRTB1 for resource two, etc. At the moment the processor at the primary SPI starts using resource 3, resource 4 was already in use, it writes SEM1WRTB[5:0]=001100, and an interrupt is generated to the other processor. If it frees up resource three it can program SEM1WRTB[5:0]=001000 which again will generate an interrupt.

When starting from default but with the SEMAFM bit cleared, any change to the semaphore register by one SPI will result in an interrupt to the other SPI because by default the word comparison is active.

3.4 Interrupt Handling

3.4.1 Control

The MC13783 has interrupt generation capability to inform the system on important events occurring. Interrupts are handled independently for both SPI busses. An interrupt is signaled to the processors connected to the primary SPI and the secondary SPI by driving the PRIINT respectively the SECINT line high.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain active until cleared. Each interrupt can be cleared by a SPI bus by writing a 1 to the appropriate bit in the Interrupt Status register, this will also cause the interrupt line to go low for that SPI bus. If a new interrupt occurs while the processor clears an existing interrupt bit, the interrupt line will remain high. Clearing an interrupt bit on one SPI bus will not clear the interrupt bit on the other SPI bus.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when the interrupt bit goes high, the interrupt line will not go high. However, even when the interrupt is masked, the interrupt source can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the MC13783. The MC13783 powers up with all interrupts masked, so the processor must initially poll the MC13783 to determine if any interrupts are active. Alternatively, the processor can later unmask the interrupt bits of interest. If the related interrupt bit was already high, the interrupt line will go high after the unmasking. All mask bits labeled as reserved in the SPI bitmap do default to a 1 and must not be programmed to 0. Each SPI bus has its own independent set of mask bits.

The MC13783 sense registers contain status and input sense bits. These bits provide information to the processor about specific MC13783 I/O, power on inputs and power up sources. They only represent the current status of the sources, and thus are not latched, and are not clearable. The values in this register are read only. The contents of the primary SPI and secondary SPI status registers are strictly identical.

3.4.2 Bit Summary

Table 3-8 summarizes all interrupt, mask and sense bits. Although the polarity of the sense bits is given, for the accurate behavior of the sense bits the related chapter has to be consulted. For the applied debounce timing per interrupt, see the related chapters.

Table 3-8. Interrupt, Mask and Sense Bits

Interrupt	Mask	Sense	Used for / Sense Bit Polarity	Trigger	Chapter
ADCDONEI	ADCDONEM	—	ADC has finished requested conversions	L2H	9
ADCBISDONEI	ADCBISDONEM	—	ADCBIS has finished requested conversions	L2H	9
TSI	TSM	—	Touchscreen wake up	Dual	9
WHIGHI	WHIGHM	—	ADC reading above high limit	L2H	9
WLOWI	WLOWM	—	ADC reading below low limit	L2H	9
CHGDETI	CHGDETM	CHGDETS	Charger attach and removal Sense is 1 if above threshold	Dual	8

Table 3-8. Interrupt, Mask and Sense Bits (continued)

Interrupt	Mask	Sense	Used for / Sense Bit Polarity	Trigger	Chapter
CHGOVI	CHGOVM	CHGOVS	Charger over voltage detection Sense is 1 if above threshold	Dual	8
CHGREVI	CHGREVM	CHGREVS	Charger path reverse current Sense is 1 if current flows into phone	L2H	8
CHGSHORTI	CHGSHORTM	CHGSHORTS	Charger path short circuit Sense is 1 if above threshold	L2H	8
CCCVI	CCCVM	CCCVS	Charger regulator operating mode Sense is 1 if voltage regulation	Dual	8
CHGCURRI	CHGCURRM	CHGCURRS	Charge current below threshold Sense is 1 if above threshold	H2L	8
BPONI	BPONM	BPONS	BP turn on threshold detection Sense is 1 if above threshold	L2H	5
—	—	—	End of life / low battery detect	—	5
LOBATLI	LOBATLM	LOBATLS	Sense is 1 if end of life detected	L2H	—
—	—	—	Sense is 1 if below low battery threshold	—	—
LOBATHI	LOBATHM	LOBATHS	Low battery warning Sense is 1 if above threshold	Dual	5
USBI	USBM	USB4V4S	USB 4V4 detect Sense is 1 if above threshold	Dual	10
—	—	USB2V0S	USB 2V0 detect Sense is 1 if above threshold	Dual	10
—	—	USB0V8S	USB 0V8 detect Sense is 1 if above threshold	Dual	10
UDPI	UDPM	UDPS	UDP detect Sense is 1 if pin is high	L2H	10
UDMI	UDMM	UDMS	UDM detect Sense is 1 if pin is high	L2H	10
IDI	IDM	IDFLOATS	USB ID Line detect Sense bits are coded, see related chapter	Dual	10
—	—	IDGNDS	—	—	—
SE1I	SE1M	SE1S	Single ended 1 detect Sense is 1 if detected	Dual	10
CKDETI	CKDETM	CKDETS	Carkit detect Sense is 1 if detected	L2H	10
MC2BI	MC2BM	MC2BS	Microphone bias 2 detect Sense is 1 if detected	Dual	7
HSDETI	HSDETM	HSDETS	Headset attach Sense is 1 if attached	Dual	7
HSLI	HSLM	HSLS	Stereo headset detect Sense is 1 if detected	L2H	7

Table 3-8. Interrupt, Mask and Sense Bits (continued)

Interrupt	Mask	Sense	Used for / Sense Bit Polarity	Trigger	Chapter
ALSPTHI	ALSPTHM	ALSPTHS	Thermal shutdown Alsp Sense is 1 if above threshold	L2H	7
AHSSHORTI	AHSSHORTM	AHSSHORTS	Short circuit on Ahs outputs Sense is 1 if detected	L2H	7
1HZI	1HZM	—	1 Hz timetick	L2H	4
TODAI	TODAM	—	Time of day alarm	L2H	4
ONOFD1I	ONOFD1M	ONOFD1S	ON1B event Sense is 1 if pin is high	Dual	5
ONOFD2I	ONOFD2M	ONOFD2S	ON2B event Sense is 1 if pin is high	Dual	5
ONOFD3I	ONOFD3M	ONOFD3S	ON3B event Sense is 1 if pin is high	Dual	5
SYSRSTI	SYSRSTM	—	System reset	L2H	5
PWRRDYI	PWRRDYM	PWRRDYS	Power ready Sense is 1 if detected	L2H	5
THWARNHI	THWARNHM	THWARNHS	Thermal warning higher threshold Sense is 1 if above threshold	Dual	2
THWARNLI	THWARNLM	THWARNLS	Thermal warning lower threshold Sense is 1 if above threshold	Dual	2
PCI	PCM	—	Power cut event	L2H	5
WARMI	WARMM	—	Warm start event	L2H	5
MEMHLDI	MEMHLDM	—	Memory hold event	L2H	5
CLKI	CLKM	CLKS	Clock source change Sense is 1 if source is XTAL	Dual	4
SEMAFI	SEMAFM	—	Semaphore	Dual	3
RTCRSTI	RTCRSTM	—	RTC reset occurred	L2H	4

Additional sense bits are available in the power up mode sense register. Via these bits the state of the power up mode selection pins for the regulators, charger and USB can be read out. Table 3-9 provides a summary.

Table 3-9. Additional Sense Bits

Sense	Description	Chapter
ICTESTS	0 = ICTEST low 1 = ICTEST high	3
CHRGMOD0S[1:0]	00 = CHRGMOD0 low 01 = CHRGMOD0 open 10 = Not available 11 = CHRGMOD0 high	8

Table 3-9. Additional Sense Bits (continued)

Sense	Description	Chapter
CHRGMOD1S[1:0]	00 = CHRGMOD1 low 01 = CHRGMOD1 open 10 = Not available 11 = CHRGMOD1 high	8
UMODS[1:0]	00 = UMOD0 low, UMOD1 = low 01 = UMOD0 open, UMOD1= low 10 = UMOD0 don't care, UMOD1 = high 11 = UMOD0 high, UMOD1 = low	10
USBEN	0 = USBEN low 1 = USBEN high	10
SW1ABS	0 = SW1A and SW1B independent operation 1 = SW1A and SW1B joined operation	6
SW2ABS	0 = SW2A and SW2B independent operation 1 = SW2A and SW2B joined operation	6
PUMS1S[1:0] PUMS2S[1:0] PUMS3S[1:0]	00 = PUMS1/PUMS2/PUMS3 low 01 = PUMS1/PUMS2/PUMS3 open 10 = Not available 11 = PUMS1/PUMS2/PUMS3 high	5

3.5 Interface Requirements

3.5.1 SPI Interface Description

The operation of both SPI interfaces is equivalent. Therefore, all SPI bus names without prefix PRI or SEC correspond to both the PRISPI and SECSPI interfaces.

The control bits are organized into 64 fields. Each of these 64 fields contains 32 bits. A maximum of 24 data bits is used per field. In addition, there is one *dead* bit between the data and address fields. The remaining bits include 6 address bits to address the 64 data fields and one write enable bit to select whether the SPI transaction is a read or a write.

For each SPI transfer, first a one is written to the read/write bit if this SPI transfer is to be a write. A zero is written to the read/write bit if this is to be a read command only. If a zero is written, then any data sent after the address bits are ignored and the internal contents of the field addressed do not change when the 32nd CLK is sent. Next the 6-bit address is written, MSB first. Finally, data bits are written, MSB first. Once all the data bits are written then the data is transferred into the actual registers on the falling edge of the 32nd CLK.

The default CS polarity is active high. A metal option is available to be able to change the CS polarity from an active high to an active low. The CS line must remain active during the entire SPI transfer. In case the CS line goes inactive during a SPI transfer all data is ignored. To start a new SPI transfer, the CS line must go inactive and then go active again. The MISO line will be tri-stated while CS is low.

NOTE

Not all bits are truly writeable. Refer to the individual sub-circuit descriptions to determine the read/write capability of each bit.

All unused SPI bits in each register must be written to a zero. SPI readbacks of the address field and unused bits are returned as zero. To read a field of data, the MISO pin will output the data field pointed to by the 6 address bits loaded at the beginning of the SPI sequence.

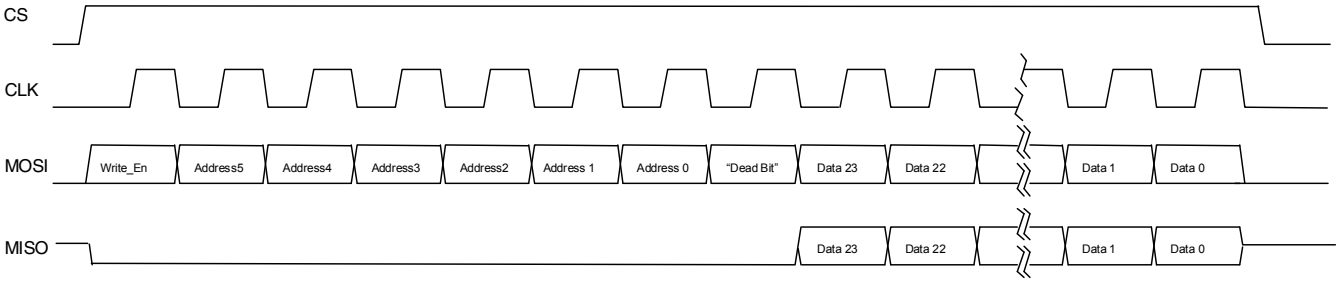


Figure 3-1. SPI Transfer Protocol Single Read/Write Access

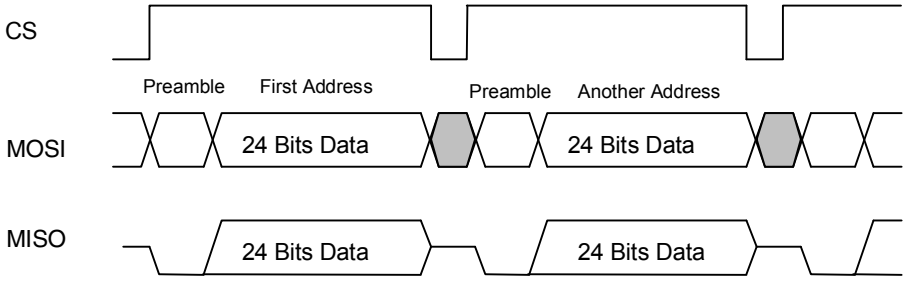


Figure 3-2. SPI Transfer Protocol Multiple Read/Write Access

3.5.2 SPI Requirements

The requirements for both SPI interfaces are equivalent. Therefore, all SPI bus names without prefix PRI or SEC correspond to both SPI interfaces. Figure 3-3 and Table 3-10 summarize the SPI electrical and timing requirements. The SPI input and output levels are set independently via the PRIVCC and SECVCC pins by connecting those to the proper supply.

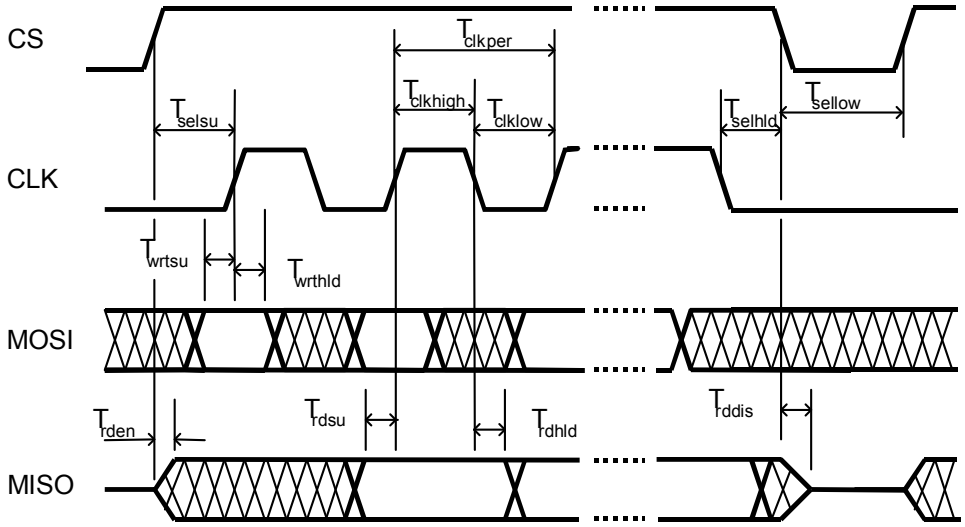


Figure 3-3. SPI Interface Timing Diagram

Table 3-10. SPI Interface Timing Specifications

Parameter	Description	T Min (ns)
T_{selsu}	Time CS has to be high before the first rising edge of CLK	20
T_{selhld}	Time CS has to remain high after the last falling edge of CLK	20
T_{sellow}	Time CS has to remain low between two transfers	20
T_{clkper}	Clock period of CLK[1]	50
$T_{clkhigh}$	Part of the clock period where CLK has to remain high	20
T_{clklow}	Part of the clock period where CLK has to remain low	20
T_{wrtsu}	Time MOSI has to be stable before the next rising edge of CLK	5
T_{wrthld}	Time MOSI has to remain stable after the rising edge of CLK	5
T_{rdsu}	Time MISO will be stable before the next rising edge of CLK	5
T_{rdhld}	Time MISO will remain stable after the falling edge of CLK	5
T_{rden}	Time MISO needs to become active after the rising edge of CS	5
T_{rddis}	Time MISO needs to become inactive after the falling edge of CS	5

1 Equivalent to a maximum clock frequency of 20 MHz.

Table 3-11. SPI Interface Logic I/O Specifications

Parameter	Condition	Min	Max	Units
Input High CS, MOSI, CLK	—	0.7*VCC	VCC+0.5 < 3.10	V
Input Low CS, MOSI, CLK	—	0	0.3*VCC	V
Output Low MISO, INT	Output sink 100 uA	0	0.2	V
Output High MISO, INT	Output source 100 uA	VCC-0.2	VCC	V
VCC Operating Range	—	1.74	3.10	V
Note: VCC refers to PRIVCC and SECVCC respectively.				

3.6 Test Modes

3.6.1 Identification

The MC13783 parts can be identified by version and revision number.

The revision of the MC13783 is tracked with the revision identification bits REV[4:0]. The bits REV[4:3] track the full mask set revision, where bits REV[2:0] track the metal revisions. These bits are hard wired.

Table 3-12. IC Revision Bit Assignment

Bits REV[4:0]	IC Revision
01000	Pass 1.0
01001	Pass 1.1
01010	Pass 1.2

Table 3-12. IC Revision Bit Assignment (continued)

Bits REV[4:0]	IC Revision
10000	Pass 2.0
10001	Pass 2.1
11000	Pass 3.0
11001	Pass 3.1
11010	Pass 3.2
00010	Pass 3.2A
11011	Pass 3.3
11100	Pass 3.4
11101	Pass 3.5

The version of the MC13783 can be identified by the ICID[2:0] bits. This is used to distinguish future derivatives or customizations from the MC13783. For the MC13783 the bits are set to ICID[2:0]=010 and are located in the revision register. A duplicate of the ICID[2:0] bits is located in register 46. These bits are hard wired.

The bits FIN[3:0] are used during development and are not to be explored by the application.

The MC13783 die is produced using different wafer fabs. The fabs can be identified via the FAB[1:0] bits. These bits are hard wired.

3.6.2 Test Mode Registers

During evaluation and testing, several modules are configured in specific modes via the test mode bits and are accessible only when ICTEST is pulled high. In the application, ICTEST is to be tied to the system ground. The same is valid for the ICSCAN pin.

Chapter 4
Clock Generation and Real Time Clock

4.1 Clock Generation

The MC13783 generates a 32.768 kHz clock as well as several 32.768 kHz derivative clocks that are used internally for control. In addition, a 32.768 kHz square wave is output to external pins.

4.1.1 Clocking Scheme

The MC13783 contains an internal RC oscillator powered from VATLAS that delivers a 32kHz nominal frequency (20%) at its output when an external 32.768 kHz crystal is not present. The RC oscillator will then be used to run the debounce logic, the PLL for the switchers, the real time clock (RTC) and internal control logic.

If a 32.768 kHz crystal is present and running, then all control functions will run off the crystal derived 32 kHz oscillator. The 32 kHz crystal will be output through a buffer at VIOLO to the external pin CLK32K. A second output CLK32KMCU dedicated to the processor runs at VBKUP1 and can be maintained active during user off mode if desired, see Chapter 5, “Power Control System”. If not active, the clock output is active low. The VBKUP1 regulator does not have to be active to have the CLK32KMCU output active as long as on the phone PCB the output of an other regulator is connected to VBKUP1. The crystal oscillator itself is supplied by VATLAS and, in absence of the main battery, from LICELL.

If the CLKSEL pin is connected to VATLAS, the output of the internal RC oscillator will not be routed to the clock output pins under any circumstances. If the CLKSEL pin is grounded, however, the internal RC oscillator output will be routed to clock output pins when the external crystal 32 kHz oscillator is not running.

A status bit, CLKS, is available to indicate to the processor which clock is currently selected: CLKS=0 when the internal RC is used, and CLKS=1 if the XTAL source is used. An interrupt CLKI can also be generated whenever a change in clock source occurs if the corresponding CLKM mask bit is not set.

4.1.2 Oscillator Specifications

The crystal oscillator has been designed for use in conjunction with the Micro Crystal CC5V-T1-32.768kHz-9pF-30 ppm.

Table 4-1. RTC Crystal Specifications

Description	Measurement
Nominal Frequency	32.768 kHz
Make Tolerance	+/- 30 ppm

Table 4-1. RTC Crystal Specifications (continued)

Description	Measurement
Temperature Stability	-0.038 ppm /C^2
Series Resistance	80 kOhms
Maximum Drive Level	1 uW
Operating Drive Level	0.25 to 0.5 uW
Nominal Load Capacitance	9 pF
Pin-to-pin Capacitance	1.3 pF
Aging	3 ppm/year

The electrical characteristics of the 32 kHz crystal oscillator are given in Table 4-2, taking into account the above crystal characteristics.

Table 4-2. Crystal Oscillator Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage	Oscillator and RTC Block from LICELL	RTCUVDET	—	3.5	V
RTC Under voltage Detection RTCUVDET	—	—	—	1.5	V
RTC Low Battery Detection RTCLOBATDET	—	1.75	—	1.85	V
Operating Current ON mode	LICELL=2V, T=25C, incl. RTC Block	—	4.0	—	uA
Operating Current OFF mode	incl. RTC Block	—	4.0	6.0	uA
RTC oscillator startup time	Upon application of power	—	—	1	s
RTCX1 Input Voltage Swing	External signal source, capacitor coupled	500	—	—	mV
RTCX1 Input Duty Cycle Range	External signal source	45	—	55	%
Total Frequency Stability	Sum of IC (including the crystal and external capacitance) as well as manufacturing and temperature	-100	—	+100	ppm
Output Low CLK32K	Output sink 100 uA	0	—	0.2	V
Output High CLK32K	Output source 100 uA	VIOLO-0.2	—	VIOLO	V
Output Low CLK32KMCU	Output sink 100 uA	0	—	0.2	V
Output High CLK32KMCU	Output source 100 uA	VBKUP1-0.2	—	VBKUP1	V
CLK32K, CLK32KMCU Output Rise Time	Load Capacitance 50 pF	—	—	100	ns
CLK32K, CLK32KMCU Output Fall Time	Load Capacitance 50 pF	—	—	100	ns
CLK32K, CLK32KMCU Output Duty Cycle	Crystal on XTAL1, XTAL2 pins	45	—	55	%

Table 4-2. Crystal Oscillator Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
CLK32K, CLK32KMCU Output Duty Cycle	External signal source Relative to XTAL1 Input Duty Cycle	-10	—	+10	%
Peak Output Jitter	MC13783 in ON mode	—	—	100	ns pp
RMS Output Jitter	MC13783 in ON mode	—	—	30	ns rms

4.1.3 Oscillator Application Guidelines

The following guidelines may prove to be helpful in providing a crystal oscillator that starts reliably and runs with minimal jitter.

- PCB leakage: The RTC amplifier is a low current circuit; therefore, PCB leakage may significantly change the operating point of the amplifier and even the drive level to the crystal. (Changing the drive level to the crystal may change the aging rate, jitter, and even the frequency at a given load capacitance.) The traces must be kept as short as possible to minimize the leakage and good PCB manufacturing processes must be maintained.
- Layout: The traces from the MC13783 to the crystal and load capacitance and the RTC Ground are sensitive. They must be kept as short as possible with minimal coupling to other signals. The signal ground for the RTC is to be connected to GNDRTC and, via a single connection, GNDRTC to the system ground. The CLK32K and CLK32KMCU square wave outputs must be kept away from the crystal / load capacitor leads as the sharp edges can couple into the circuit and lead to excessive jitter. The crystal / load capacitance leads and the RTC Ground must form a minimal loop area.
- Crystal Choice: Generally speaking, crystal's are not interchangeable between manufacturers, or even different packages for a given manufacturer. If a different crystal is considered, it must be fully characterized with the MC13783 before it can be considered.
- Tuning Capacitors: The nominal load capacitance is 9 pF, therefore the total capacitance at each node must be 18 pF, composed out of the load capacitance, the effective input capacitance at each pin plus the PCB stray capacitance for each pin.

4.2 Real Time Clock

4.2.1 Time and Day Counters

The real time clock runs from the 32 kHz clock, either the RC oscillator or the crystal oscillator if a crystal is present. This clock is divided down to a 1Hz time tick which drives a 17 bit time of day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399 and will then roll over to 0. When the roll over occurs, it increments the 15 bit DAY counter. The DAY counter can count up to 32767 days. The 1 Hz timetick can be used to generate an 1HZI interrupt. The 1HZI can be masked with corresponding 1HZM mask bit.

If the TOD and DAY registers are read at a point in time in which DAY is incremented, then care must be taken that, if DAY is read first, DAY has not changed before reading TOD. The following sequence of events can occur.

1. Software reads a value of DAY
2. The DAY counter increments (by definition, the TOD register also increments)
3. Software then reads the value of TOD

In this case, the value that is read from the TOD register is not valid for the value of DAY just read. In order to guarantee stable TOD and DAY data, all SPI reads and writes to TOD and DAY data must happen immediately after the 1HZI interrupt occurs. Alternatively, TOD or DAY readbacks can be double-read and then compared to verify that they haven't changed.

4.2.2 Time of Day Alarm

A Time of Day (TOD) alarm function can be used to turn on the phone and alert the processor. If the phone is already on, the processor will be interrupted. The TODA and DAYA registers are used to set the alarm time. When the TOD counter is equal to the value in TODA and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

At initial power up of the phone (application of the coin cell) the state of TODA and DAYA registers will be all 1's. The interrupt for the alarm (TODAI) is backed up by LICELL and will be valid at power up. If the mask bit for the TOD alarm (TODAM) is high, then the TODAI interrupt is masked and the phone will not turn on upon the time of day alarm event (TOD[16:0] = TODA[16:0] and DAY[14:0] = DAYA[14:0]). Alternatively, to avoid the phone turns on while no alarm is set, the TODA[16:0] can be set to all 1's.

By default, the TODAM mask bit is set to 1, thus masking the interrupt and turn on event. This is valid for both the primary and the secondary SPI. Internally, the TODAM bits of both SPI busses are logically AND-ed so both bits will have to be set to a 1 to mask the turn on event. If one of the SPI busses sets its TODAM bit to a 0, the turn on event is no longer prevented. Note that an interrupt is generated only to the SPI which has set TODAM to a 0.

On the MC13783, the TOD count must equal the TODA value and the DAY count must equal the DAYA value for an interrupt to be generated. This does mean that there will always be some microcontroller intervention to schedule a regular daily event, but it is only to increment the DAYA value. So, the MC13783 does make it convenient to schedule multiple daily events, where a single list can be used, or to skip any number of days.

4.2.3 Timer Reset

As long as the supply at BP is valid, the real time clock will be supplied from VATLAS. If not, it can be backed up from a coincell via the LICELL pin. When the backup voltage drops below the real time clock operating range, the RTCUVDET is tripped and the contents of the RTC will be reset by the RTCPORB reset signal. To inform the processor that the contents of the RTC are no longer valid due to the reset, a timer reset interrupt function is implemented via the RTCRSTI bit. The RTCRSTI bit defaults to a 1 when a RTCPORB reset occurs and can only be cleared by SPI programming.

At very first phone power up, the interrupt bit RTCRSTI will be set. The processor now has to program the RTC data, after the phone user has entered the date and time information, and then clear the RTCRSTI bit by writing a 1 to it. As long as no RTC reset occurs no new RTSRSTI interrupt will be generated. Only when a RTC reset occurs, and at the next phone power up, for instance after a valid battery is applied, an interrupt is again generated. Because the RTC contents are not relevant when running on the internal RC clock, the RTCRSTI will remain a logic 0 in applications without an external crystal or where no external clock is applied at RTCX1 input.

4.3 RTC Control Register Summary

Table 4-3. RTC Time Register

Name	Bit #	R/W	Reset Signal	Reset State	Description
TOD0	0	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD1	1	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD2	2	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD3	3	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD4	4	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD5	5	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD6	6	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD7	7	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD8	8	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD9	9	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD10	10	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD11	11	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD12	12	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD13	13	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD14	14	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD15	15	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
TOD16	16	R/W	RTCPORB	0	Contains the value of the Time-of-day (TOD) Counter
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available

Table 4-3. RTC Time Register (continued)

Name	Bit #	R/W	Reset Signal	Reset State	Description
Unused	23	R	—	0	Not available
Unused	24	R	—	0	Not available

Table 4-4. RTC Alarm Register

Name	Bit #	R/W	Reset Signal	Reset State	Description
TODA0	0	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA1	1	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA2	2	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA3	3	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA4	4	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA5	5	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA6	6	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA7	7	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA8	8	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA9	9	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA10	10	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA11	11	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA12	12	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA13	13	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA14	14	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA15	15	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
TODA16	16	R/W	RTCPORB	1	Contains the value of the Time-of-day Alarm (TODA)
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available
Unused	24	R	—	0	Not available

Table 4-5. RTC Day Register

Name	Bit #	R/W	Reset Signal	Reset State	Description
DAY0	0	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY1	1	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY2	2	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY3	3	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY4	4	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY5	5	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY6	6	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY7	7	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY8	8	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY9	9	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY10	10	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY11	11	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY12	12	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY13	13	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
DAY14	14	R/W	RTCPORB	0	Contains the value of the Day (DAY) Counter
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available
Unused	24	R	—	0	Not available

Table 4-6. RTC Day Alarm Register

Name	Bit #	R/W	Reset Signal	Reset State	Description
DAYA0	0	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA1	1	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA2	2	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA3	3	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter

Table 4-6. RTC Day Alarm Register (continued)

Name	Bit #	R/W	Reset Signal	Reset State	Description
DAYA4	4	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA5	5	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA6	6	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA7	7	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA8	8	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA9	9	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA10	10	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA11	11	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA12	12	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA13	13	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
DAYA14	14	R/W	RTCPORB	1	Contains the value of the Day Alarm (DAYA) Counter
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available
Unused	24	R	—	0	Not available

Chapter 5
Power Control System

5.1 Interface

The power control system on the MC13783 interfaces with the processors via different I/O signals and the SPI bus. It also uses on-chip signals and detector outputs. Table 5-1 gives a listing of the principle elements of this interface.

Table 5-1. Power Control System Interface Signals

Name	Type of Signal	Function
ON1B	Input pin	Connection for a power on/off button
ON2B	Input pin	Connection for an accessory power on/off button
ON3B	Input pin	Connection for a third power on/off button
WDI	Input pin	Watchdog input has to be kept high by the processor to keep the MC13783 active
RESETB	Output pin	Reset Bar output (active low) to the application. Open drain output.
RESETBMCU	Output pin	Reset Bar output (active low) to the processor core. Open drain output.
PWRFAIL	Output pin	Power fail signal indicates if an under voltage condition occurs
LOBATB	Output pin	Low battery detection signal, goes low when a low BP condition occurs
USEROFF	Input pin	Signal from processor to confirm user off mode after a power fail
STANDBYPRI	Input pin	Signal from primary processor to put the MC13783 in a low-power mode
STANBYPRIINV	SPI bit	If set then STANDBYPRI is interpreted as active low
STANDBYSEC	Input pin	Signal from secondary processor to put the MC13783 in a low-power mode
STANDBYSECINV	SPI bit	If set then STANDBYSEC is interpreted as active low
UVDET	Detector	Under voltage detector output
LOBATDET	Detector	Low battery detector output
RTCUVDET	Detector	RTC under voltage detector output
RTCLOBATDET	Detector	RTC low battery detector output
CHGDET	Detector	Charger presence detector output
USBDET	Detector	USB presence detector output
BPONI	SPI bit	BP Turn on threshold interrupt
LOBATHI	SPI bit	Low battery (BP) warning
LOBATLI	SPI bit	Low battery (BP) turn off

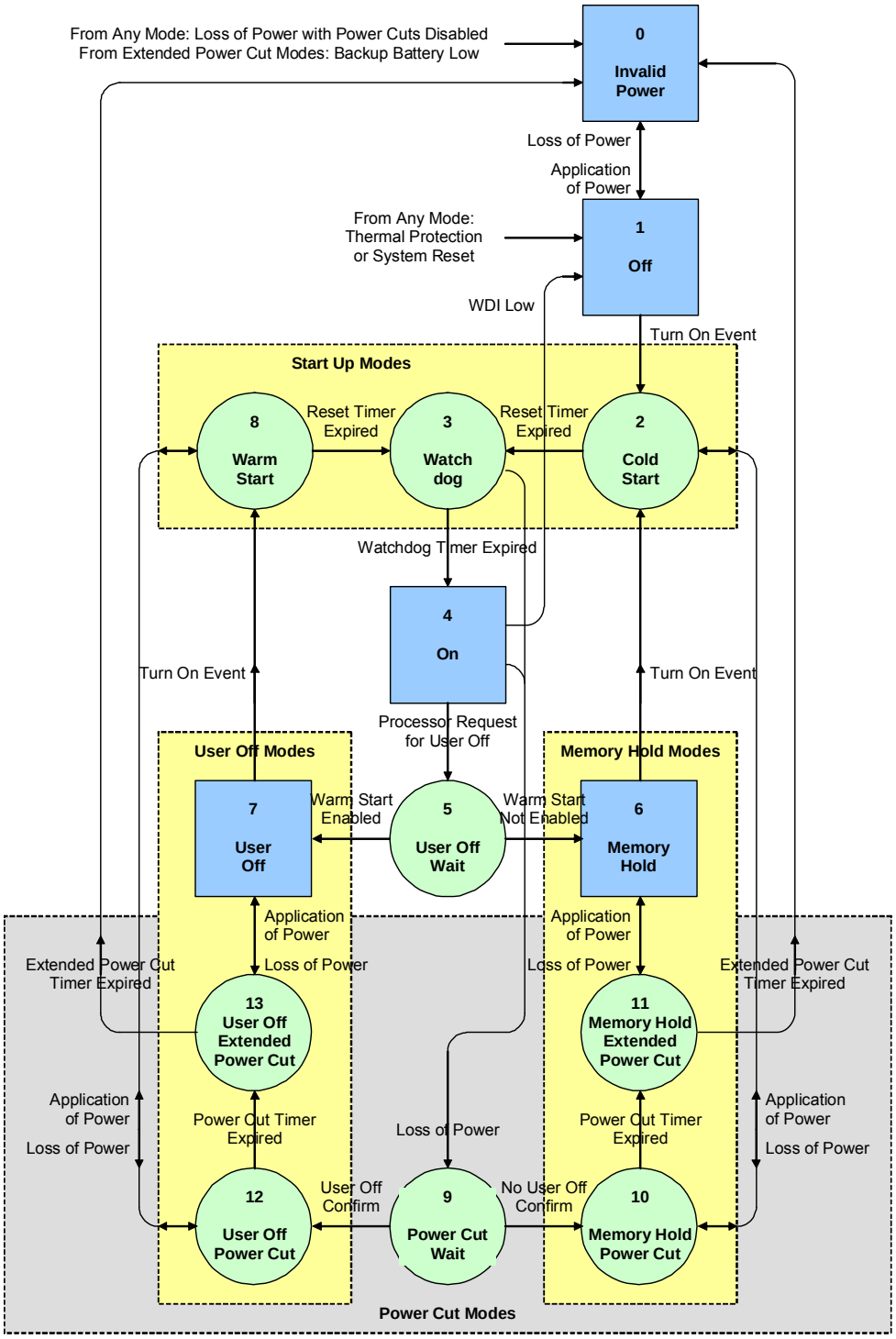
Table 5-1. Power Control System Interface Signals (continued)

Name	Type of Signal	Function
BPDET[1:0]	SPI bits	BP detection thresholds setting
USEROFFSPI	SPI bit	Initiates a transition to memory hold mode or user off mode
USEROFFPC	SPI bit	Allows to transition to user off during power cut with USEROFF low
USEROFFCLK	SPI bit	Keeps the CLK32KMCU active during user off modes
CLK32KMCUEN	SPI bit	Enables the CLK32KMCU clock output, defaults to 1
VBKUP1EN	SPI bit	Enables VBKUP1 in startup modes, on and user off wait modes
VBKUP1AUTO	SPI bit	Enables VBKUP1 in user off and memory hold modes
VBKUP2EN	SPI bit	Enables VBKUP2 in startup modes, on and user off wait modes
VBKUP2AUTOMH	SPI bit	Enables VBKUP2 in memory hold modes
VBKUP2AUTOUO	SPI bit	Enables VBKUP2 in user off modes
WARMEN	SPI bit	Enables for a transition to user off mode
WARMI	SPI bit	Indicates that the application powered up from user off mode
MEMHLDI	SPI bit	Indicates that the application powered up from memory hold mode
PCEN	SPI bit	Enables power cut support
PCI	SPI bit	Indicates that a power cut has occurred
ON1BDBNC[1:0]	SPI bits	Debounce time on ON1B pin
ON2BDBNC[1:0]	SPI bits	Debounce time on ON2B pin
ON3BDBNC[1:0]	SPI bits	Debounce time on ON3B pin
ON1BRSTEN	SPI bit	System reset enable for ON1B pin
ON2BRSTEN	SPI bit	System reset enable for ON2B pin
ON3BRSTEN	SPI bit	System reset enable for ON3B pin
SYSRSTI	SPI bit	System reset interrupt
RESTARTEN	SPI bit	Allows for restart after a system reset

5.2 Operating Modes

5.2.1 Power Control State Machine

Figure 5-1 shows the flow of the power control state machine. This diagram serves as the basis for the description in the reminder of this chapter.



Legend and Notes

Blue Box = Steady State, no specific timer is running
Green Circle = Transitional State, a specific timer is running, see text
Dashed Boxes = Grouping of Modes for clarification
Loss of Power assumes that the power cuts function is enabled, else go to 'Invalid Power'
If a power cut occurs, asynchronously to the state machine, the backup circuit is activated
WDI has influence only in the 'On' state
For details on turn on events, see text

Figure 5-1. Power Control State Machine Flow Diagram

5.2.2 Battery Powered Modes

The following battery powered modes include the standard operation of the state machine. So called power cut modes are described in the next paragraph.

Invalid Power

The supply to the MC13783 at BP is below the UVDET threshold and the MC13783 is not in a Power Cut mode. No turn on event is accepted. The only blocks operational can be the charger interface and the RTC module. For the charger interface, see Chapter 8, “Battery Interface and Control”. For the RTC module, see Chapter 4, “Clock Generation and Real Time Clock”. No specific timer is running in this mode.

Off

The supply to the MC13783 at BP is above the UVDET threshold. Only the MC13783 core circuitry at VATLAS is powered as well as the RTC module, all regulators including VBKUPx are inactive. To exit the Off mode, a turn on event is required. No specific timer is running in this mode.

Cold Start

The switchers and regulators are powered up sequentially to limit the inrush current, see the power up sequence for further details in Section 5.3, “Power Up. The reset signals RESETB and RESETBMCU are kept low. The reset timer is set to zero and starts running when entering Cold Start. When expired, the Cold Start mode is exited for the watchdog mode and RESETB and RESETBMCU will be go high. Since RESETB and RESETBMCU are open drain outputs, the output will only go high if an external pull up resistor is available, either embedded on the processor or as a discrete.

Watchdog

The circuit is fully powered and under SPI control. The RESETB and RESETBMCU are high. The watchdog timer is set to zero when entering Watchdog mode and starts running from that point. The watchdog timer is voluntarily long when coming from the Cold Start mode to accommodate to the booting period of a wide range of processors. When coming from Warm start mode, the timer is set to a shorter period. When expired, the Watchdog mode is exited.

On

The circuit is fully powered and under SPI control. When entering this mode from Watchdog, the WDI pin has to be high and remain high to stay in this mode. The WDI I/O supply voltage, which is VIOLO, has to remain enabled to allow for proper WDI detection. If WDI is made low, or if VIOLO is disabled, the part will transition to Off mode. No specific timer is running in this mode.

User Off Wait

The circuit is fully powered and under SPI control. The WDI pin has no more control over the part. The Wait mode is entered by a processor request for user off by setting the USEROFFSPI bit high. The wait timer is set to zero when entering User Off Wait mode and starts running from that point. This leaves the processor time to finish its tasks. When expired, the Wait mode is exited for User Off mode or Memory

Hold mode depending on warm starts being enabled or not via the WARMEN bit. The USEROFFSPI bit is being reset at this point by RESETB going low.

Memory Hold

All switchers and regulators are powered off except for VBKUP1 and VBKUP2 if they were enabled up front by setting the VBKUP1AUTO and VBKUP2AUTOMH bits. The RESETB and RESETBMCU are low and CLK32K and CLK32KMCU are disabled. Upon a turn on event, Cold Start mode is entered, the default power up values are loaded, and the MEMHLDI interrupt bit is set. A cold start out of Memory Hold mode will result in shorter boot times compared to starting out of Off mode, since the program does not have to be loaded and expanded from flash. This is also called warm boot. No specific timer is running in this mode.

User Off

All switchers and regulators are powered off except for VBKUP1 and VBKUP2 if they were enabled up front by setting the VBKUP1AUTO and VBKUP2AUTOUO bits. The RESETB is low and RESETBMCU is kept high. The 32kHz output signal CLK32K is disabled, and CLK32KMCU is maintained in this mode if the CLK32KMCUEN and USEROFFCLK bits were both set. Upon a turn on event, Warm Start mode is entered, the default power up values are loaded. A warm start out of User Off mode will result in an almost instantaneous startup of the system, since the internal states of the processor were conserved. No specific timer is running in this mode.

Warm Start

The switchers and regulators are powered up sequentially to limit the inrush current, see the power up sequence for further details in Section 5.3, “Power Up. The reset signal RESETB is kept low and RESETBMCU is kept high and CLK32KMCU kept active if CLK32KMCU was set. The reset timer is set to zero when entering Warm Start and starts running from that point. When expired, the Warm Start mode is exited for the watchdog mode, a WARMI interrupt is generated, and RESETB will be made high.

NOTE

The SPI control is only possible in the Watchdog, On and User Off Wait modes and that the interrupt lines PRIINT and SECINT are kept low in all modes except for Watchdog and On.

5.2.3 Power Cut Modes

A power cut is defined as a momentary loss of power. This can be caused by battery contact bounce or a user-initiated battery swap. The memory and the processor core can be backed up in that case by the coincell depending on the supported mode selected.

The maximum duration of a powercut is determined by the powercut timer PCT[7:0]. By SPI this timer is set to a preset value. When a power cut occurs, the timer will internally be decremented till it expires, meaning counted down to zero. The contents of PCT[7:0] does not reflect the actual counted down value but will keep the programmed value and therefore does not have to be reprogrammed after each power cut.

To avoid a so called ambulance mode with a relaxing supply rail, the number of times a power cut mode occurs is counted with a 4 bit counter PCCOUNT[3:0] and can be limited up front to PCMAXCNT[3:0] by SPI programming. Upon exiting the power cut mode, due to reapplication of power, the PCCOUNT[3:0] counter is incremented by 1. When the contents of PCCOUNT[3:0] is equal to PCMAXCNT[3:0] then the next power cut will not be supported. After a successful power up after a power cut, software will have to clear the PCCOUNT[3:0] counter therefore. This function is enabled via the PCCOUNTEN bit.

To use the following described modes, power cuts have to be enabled by setting the PCEN bit high and by programming the power cut timer PCT[7:0] different from 0, and a valid backup voltage such as a lithium coincell has to be present. When powering on after a power cut has occurred, the PCI interrupt bit is set high.

In the extended power cut modes, the backup cell voltage is indirectly monitored by a comparator. When it falls below the RTCLOBATDET threshold, see chapter 4, the circuit transitions to Invalid Power mode.

When power cuts are not enabled, then in case of a power failure the state machine will transition to Invalid Power mode.

When in User Off Wait mode the current drain of the total application is supposed to be very low, a power cut in this mode is therefore ignored and the state machine will transition to Memory Hold or User Off mode at the end of the wait mode.

SPI control is not possible and the interrupt lines PRIINT and SECINT are kept low in all of the power cut modes.

Power Cut Wait

When the supply to the MC13783 at BP drops below the UVDET threshold the Power Cut Wait mode is entered and the power cut timer starts running. The backup coincell will now supply the memory and the processor cores via VBKUP1 and VBKUP2 respectively if the VBKUP1AUTO and one of the VBKUP2AUTOMH or VBKUP2AUTOUO bits were set. The PWRFAIL signal is pulled high and one timetick of the 32kHz clock later, the RESETB is pulled low while RESETBMCU is left high. The 32kHz output signal CLK32K is disabled, and CLK32KMCU is maintained in this mode if it was active. The wait timer is set to zero when entering Power Cut Wait mode and starts running from that point. This leaves the processor time to finish its tasks in a low-power mode. When expired, the Power Cut Wait mode is exited for User Off Power Cut mode or Memory Hold Power Cut mode depending on the input pin USEROFF being pulled high or low by the processor. When the USEROFFPC bit was set high it will always transition to User Off Power Cut mode independent of the USEROFF signal. The PWRFAIL signal is pulled low when leaving the Power Cut Wait mode.

Memory Hold Power Cut

The backup supply VBKUP1 is active if VBKUP1AUTO=1, supplying the core of the memory. The VBKUP2 can be active as well if VBKUP2AUTOMH=1. The RESETB and RESETBMCU are actively pulled low. The CLK32K and CLK32KMCU are disabled. When the power cut timer expires, the state machine transitions to the Memory Hold Extended Power Cut mode. Upon re-application of power, meaning BP rises first above the UVDET threshold and then above the BPON threshold, a cold start is engaged after the UVTIMER has expired

Memory Hold Extended Power Cut

The backup supplies VBKUP1 and VBKUP2 are active if VBKUP1AUTO and VBKUP2AUTOMH are set to 1 respectively. The RESETB and RESETBMCU are low and CLK32K is disabled. The extended power cut timer starts running when entering Memory Hold Extended Power Cut mode. If the timer is set to zero or when it expires, the state machine transitions to the Invalid Power mode. If the timer is set to infinite via the MEMALLON bit, the state machine will transition to Invalid Power mode when the coincell drops below RTCLOBATDET. Upon re-application of power while in the Memory Hold Extended Power Cut, meaning BP rises above the BPON threshold, the circuit ends up in the Memory Hold mode. When in Memory Hold mode, a loss of power is indicated by BP falling below the BPON threshold and not by BP falling below the UVDET threshold.

User Off Power Cut

The backup supplies VBKUP1 and VBKUP2 are active, supplying the cores of the memory and the processor if VBKUP1AUTO=1 respectively VBKUP2AUTOUO=1. The RESETB is low and the RESETBMCU is high. The CLK32K is disabled, and CLK32KMCU is maintained if the USEROFFCLK bit was set to 1. Note that CLK32KMCUEN has to be high as well for having the CLK32KMCU during On mode and User Off modes. The CLK32KMCU will not be maintained if the USEROFFCLK is set to 0. When the power cut timer expires, the state machine transitions to the User Off Extended Power Cut mode. Upon re-application of power, meaning BP rises first above the UVDET threshold and then above the BPON threshold, a warm start is engaged after the UVTIMER has expired.

User Off Extended Power Cut

The backup supplies VBKUP1 and VBKUP2 are active, supplying the cores of the memory and the processor if VBKUP1AUTO=1 respectively VBKUP2AUTOUO=1. The RESETB is low and the RESETBMCU is high. The CLK32K is disabled, and CLK32KMCU is maintained if the USEROFFCLK bit was set to 1. The extended power cut timer starts running when entering User Off Extended Power Cut mode. When expired, or when the coincell drops below RTCLOBATDET, the state machine transitions to the Invalid Power mode. Upon re-application of power while in the User Off Extended Power Cut mode, meaning BP rises above the BPON threshold, the circuit ends up in the User Off mode. When in User Off mode, a loss of power is indicated by BP falling below the BPON threshold and not by BP falling below the UVDET threshold.

As described above, the clocking and backup supply behavior depends on the actual power mode the state machine is in and the setting of the clocking and backup supply related SPI bits. Table 5-2 provides a summary for the clock output CLK32KMCU, for a summary of the VBKUPx behavior see Section 5.4.2, “Backup Regulators.”

Table 5-2. CLK32MCU Control Logic

Mode	CLK32KMCUEN	USEROFFCLK	Clock Output CLK32KMCU
Off Invalid Power Memory Hold Memory Hold Power Cut Memory Hold Extended Power Cut	X	X	Disabled
On	0	X	Disabled

Table 5-2. CLK32MCU Control Logic (continued)

Mode	CLK32KMCUEN	USEROFFCLK	Clock Output CLK32KMCU
Cold Start Warm Start Watchdog User Off Wait Power Cut Wait	1	X	Enabled
User Off	X	0	Disabled
User Off Power Cut	0	1	Disabled
User Off Extended Power Cut	1	1	Enabled

5.2.4 Turn On Events

If the MC13783 is in Off, User Off or Memory Hold mode, the circuit can be powered on via a turn on event. The turn on events are listed in the following paragraph. To indicate to the processor what turn on event caused the system to power on, an interrupt bit is associated with each of the turn on events.

ON1B, ON2B or ON3B pulled low with corresponding interrupts ONOFD1I, ONOFD2I and ONOFD3I. A power on/off button is connected here. The state of the ONxB pins can be read out via the corresponding sense bits ONOFD1S, ONOFD2S and ONOFD3S.

At default, the falling edge of the ONxB pins is not debounced. A software debounce can be created by reading out the sense bits while starting up. Accidental triggering of the ONxB lines due to for instance a very short key press then remains unnoticed to the user. By SPI, a falling edge hardware debounce can be programmed via the ONxBDBNC[1:0] bits which will be backed up by the coincell. This avoids the application to power up upon a very short key press.

The rising edge of the ONxB pins will generate an interrupt as well. This edge is always debounced for 30ms. This interrupt generation avoids software from pulling the state of the sense bit.

The interrupt bits are always debounced with 30 ms on top of the optional falling edge debounce. The interrupts are reset by RESETB which makes that at power up no ONOFDxI interrupt will be generated. The total minimum time the OnxB must be pulled low at power up in order to be recognized by software by the sense bit being low therefore equals the ONxBDBNC delay time plus the Cold Start timer length.

For a falling edge of ONxB, when the input signal bounces during the 30ms debounce period of the interrupt bit, no interrupt will be generated. On the other hand, if the part was powered off, it will not prevent the part from powering on. In general, it is advised that the debounce period is set long enough to filter out mechanical bouncing.

The interaction between the OnxB pin, the turn on event, the sense and interrupt bits as described above is depicted in Figure 5-2.

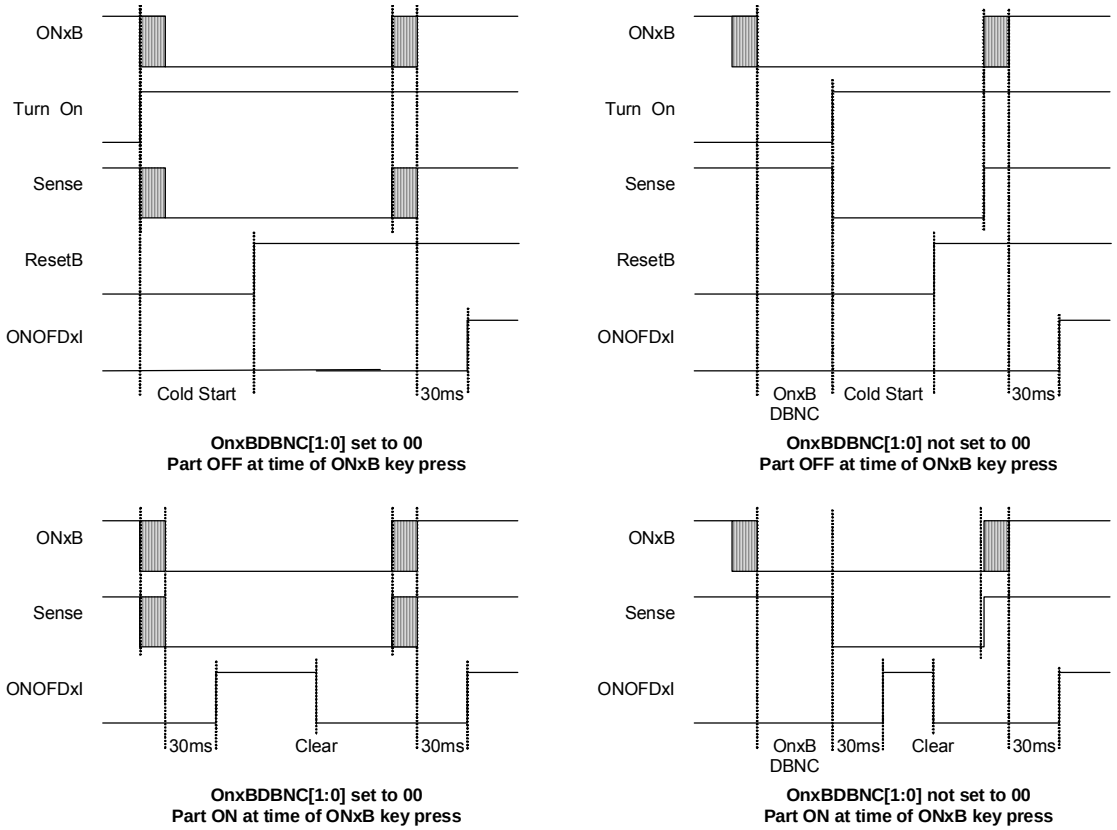


Figure 5-2. ONxB Debounce Timing Diagrams

Table 5-3. ONxB Debounce Bit Settings

Bits	State	Debounce in ms
ON1BDBNC[1:0]	00	0
ON2BDBNC[1:0]	01	30
ON3BDBNC[1:0]	10	150
	11	750

The ON1B, ON2B and ON3B turn on events are different from the other turn on events in that as long as BP is greater than the UVDET threshold, a cold or warm start is engaged when in Off, User Off or Memory Hold mode. However, when in the power cut modes, the BP has to rise above the BPON threshold before turning on

CHRGRAW pulled high with corresponding interrupt CHGDETI (reset by RESETB). This is equivalent to plugging in a charger. The state of the CHRGRAW pin can be read out via the corresponding sense bit CHGDETS. The charger turn on event is conditioned by other parameters like the BATT voltage and is dependent on the charge mode selected. For details on the charger detection and turn on, see the charger control logic table with the 'charger turn on signal' in Chapter 8, “Battery Interface and Control”.

BP crossing the BPON threshold with corresponding interrupt BPONI which corresponds to attaching a charged battery to the phone. In order for a valid BPON event to occur, the BP voltage needs to cross the UVDET threshold and then the BPON threshold within 8mS.

VBUS pulled high with corresponding interrupt USBI. This is equivalent to plugging in a supplied USB cable. For details on the USB detection, see Chapter 10, “Connectivity”.

TODA and DAYA register contents match the TOD and DAY contents with corresponding interrupt TODAI. This corresponds to a preset alarm time and day being reached. This allows powering up a phone at a preset time.

System restart with SYSRTSI interrupt which may occur after a system reset. This is an optional function, see also the turn off events section in this chapter.

Masking the interrupts related to the turn on events will not prevent the part to turn on except for the time of day alarm, see also Chapter 4, “Clock Generation and Real Time Clock”.

When powering up, it is also important for the software to know from which initial mode it powered up. In particular the interrupts PCI, WARMI, and MEMHLDI are used for this. Table 5-4 lists the state of these bits as a function of the last mode before power up (initial mode) and the intermediate modes between On and the initial mode.

Table 5-4. Power Up Initial Mode Determination

Initial Mode (#)	Intermediate Modes #	MEMHLDI	WARMI	PCI
User Off (7)	5 or 5-7-13	0	1	0
	9-12-13	0	1	1
User Off Power Cut (12)	9	0	1	1
Memory Hold (6)	5 or 5-6-11	1	0	0
	9-10-11	1	0	1
Memory Hold Power Cut (10)	9	0	0	1

As can be seen, in the case of a power up out of User Off Power Cut or out of User Off via power cuts (9-12-13), no distinction can be made based on the three interrupt bits. In that case, the distinction can be made based on the normal turn on event detection, because in order to power up when in User Off, a turn on event is required to go to Warm start, which is not the case for User Off Power Cut for which a battery insertion is sufficient.

Because the these interrupt bits are only reset by RTCPORB or by SPI access, it may be indifferent when coming out of the OFF mode or any of the previously listed modes. To identify that the power up occurs starting from Off, the VBKUP1AUTO bit can be verified. This bit is reset to 0 when in OFF mode and if the platform supports modes such as User Off or Memory Hold this bit has to be set to a 1 right after startup so in practice it will be a 1 when starting up out of any other mode.

5.2.5 Turn Off Events

To turn off the phone, the user will press the power button connected to the ONxB pin. This will generate an ONxBI interrupt but will not power off the part. The phone is powered off upon software initiative based on this interrupt, by pulling WDI low. Pressing the power button is therefore under normal circumstances not considered as a turn off event for the state machine in the MC13783.

A second function of the ONxB pins is the possibility to generate a system reset. This is recognized as a turn off event. By default, the system reset function is disabled but can be enabled via the ONxBRSTEN bits which are backed up via the coincell. When enabled, a 4 second long press on the power button ONxB while WDI is high will cause the MC13783 to go to the Off mode and as a result the entire application will power down. A SYSRSTI interrupt is generated upon the next power up. The system will restart automatically one second later if the RESTARTEN bit was set.

When the MC13783 die gets overheated, the thermal protection will power off the part to avoid damage. If a Cold Start is engaged when the thermal protection is still being tripped, the part will revert back to Off mode. See Chapter 2, “General Description” for details on the thermal protection thresholds.

When the voltage at BP drops below the under voltage threshold the parts is turned off as well.

5.2.6 Power Monitoring

The voltage at BP is permanently monitored by a set of detectors. Figure 5-3 shows the behavior for each of these detectors as a function of the BP voltage.

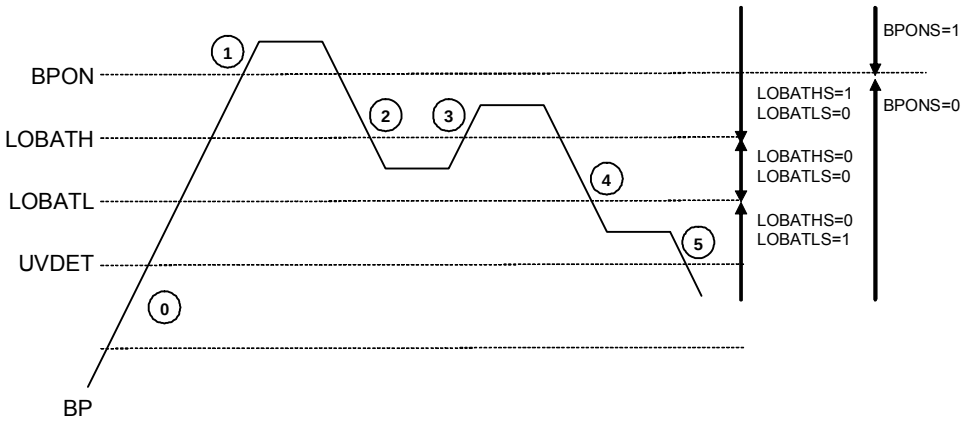


Figure 5-3. BP Detection Diagram

The following list describes events 0 to 5 together with the typical circumstances under which the events occur.

0. Application of battery. BP exceeds the minimum operating voltage which enables the MC13783 core circuitry. BP also exceeds UVDET which starts the UVTIMER.

1. Application of battery. BP exceeds BPON which creates a turn on event, see also turn on events section, if the UVTIMER is expired, and an interrupt BPONI=1 is generated. An interrupt is only generated on the rising edge of the BPON and is debounced by 30 ms (milliseconds). BPONS follows the state of the comparator.

2. The battery voltage sags due to transmit bursts. BP drops below LOBATH which generates an interrupt LOBATHI debounced by 30 us (microseconds).
3. The battery voltage recovers at the end of the transmit burst. BP exceeds LOBATH which generates an interrupt LOBATHI debounced by 30 us (microseconds). LOBATHS follows the state of the comparator. Setting the EOLSEL bit high has no influence on this behavior.
4. The battery voltage sags due to transmit bursts or battery removal. BP drops below LOBATL which generates an interrupt LOBATLI which is not debounced. At the same time the LOBATB pin will go low. Any BP transitions shorter than 1us will be filtered out by the comparator to avoid that very rapid current spikes cause the LOBATLI to be generated and LOBATB to go low. LOBATLS follows the state of the comparator.

   If the EOLSEL bit is set, the LOBATL threshold is not monitored but the drop out on the VRF1, VRF2 and VRFREF regulators. If one of these regulators get out of regulation, the non debounced LOBATLI interrupt is generated and the LOBATB pin will be made low. There is no additional filtering on the EOL comparator. LOBATLS will follow the state of the EOL comparator.
5. The battery voltage sags due to transmit bursts or battery removal. BP drops below UVDET which is recognized as a power cut which will make the PWRFAIL pin go high. The UVDET comparator is intentionally made slow to avoid phone shut down upon fast BP transitions due to rapid current spikes.

The thresholds are programmable via the BPDET[1:0] bits which are maintained by the coincell in order to allow for different detection levels depending on the application.

Table 5-5. BP Detection Thresholds

Bit Setting		Falling Edge Threshold in V			
BPDET1	**BPDET0**	**UVDET**	**LOBATL**	**LOBATH**	**BPON**
0	0	2.6	UVDET + 0.2	UVDET + 0.4	3.2
0	1	2.6	UVDET + 0.3	UVDET + 0.5	3.2
1	0	2.6	UVDET + 0.4	UVDET + 0.7	3.2
1	1	2.6	UVDET + 0.5	UVDET + 0.8	3.2
Default setting for BPDET[1:0] at startup is 00. The rising edge threshold is 100 mV higher than the falling edge threshold. The detection thresholds are ±50 mV accurate. All thresholds are correlated.					

Table 5-6 summarizes the detect and interrupt behavior as described above.

Table 5-6. BP Detection Summary

Comparator	Output	Description	Functionality
BPON	BPONS	Output of ON comparator BPONS = 1 when BP > BPON Threshold	Turn On event BPONI = 1 interrupt generated at rising edge of BPONS, debounced by 30 ms
LOBATH	LOBATHS	Output of LOBAT HIGH Comparator LOBATHS = 1 when BP > LOBATH Threshold	LOBATHI = 1 interrupt generated at rising and falling edge of LOBATHS, debounced by 30 us

Table 5-6. BP Detection Summary (continued)

Comparator	Output	Description	Functionality
LOBATL	LOBATLS[1]	Output of LOBAT LOW Comparator LOBATLS = 1 when BP < LOBATL Threshold	LOBATLI = 1 interrupt generated at rising edge of LOBATLS. The LOBATB pin is asserted LOW at the same time
EOL	—	Output of End Of Life comparator EOLS = 1 when VRF1 or VRF2 or VRFREF Get out of Regulation	—
UVDET	UVDETS	Output of Under Voltage comparator UVDETS = 0 when BP < UVDET Threshold	Power cut PWRFAIL pin is asserted HIGH

[1] LOBATLS is a result of LOBATL if EOLSEL = 0, and of EOL if EOLSEL = 1.

5.2.7 Timers

The different timers as used by the state machine are listed in Table 5-7. This listing does not include RTC timers for timekeeping. A synchronization error of up to one clock period may occur with respect to the occurrence of an asynchronous event, the duration listed in Table 5-7 is therefore the effective minimum time period.

Table 5-7. Timer Main Characteristics

Timer	Mode	Duration
Under Voltage Timer	Invalid Power Power Cut Modes	4 ms
Reset Timer	Cold Start Warm Start	56 ms
Watchdog Timer	Watchdog when coming from Warm Start	62.5 ms
	Watchdog when coming from Cold Start	500 ms
Wait Timer	User Off Wait Power Cut Wait	8 ms
Power Cut Timer PCT[7:0]	Power Cut Wait Memory Hold Power Cut User Off Power Cut	Programmable up to 8 seconds
Extended Power Cut Timer MEMTMR[3:0]	Memory Hold Extended Power Cut User Off Extended Power Cut	—
	with MEMALLON=0	Programmable up to 8 minutes
	with MEMALLON=1 and MEMTMR[3:0]<>0000	Infinite

5.3 Power Up

The default power up state and sequence of the MC13783 is controlled by the power up mode select pins PUMS.

At power up all regulators and switchers are sequentially enabled at equidistant steps of 2 ms to limit the inrush current. Any under voltage detection at BP is masked while the power up sequencer is running.

Three different power up sequences are selectable via the PUMS3 setting as given in Table 5-8.

Table 5-8. Power Up Sequence

Tap x 2ms	Supply Enable		
	PUMS3 = Ground	PUMS3 = Open	PUMS3 = VATLAS
0	Power Gating	Power Gating	Power Gating
1	SW2A	SW3	VBKUP1, VRFREF
2	SW2B	VBUS, VUSB	VIOHI, VIOLO
3	VIOLO, VIOHI	VBKUP1, VRFREF	SW1A
4	VRFDIG, VRFREF, VRFCP, VRFBG	SW1A	SW1B
5	VMMC1	SW1B	VGEN, VRFDIG, VBKUP2
6	VMMC2	VIOHI, VIOLO, VRFDIG, VGEN	VDIG, VRFCP, VRFBG
7	VSIM, VESIM	SW2A	SW2A
8	SW1A	SW2B	SW2B
9	SW1B	VDIG, VCAM, VBKUP2	VRF1
10	VDIG, VGEN, VBKUP1, VBKUP2	VSIM, VESIM	VRF2
11	VCAM	VRFCP, VRFBG, VAUDIO	VMMC1
12	VRF1	VRF1	VMMC2
13	VRF2	VRF2	SW3
14	SW3	VMMC1	VSIM, VESIM, VCAM
15	VBUS, VUSB, VAUDIO	VMMC2	VBUS, VUSB, VAUDIO

The state of the PUMS3 pin is latched in before any of the switchers or regulators is enabled. The startup sequencing of the switchers is not different when the switchers A and B section are joined.

The state of the PUMS1 and PUMS2 pins is also latched in at the start of the power up sequence. The PUMS1 and PUMS2 determine the initial setup for the voltage level of the switchers and regulators and if they get enabled or not. See Table 5-9 for the assignment.

Table 5-9. Power Up Defaults

Supply	Default Value								
PUMS2 ◊ PUMS1 ◊	Ground Ground	Ground Open	Ground VATLAS	Open Ground	Open Open	Open VATLAS	VATLAS Ground	VATLAS Open	VATLAS VATLAS
SW1A (*)	1.2	1.6	1.6	1.85	1.5	NA	NA	NA	NA
SW1B (*)	1.2	1.6	1.6	1.85	Off	NA	NA	NA	NA
SW2A (*)	1.8	1.8	1.2	1.20	1.8	NA	NA	NA	NA
SW2B (*)	1.8	1.8	1.2	1.20	Off	NA	NA	NA	NA
SW3	5.5	5.5	5.5	5.5	Off	NA	NA	NA	NA
VAUDIO	2.775	2.775	2.775	2.775	Off	NA	NA	NA	NA
VIOHI	2.775	2.775	2.775	2.775	2.775	NA	NA	NA	NA
VIOLO	1.8	1.8	1.8	1.8	1.8	NA	NA	NA	NA
VDIG	1.2	1.5	1.3	1.3	Off	NA	NA	NA	NA
VRFDIG	1.875	1.875	1.5	Off	1.5	NA	NA	NA	NA
VRFREF	2.775	2.775	2.775	2.775	Off	NA	NA	NA	NA
VRFCP	2.775	2.775	2.775	2.775	Off	NA	NA	NA	NA
VRFBG	1.2	1.2	1.2	1.2	Off	NA	NA	NA	NA
VSIM	Off	Off	Off	Off	Off	NA	NA	NA	NA
VESIM	Off	Off	Off	Off	Off	NA	NA	NA	NA
VGEN	1.5	1.5	1.1	1.1	Off	NA	NA	NA	NA
VCAM	Off	2.8	Off	Off	Off	NA	NA	NA	NA
VRF1	2.775	2.775	2.775	2.775	2.775	NA	NA	NA	NA
VRF2	2.775	2.775	2.775	Off	2.775	NA	NA	NA	NA
VMMC1	Off	2.8	2.8	3.0	Off	NA	NA	NA	NA
VMMC2	Off	2.8	2.8	Off	Off	NA	NA	NA	NA
VBKUP1	Off	Off	Off	1.575	Off	NA	NA	NA	NA
VBKUP2	Off	Off	Off	Off	Off	NA	NA	NA	NA
VUSB	Off	Off	Off	Off	Off	NA	NA	NA	NA
VBUS	Off	Off	Off	Off	Off	NA	NA	NA	NA

Off indicates the regulator is not enabled and the regulator setting bits are set to 0.
(*) The same voltage setting is loaded for SWxy[5:0], SWxyDVS[5:0] and SWxySTBY[5:0] and the same mode setting is loaded for SWxyMODE[1:0] and SWxySTBYMODE[1:0].

The state of the PUMS pins as well as the combined switcher modes can be read out via the sense bits PUMS1SNS[1:0], PUMS2SNS[1:0], PUMS3SNS[1:0], SW1ABSNS, SW2ABSNS, ICTESTSNS. A pin to ground corresponds to 00, open to 01 and to VATLAS to 11. See also Chapter 3, “Programmability”.

5.4 Memory Hold

5.4.1 Memory Hold Operation

The Memory Hold circuit provides power to the memory in the memory hold and user off modes and during a power cut via VBKUP1. To avoid leakage from the VBKUP1 into circuitry connected to BP during these modes, an external PMOS is to be placed between the memory supply, for example, the switcher 2B, and the memory itself. The MEMHLDDRV pin controls the gate of the external PMOS and is normally active low. During for instance a power cut, MEMHLDDRV will go high to VBKUP1 immediately when the power cut is detected (so at the same time as PWRFAIL goes high) and the PMOS is no longer conducting. The intrinsic diode of the PMOS will now avoid any leakage. When getting out of the power cut, the MEMHLDDRV pin is made low after the last tap of the power up sequencer, but before the reset timer has expired. If power cuts, memory hold and user off modes are not to be supported by the application, the PMOS can be removed.

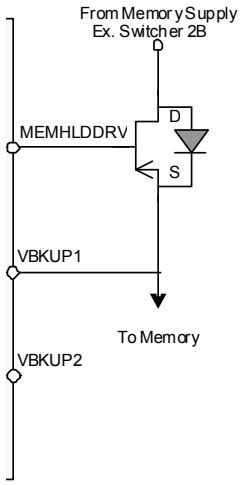


Figure 5-4. Memory Hold Circuit

Table 5-10. MEMHLDDRV Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
MEMHLDDRV Turn On Delay	1 nF load	—	—	1	us
MEMHLDDRV Output Low	100 uA load	0	—	0.2	V
MEMHLDDRV Output High	100 uA load	VBKUP1–0.2	—	VBKUP1	V

The state of the memory hold drive output is entirely determined by the power control state machine. The power gate drive output is SPI and pin controlled in the active modes, see Chapter 6, “Supplies”, and by the power control state machine in the other modes. This behavior is summarized in Table 5-11.

Table 5-11. Memory Hold and Power Gate Drive State Control

Mode		MEMHLDDRV	PWGTxDRV
Off Invalid Power		Hi Z or Low	Hi Z or Low
Cold Start	When coming from Off mode	Low	High[1]
Cold Start Warm Start	When NOT coming from Off mode and until end of power up sequencer	High	Low
	After power up sequencer has ended	Low	High
Watchdog On User Off Wait		Low	Controlled
Power Cut Wait User Off User Off Power Cut User Off Extended Power Cut Memory Hold Memory Hold Power Cut Memory Hold Extended Power Cut		High	Low

1 At the first tap of the power up sequencer.

5.4.2 Backup Regulators

The backup regulators VBKUP1 and VBKUP2 provide two independent low-power supplies during memory hold, user off and power cut operation. VBKUP1 is dedicated for backing up the memory core supply, and VBKUP2 the processor core. They can however also be used during normal operation. During normal operation they can be enabled via their enable bit VBKUP1EN and VBKUP2EN. For VBKUP1EN, its programming may be done during Watchdog or On mode but will have only effect in On mode. The VBKUP2EN has not such a limitation. The regulators can be enabled automatically when transitioning to the memory hold, user off and power cut modes by setting the VBKUP1AUTO, VBKUP2AUTOMH and VBKUP2AUTOUO bits.

The output voltage of the backup regulators is programmable via VBKUP1[1:0] and VBKUP2[1:0] to accommodate the different memory and core voltage ranges. Low-power discrete regulators can be attached to the VBKUPx regulators but note that some of the IOs of the MC13783, especially related to power cuts, are driven from VBKUPx. Therefore care must be taken that during normal operation the VBKUPx outputs are pulled high, see Figure 5-5.

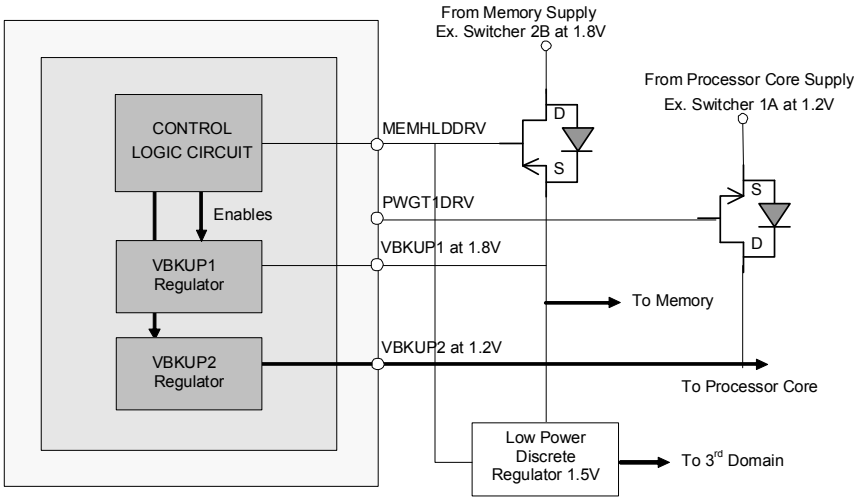


Figure 5-5. Backup Of Three Domains

Table 5-12. Backup Regulators Voltage Settings

Parameter	Value	Function
VBKUP1[1:0]	00	output = 1.0 V
	01	output = 1.2 V
	10	output = 1.575 V
	11	output = 1.8 V
VBKUP2[1:0]	00	output = 1.0 V
	01	output = 1.2 V
	10	output = 1.5 V
	11	output = 1.8 V

The power up default voltage of the backup regulators when coming from Off mode is determined by the PUMS2:1 setting so '00' in nearly all cases. When powering up from the other modes the already programmed voltage is maintained.

Table 5-13. VBKUPx Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Output Voltage	Vout + 0.3V < Vin < 3.1V 0 < IL < ILmax	nom - 50m	nominal	nom +50m	V
Maximum Continuous Load Current ILmax	Vout + 0.3V < Vin < 3.1V	—	—	2	mA
PSRR	Vin = Vout + 1V IL = 75% of ILmax 20 Hz to 24 kHz	35	40	—	dB
Start-Up Overshoot	IL = 0	—	1	3	%

Table 5-13. VBKUPx Performance Specifications (continued)

Parameter	Condition	Min	Typ	Max	Units
Turn-on Time	Enable to 90% of end value IL = 0	—	—	1	ms
	Bypass capacitor already precharged	—	—	2	µs
Transient Load Response	See waveform chapter 6	—	1	2	%
Transient Line Response	See waveform chapter 6	—	5	8	mV
Active quiescent current	No load	—	5	8	µA
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	1	+35%	µF
Bypass Capacitor ESR	—	0	—	0.5	Ω
Note: For test purposes VATLAS will be used as the input to the VBKUPx regulator. Some items will not be tested and therefore must be considered as IC design targets.					

5.4.3 Chip Select

During a power cut, including the power cut wait period, the CSOUT pin will be pulled high to VBKUP1 via an internal 100 kOhm pull resistor. The CSOUT is to be connected to an SRAM chip select line to avoid the SRAM memory devices get written to during power cut conditions. In case of SDRAM as a memory device, the CSOUT function is not used.

5.4.4 Embedded Memory

The MC13783 has a small general purpose embedded memory to store critical data. The data written to MEMA[23:0] and MEMB[23:0] is maintained by the coincell, also during a power cut. This allows for certain applications to implement power cut support without the need for maintaining the SDRAM. The contents of the embedded memory is reset by RTCPORB.

5.5 Power Saving Modes

Several regulator and switcher power saving modes are provided in On mode. The regulators can be used in On mode, Low-power mode, and Off. The switchers can be used in On synchronous mode without pulse skipping, On non-synchronous mode with pulse skipping, Low-power hysteretic or pulse frequency mode, and Off. The performance in each of these modes is described in Chapter 6, “Supplies”. The regulators and switcher modes are fully programmable by SPI and controllable via a number of pins. This paragraph describes the relationship between them.

5.5.1 Regulators and Boost Switcher

Two standby pins are provided STANDBYPRI, coupled to the primary SPI, and STANDBYSEC coupled to the secondary SPI. In the following text, STANDBY is used to describe both pins. The regulators can be put in one of their power saving modes by programming and by controlling the standby pins. Each

regulator has an associated standby enable bit VxSTBY. This is valid for both the primary SPI set and the secondary SPI set. If this bit is set to 0, then the state of the STANDBY has no influence. If set to 1, then the power mode of the corresponding regulator can be controlled via the STANDBY pin. The power saving mode during standby itself is determined by up front SPI programming. By default the STANDBY pin will need to be active high to put the regulator in the desired power saving mode, however by setting the STANDBYPRIINV or the STANDBYSECINV bit to 1 the STANDBYPRI pin respectively the STANDBYSEC pin are interpreted as active low. In the reminder of this section it is supposed the STANDBY pins are interpreted as active high.

Table 5-14 summarizes the described behavior with VxEN = Regulator enable bit, VxMODE = Regulator power mode bit, under the assumption that a single SPI controls a regulator.

Table 5-14. Regulator Standby Control

VxEN	VxMODE	VxSTBY	STANDBY Pin	Regulator Vx
0	X	X	X	Off
1	0	0	X	On
1	1	0	X	Low Power
1	X	1	0	On
1	0	1	1	Off
1	1	1	1	Low Power
This table is valid for all regulators, except for: • VRFBG which has no low-power mode • VVIB which has no low-power mode and no standby control • ADREF which has no standby control For those cases consider the VxMODE or VxSTBY bits to be 0.				

By the arbitration register, see Chapter 3, “Programmability”, the primary SPI determines if a regulator is under control of the primary SPI or secondary SPI by programming the VxSEL[1:0] bits.

If set to 00 the primary SPI has sole control. If set to 01, only the primary SPI can program the voltage setting of the regulator while the control of its operating mode via the VxEN, VxMODE and VxSTBY bits can be done by both processors where the highest power mode is selected. If set to 10, only the secondary SPI can program the voltage setting of the regulator while the control of its operating mode can be done by both processors where the highest power mode is selected. If set to 11, the primary SPI has sole control and the STANDBYPRI and STANDBYSEC pins both have to be high to be able to enter the standby mode.

To determine the highest power mode for each regulator in case of a dual SPI control, the independent controls from each SPI are compared. The highest mode is ON, the lowest is Off. If for example the primary SPI has set a regulator On while the secondary SPI has set it to low-power, the resulting operating mode will be On. If the primary SPI has the standby mode programmed to Off, then if STANDBYPRI goes high the regulator will transition to low-power.

Table 5-15. Regulator Highest Power Mode Arbitration

Regulator Vx Mode Primary SPI Control	Regulator Vx Mode Secondary SPI Control	Regulator Vx Resulting Mode[1]	Read Back VxEN[2]	Read Back VxMODE[2]
Off	Off	Off	0	X
Off	Low Power	Low Power	1	1
Low Power	Off			
Low Power	Low Power			
X	On	On	1	0
On	X			

1 The resulting mode is also dependent on the VxSEL[1:0] setting, see Chapter 3, “Programmability”.

2 Valid for all regulators except VSIM when SIMEN is low, Chapter 6, “Supplies”.

The read back of the regulator control bits is based on the actual operating mode of the regulator. The three modes Off, Low-power and On are coded on the VxEN and VxMODE bits according to Table 5-15. As a result, the value read back may be different then the value written to these bits. Both the primary and secondary SPI will read back the same data independent of the fact if they have control or not over the regulator mode. The VxSTBY bit is not affected by this and is read back as programmed.

When starting up, the regulators get enabled according the power up sequencer settings. Some will be enabled, others will remain off. In case a regulator gets enabled during power up, the VxEN bit will be made high for both SPI busses. As a result, when selecting VxSEL[1:0]=01 or 10, both SPI busses will have to program the VxEN bit low to disable the Vx regulator.

The boost switcher SW3 is controlled in the same way as the regulators via the corresponding bits SW3EN, SW3MODE, and SW3STBY with the same modes on, off and low-power and the same coding for the read back.

5.5.2 Buck Switchers

The switchers can be put in one of their power saving modes by SPI programming and by controlling the STANDBY pins. Each switcher has associated power saving mode bits. The SWxMODE bit setting is valid for STANDBY being low, while the SWxSTBYMODE bits are validated for STANDBY is high. This is applicable for both the primary SPI set and the secondary SPI set. Table 5-16 summarizes the buck switcher power saving modes under the assumption that a single SPI controls a switcher.

Table 5-16. Switcher Mode Control

SWxMODE for STANDBY = Low	SWxSTBYMODE for STANDBY = High	Switcher SWx	Control Loop	Pulse Skipping	Current Range
00	00	Off	—	—	—
01	01	On	PWM	No	500 mA
10	10	On	PWM	Yes	500 mA
11	11	On	PFM	—	50 mA

The buck switchers have dynamic voltage scaling capability (DVS). With DVS the output voltage setting can be controlled via the DVS pins DVSSWxy (xy being 1A, 1B, 2A and 2B) and the STANDBY pins. Each of the switchers have 6 bits of control SWxy for their output voltage setting. There is a separate setting for the different operating modes and there is a separate setting for each of the SPI interfaces.

Table 5-17. Switcher Output Voltage Control, Single DVS

State of Pin STANDBY	State of Pin DVSSWxy	SWxABDVS=0 SWxy Output Voltage Determined By
0	0	SWxy[5:0]
0	1	SWxyDVS[5:0]
1	0	SWxySTBY[5:0]
1	1	SWxySTBY[5:0]

The polarity of the DVS pin is an active high. However, it does not mean that if the DVS pin is high, the output voltage of the switcher has to be lower. This is only determined by the value programmed into the SWxyDVS bits which therefore can be lower but also higher than the SWxy setting. The same counts for standby operation although in this case the SWxySTBY will be chosen to be lower or equal to SWxy.

The DVS pins of the switchers can be combined by setting the SW1ABDVS and the SW2ABDVS bit to a "1" for combining respectively the DVSSW1A with the DVSSW1B pin and the DVSSW2A pin with DVSSW2B pin. The combined DVS pins are associated to the switcher A section. Combining the DVS pins does not necessarily make that the outputs and control of the A and B sections are combined, that is determined at startup by the SWxBFB pin being connected to VATLAS or not. So, 2 DVS pins can be used for switcher A while still using the A and B switcher independently. In this case switcher B has no longer DVS control. The SWxABDVS bits are only accessible via the primary SPI. Table 5-18 indicates the output setting of the switcher in case of combined DVS pin use.

Table 5-18. Switcher Output Voltage Control, Dual DVS

State of Pin STANDBY	State of Pin DVSSWxA	State of Pin DVSSWxB	SWxABDVS=1 SWxA Output Voltage Determined By
0	0	0	SWxA[5:0]
0	1	0	SWxADVS[5:0]
0	0	1	SWxBDVS[5:0]
0	1	1	SWxBSTBY[5:0]
1	X	X	SWxASTBY[5:0]

A particular use case of this function is when the DSP and MCU of a processor share the same switcher. Both the DSP and the MCU can then control a DVS pin. By making SWxA, SWxADVS and SWxBDVS settings equal, the switcher will transition to the lower setting of SWxBSTBY if both DVS pins are high.

By the arbitration register, see Chapter 3, "Programmability," the primary SPI determines if a switcher is under control of the primary SPI or secondary SPI. If the primary SPI has assigned a switcher to the

secondary SPI, a switcher is programmable only via the secondary SPI and only controllable by STANDBYSEC. The same applies if it remains assigned to the primary SPI with the corresponding STANDBYPRI pin.

Like for the regulators, also switchers may be shared between processors. Examples are a shared switcher for modem and applications processor SDRAM, or a shared switcher for DSP and MCU side of the modem. Therefore also the switcher mode control can be shared. This sharing can be assigned on a switcher per switcher basis. By setting the SWxySTBYAND bit high both STANDBYPRI and STANDBYSEC have to be high before the standby mode is selected for switcher SWxy. The SWxSTBYAND bits are only accessible via the primary SPI.

5.5.3 Power Ready

To inform the processor that the switcher outputs have reached their new set point and that a power gate is fully conducting, a power ready signal is generated at the PWRRDY pin. At the same time a maskable PWRRDYI interrupt is generated.

In normal steady state operating mode the PWRRDY pin is high. When changing for a higher DVS set point for a buck switcher this pin will go low and will go high again when the higher set point is reached. When de-activating a power gate (so when the external NMOS goes from non conducting to conducting state) this pin will first go low and become high again when the gate of the external NMOS is fully charged. This pin does not change state when setting a lower DVS set point or when activating a power gate (so when the external NMOS goes from conducting to non conducting state).

When the buck switcher is in PFM mode, it will not affect the PWRRDY signal, the same is valid when the DVSSPEED is set to '00'. However, when enabling a switcher which was disabled, the PWRRDY signal will be made low during the startup period independent of its mode of operation. Also, at start up of the MC13783, PWRRDY will be maintained low throughout the cold start and warm start period.

The power ready function is not directly controlled by standby, but in case standby makes the set points of the switchers change it will indirectly influence it when getting out of standby. In Chapter 6, “Supplies”, more details on the power ready timing is given in the buck switcher and power gating sections.

5.6 Power Control Register Summary

Table 5-19 provides the Power Control 0 register 13 information for MC13783.

Table 5-19. Register 13, Power Control 0

Name	Bit #	R/W	Reset [1]	Default	Description
PCEN	0	R/W	RTCPORB	0	Power cut enable
PCCOUNTEN	1	R/W	RTCPORB	0	Power cut counter enable
WARMEN	2	R/W	RTCPORB	0	Warm start enable
USEROFFSPI	3	R/W	RESETB	0	SPI command for entering user off modes
USEROFFPC	4	R/W	RTCPORB	0	Automatic transition to user off during power cut
USEROFFCLK	5	R/W	RTCPORB	0	Keeps the CLK32KMCU active during user off power cut modes

Table 5-19. Register 13, Power Control 0 (continued)

Name	Bit #	R/W	Reset [1]	Default	Description
CLK32KMCUEN	6	R/W	RTCPORB	1	Enables the CLK32KMCU
VBKUP2AUTOMH	7	R/W	OFFB	0	Automatically enables VBKUP2 in the memory hold modes
VBKUP1EN	8	R/W	RESETB	0	Enables VBKUP1 regulator
VBKUP1AUTO	9	R/W	OFFB	0	Automatically enables VBKUP1 in the memory hold and user off modes
VBKUP10	10	R/W	NONE	*	Sets VBKUP1 voltage
VBKUP11	11	R/W	NONE	*	—
VBKUP2EN	12	R/W	RESETB	0	Enables VBKUP2 regulator
VBKUP2AUTOUO	13	R/W	OFFB	0	Automatically enables VBKUP2 in the user off modes
VBKUP20	14	R/W	NONE	*	Sets VBKUP2 voltage
VBKUP21	15	R/W	NONE	*	—
BPDET0	16	R/W	RTCPORB	0	BP detection threshold setting
BPDET1	17	R/W	RTCPORB	0	—
EOLSEL	18	R/W	RTCPORB	0	Selects EOL function instead of LOBAT
BATTDETEN	19	R/W	RTCPORB	0	Enables battery detect function
VCOIN0	20	R/W	RTCPORB	0	Coincell charger voltage setting
VCOIN1	21	R/W	RTCPORB	0	—
VCOIN2	22	R/W	RTCPORB	0	—
COINCHEN	23	R/W	RTCPORB	0	Coincell charger enable

[1] OFFB represents a reset when in Off or Invalid Power modes.

Table 5-20 provides the Power Control 1, register 14 information for MC13783.

Table 5-20. Register 14, Power Control 1

Name	Bit #	R/W	Reset	Default	Description
PCT0	0	R/W	RTCPORB	0	Power cut timer
PCT1	1	R/W	RTCPORB	0	—
PCT2	2	R/W	RTCPORB	0	—
PCT3	3	R/W	RTCPORB	0	—
PCT4	4	R/W	RTCPORB	0	—
PCT5	5	R/W	RTCPORB	0	—
PCT6	6	R/W	RTCPORB	0	—
PCT7	7	R/W	RTCPORB	0	—
PCCOUNT0	8	R/W	RTCPORB	0	Power cut counter
PCCOUNT1	9	R/W	RTCPORB	0	—

Table 5-20. Register 14, Power Control 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
PCCOUNT2	10	R/W	RTCPORB	0	—
PCCOUNT3	11	R/W	RTCPORB	0	—
PCMAXCNT0	12	R/W	RTCPORB	0	Maximum allowed number of power cuts
PCMAXCNT1	13	R/W	RTCPORB	0	—
PCMAXCNT2	14	R/W	RTCPORB	0	—
PCMAXCNT3	15	R/W	RTCPORB	0	—
MEMTMR0	16	R/W	RTCPORB	0	Extended power cut timer
MEMTMR1	17	R/W	RTCPORB	0	—
MEMTMR2	18	R/W	RTCPORB	0	—
MEMTMR3	19	R/W	RTCPORB	0	—
MEMALLON	20	R/W	RTCPORB	0	Extended power cut timer set to infinite
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 5-21 provides the Power Control 2, register 15 information for MC13783.

Table 5-21. Register 15, Power Control 2

Name	Bit #	R/W	Reset	Default	Description
RESTARTEN	0	R/W	RTCPORB	0	Enables automatic restart after a system reset
ON1BRSTEN	1	R/W	RTCPORB	0	Enables system reset on ON1B pin
ON2BRSTEN	2	R/W	RTCPORB	0	Enables system reset on ON2B pin
ON3BRSTEN	3	R/W	RTCPORB	0	Enables system reset on ON3B pin
ON1BDBNC0	4	R/W	RTCPORB	0	Sets debounce time on ON1B pin
ON1BDBNC1	5	R/W	RTCPORB	0	
ON2BDBNC0	6	R/W	RTCPORB	0	Sets debounce time on ON2B pin
ON2BDBNC1	7	R/W	RTCPORB	0	
ON3BDBNC0	8	R/W	RTCPORB	0	Sets debounce time on ON3B pin
ON3BDBNC1	9	R/W	RTCPORB	0	
STANDBYPRIINV	10	R/W	RTCPORB	0	If set then STANDBYPRI is interpreted as active low
STANDBYSECINV	11	R/W	RTCPORB	0	If set then STANDBYSEC is interpreted as active low
Unused	12	R	—	0	Not available
Unused	13	R	—	0	Not available
Unused	14	R	—	0	Not available

Table 5-21. Register 15, Power Control 2 (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 5-22 provides the Memory A, register 18 information for MC13783.

Table 5-22. Register 18, Memory A

Name	Bit #	R/W	Reset	Default	Description
MEMA0	0	R/W	RTCPORB	0	Backup memory A
MEMA1	1	R/W	RTCPORB	0	
MEMA2	2	R/W	RTCPORB	0	
MEMA3	3	R/W	RTCPORB	0	
MEMA4	4	R/W	RTCPORB	0	
MEMA5	5	R/W	RTCPORB	0	
MEMA6	6	R/W	RTCPORB	0	
MEMA7	7	R/W	RTCPORB	0	
MEMA8	8	R/W	RTCPORB	0	
MEMA9	9	R/W	RTCPORB	0	
MEMA10	10	R/W	RTCPORB	0	
MEMA11	11	R/W	RTCPORB	0	
MEMA12	12	R/W	RTCPORB	0	
MEMA13	13	R/W	RTCPORB	0	
MEMA14	14	R/W	RTCPORB	0	
MEMA15	15	R/W	RTCPORB	0	
MEMA16	16	R/W	RTCPORB	0	
MEMA17	17	R/W	RTCPORB	0	
MEMA18	18	R/W	RTCPORB	0	
MEMA19	19	R/W	RTCPORB	0	

Table 5-22. Register 18, Memory A (continued)

Name	Bit #	R/W	Reset	Default	Description
MEMA20	20	R/W	RTCPORB	0	Backup memory A
MEMA21	21	R/W	RTCPORB	0	
MEMA22	22	R/W	RTCPORB	0	
MEMA23	23	R/W	RTCPORB	0	

Table 5-23 provides the Memory B, register 19 information for MC13783.

Table 5-23. Register 19, Memory B

Name	Bit #	R/W	Reset	Default	Description
MEMB0	0	R/W	RTCPORB	0	Backup memory B
MEMB1	1	R/W	RTCPORB	0	
MEMB2	2	R/W	RTCPORB	0	
MEMB3	3	R/W	RTCPORB	0	
MEMB4	4	R/W	RTCPORB	0	
MEMB5	5	R/W	RTCPORB	0	
MEMB6	6	R/W	RTCPORB	0	
MEMB7	7	R/W	RTCPORB	0	
MEMB8	8	R/W	RTCPORB	0	
MEMB9	9	R/W	RTCPORB	0	
MEMB10	10	R/W	RTCPORB	0	
MEMB11	11	R/W	RTCPORB	0	
MEMB12	12	R/W	RTCPORB	0	
MEMB13	13	R/W	RTCPORB	0	
MEMB14	14	R/W	RTCPORB	0	
MEMB15	15	R/W	RTCPORB	0	
MEMB16	16	R/W	RTCPORB	0	
MEMB17	17	R/W	RTCPORB	0	
MEMB18	18	R/W	RTCPORB	0	
MEMB19	19	R/W	RTCPORB	0	
MEMB20	20	R/W	RTCPORB	0	
MEMB21	21	R/W	RTCPORB	0	
MEMB22	22	R/W	RTCPORB	0	
MEMB23	23	R/W	RTCPORB	0	

Chapter 6
Supplies

6.1 Supply Flow

The switch mode power supplies and the linear regulators are dimensioned to support a supply flow based upon Figure 6-1.

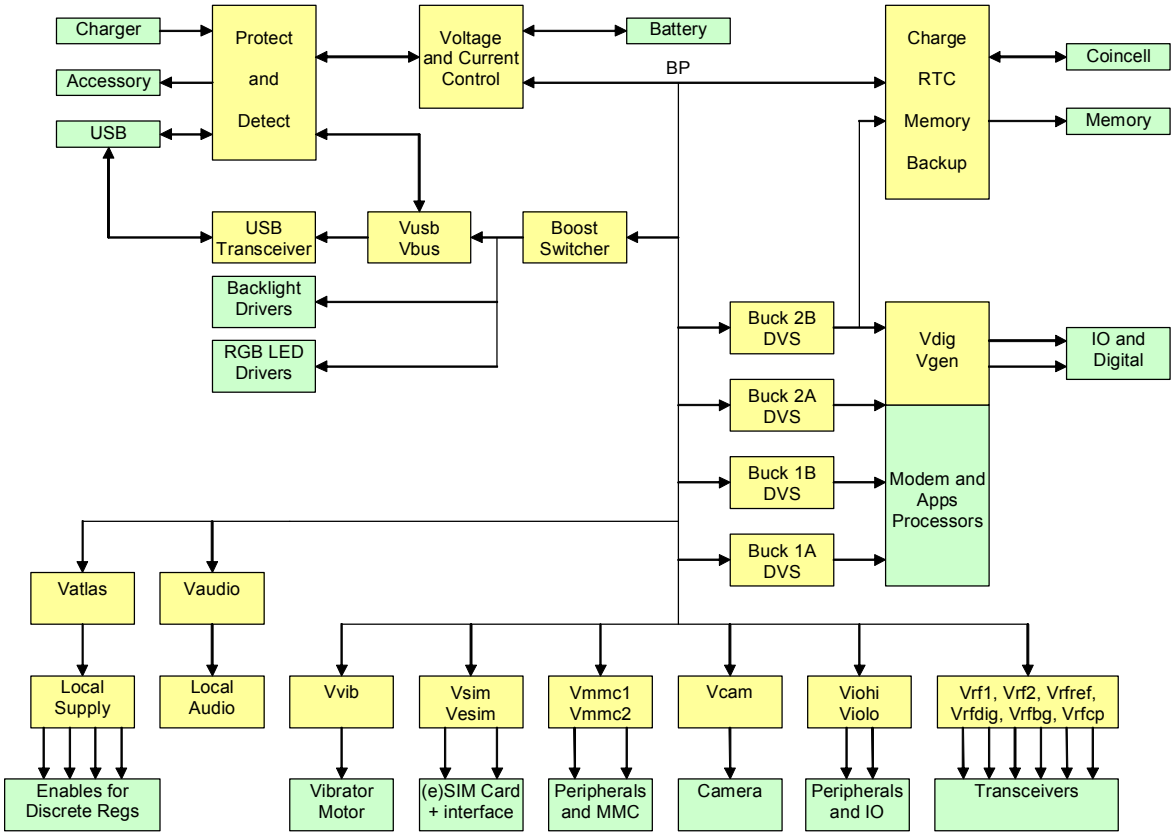


Figure 6-1. Supply Distribution

The minimum operating voltage for the supply tree, while maintaining the performance as specified, is 3.0 V. For lower voltages the performance may be degraded.

6.2 Switch Mode Supplies

The switch mode supplies consist of a core block, 4 step down (buck) switcher units and a step up (boost) switcher. The 4 buck switcher units can be combined to two buck switchers to provide more output power per switcher, see the following sections for details. The buck switchers support dynamic voltage scaling.

6.2.1 Common Circuitry

The switchers are clocked by a PLL which generates an effective 1.048 MHz signal based upon the 32.768 kHz oscillator signal by multiplying it by 32. The PLL is connected to the switchers via a clock tree and clock dividers which are gated only when one or more switchers are active. To reduce spurious for certain radio channels, the PLL can be programmed via PLLX[2:0] to different values.

Table 6-1. PLL Multiplication Factor

PLLX[2:0]	Multiplication Factor	Switching Frequency (Hz)	ADC Core Frequency (MHz)
000	28	917 504	1.835
001	29	950 272	1.901
010	30	983 040	1.966
011	31	1 015 808	2.032
100	32	1 048 576	2.097
101	33	1 081 344	2.163
110	34	1 114 112	2.228
111	35	1 146 880	2.294

Low-power standby modes are provided controlled by the standby pins. In the lowest power standby mode, the switchers no longer have to be PWM controlled and their output is maintained based on hysteresis control. If all switchers are in this mode and the ADC is not used, the PLL is automatically powered off unless the PLLEN bit was set to one.

To reduce peak inrush currents, the power up of the switchers will be sequenced according the power up sequence, see Chapter 5, “Power Control System.”

Table 6-2. Switch Mode Supplies Common Circuitry Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
Frequency Accuracy	Steady state	—	—	100	ppm
Turn On Time	Frequency within 50% of end value	—	—	100	µs
	Frequency within 5% of end value	—	—	300	µs
	Frequency within 1.4% of end value (5% phase error)	—	—	500	µs
Bias Current	PLL core only	—	130	—	µA
	PLL clock tree and dividers	—	50	—	µA

Table 6-3. PLL Control Registers

Name	R/W	Reset Signal	Reset State	Description
PLLEN	R/W	RSTSB	0	1 = Forces PLL on 0 = PLL automatically enabled
PLLX[2:0]	R/W	RSTSB	100	Selects PLL multiplication factor

6.2.2 Buck Switchers Control

Four identical sets of control bits are dedicated to each buck regulator SWxy, where xy stands for 1A, 1B, 2A and 2B.

Table 6-4. Buck Regulator Control Registers

Name	R/W	Reset Signal	Reset State	Description
SWxySTBYMODE[1:0]	R/W	NONE	**	SWxy standby mode select
SWxyMODE[1:0]	R/W	NONE	**	SWxy normal mode select
SWxyPANIC	R/W	RSTSB	0	SWxy panic mode enable 0= panic mode disabled 1= panic mode enabled
SWxySFST	R/W	RSTSB	1	SWxy soft start enable 0= soft start disabled 1= soft start enabled
SWxySTBY[5:0]	R/W	NONE	*	SWxy standby mode voltage select
SWxyDVS[5:0]	R/W	NONE	*	SWxy DVS mode voltage select
SWxy[5:0]	R/W	NONE	*	SWxy normal mode voltage select
SWxyDVSSPEED[1:0]	R/W	RSTSB	00	SWxy DVS speed select
* Reset State is identical and determined by PUMS2:1 at the beginning of cold start / warm start ** Reset State is determined by PUMS2:1 at the beginning of cold start / warm start and ‘00’ if Off and ‘01’ if On				

6.2.3 Buck Switchers

There are in total four buck switcher units: SW1A, SW1B, SW2A and SW2B. The units have the same topology. The A units are strictly identical as are the B units. The B unit can be put in parallel with the corresponding A unit, so SW1B can combine with SW1A and SW2B can combine with SW2A. When in parallel mode, the switcher voltage and mode are controlled by the programming of the A unit.

For single use, the SW1ABSPB and/or the SW2ABSPB pin(s) (i.e, SWxABSPB) must be tied high to VATLAS.

For parallel use of the switchers, the input and output power pins must be hardwired together while the SWxABSPB pin(s) must be tied to ground or left floating. The B unit feedback pin needs to be connected to VATLAS as well. The state of the hardware connection can be read back through the SPI register via the SWxABS bits. When the parallel mode is detected, all commands directed to the B switcher will be

ignored. All buck switchers have to be supplied from the BP. Figure 6-2 shows the high-level block diagram of the buck switchers. Table 6-5 shows the buck switcher units current capability.

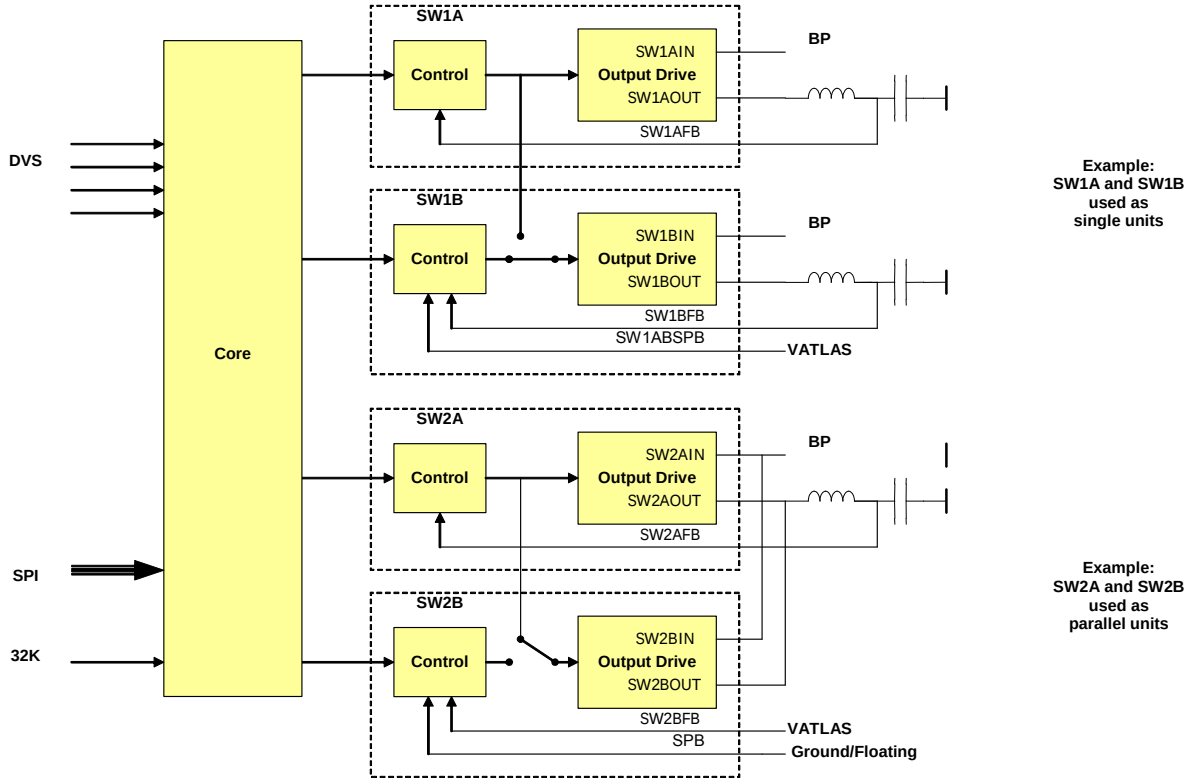


Figure 6-2. Buck Switcher Units Architecture

Table 6-5. Buck Switcher Units Current Capability

	Max Load for Single Unit		Max Load for Parallel Units	
	PWM Mode	PFM Mode	PWM Mode	PFM Mode
SW1A	500 mA	50 mA	1 A	50 mA
SW1B	500 mA	50 mA	—	—
SW2A	500 mA	50 mA	1 A	50 mA
SW2B	500 mA	50 mA	—	—

6.2.4 Buck Switchers Equations

During normal PWM operation, a high side switch (a power MOSFET) is turned on each clock cycle storing energy in the inductor while transferring energy into the load and output capacitor. The control loop compares the output voltage to internal references and controls when to turn off the high side switch. When the high side switch is off, the synchronous rectifier (a second power MOSFET) is turned on until either the inductor current changes polarity or at the start of the next converter cycle. When the synchronous rectifier is on, some of the stored energy in the inductor and capacitor are delivered to the load. At least two distinct phases occur, T1 (when the high side switch is on) and T2 (when the synchronous rectifier is on).

The ratio of T1 to a complete converter cycle is known as the duty cycle, D. In its simplest form it follows that D = Vout / Vin. In reality, D is slightly higher due to the series resistance of the inductor, high side switch and synchronous rectifier.

In medium to full load cases (greater than approximately 75 mA), the steady state, average inductor current is equal to the load current while the average capacitor current is zero. During the time that the high side switch is on the change in current flowing in the inductor is:

Eqn. 6-1

$$\Delta I = \frac{(Vin - Vout)}{L * F} D$$

Example: Vin = 3.6 V, Vout = 1.4 V, I = 200 mA, L = 10 uH, F=1 MHz, so D = 0.38 and the change in inductor current is 85.5 mA. Since the average current in the inductor is the load current, the inductor current will vary between 157.25 mA and 242.25mA. Referring to the Figure 6-3, it is apparent that the 85.5 mA of ripple current must flow into the capacitor absorbing the excess current from the inductor or providing the remaining of current required by the load.

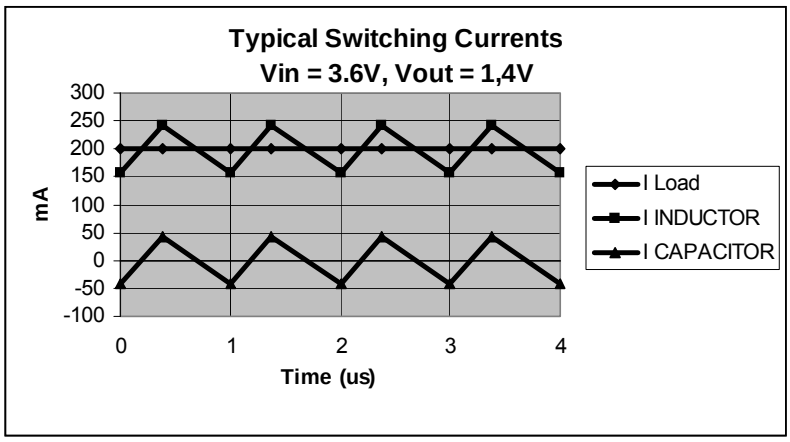


Figure 6-3. Typical Switching Currents

With +/-42.75 mA flowing through the capacitor, a ripple voltage is generated. It can be shown that:

Eqn. 6-2

$$\Delta Vripple = \Delta Iinductor * \left[ESR + \frac{1}{8CF} \right]$$

For this example using a 22 uF ceramic capacitor with 25 mOhm ESR a ripple component of 485 uV is due to the ideal capacitor while 2.14 mV is due to the ESR. The use of aluminum/tantalum electrolytic capacitors will have much more ripple voltage due to their greater ESR. In this case, a smaller ceramic capacitor must be placed in parallel to reduce the ESR induced ripple. Consequently, decreasing the inductor value will increase ripple by the same factor. The buck converters are designed to work with an inductor from 4.7 uH to 10 uH and a capacitor ranging from 22 uF to 2 x 22 uF.

6.2.5 Dynamic Voltage Scaling

The buck switchers support dynamic voltage scaling (DVS). The buck switchers are designed to directly supply the processor cores. To reduce overall power consumption, core voltages of processors may be varied depending on the mode the processor is in. The DVS scheme of the buck switchers allow for different set points between which it can transition in a controlled manner to avoid any sudden output voltage changes or peaks.

The set points for DVS are programmed via SPI. The real time control of the output voltage of each of the buck switchers is handled via one dedicated DVS control input per switcher in combination with the state of the standby pins. A total of three set points are available: a nominal which is the default value, a DVS level, and a standby level. The DVS and standby levels can be set lower or higher than nominal. Table 6-6 lists this functionality. For more details on the control and how to create 5 DVS levels per switchers by combining DVS pins, see Chapter 5, "Power Control System."

Table 6-6. DVS Control Logic

Standby	DVS	Set Point Selected By
0	0	SWxy
0	1	SWxyDVS
1	X	SWxySTBY

There are two standby pins available STANDBYPRI and STANDBYSEC. The control of these pins over the mode of the supplies is described in Chapter 5, "Power Control System."

NOTE

The standby pins also control the operation modes for the switchers.

While in PWM mode, the transition from one set point to another is effectively slope controlled by taking small steps between the set points cadenced in time. Since the buck switchers have a strong source capability and a very weak sink capability, the rising slope is fully determined by the switcher where the falling slope is determined by the load. Slope controlled behavior is provided for voltage changes in the entire voltage setting range. Note however that due to the bigger step size between the higher set points, the transition from one set point to another in that region will be not as smooth as for the lower set points, the net dV/dt however remains the same. As the current limitation in PFM mode is intentionally set low, controlled DVS transitions in PFM mode are not possible. Figure 6-4 shows the behavior.

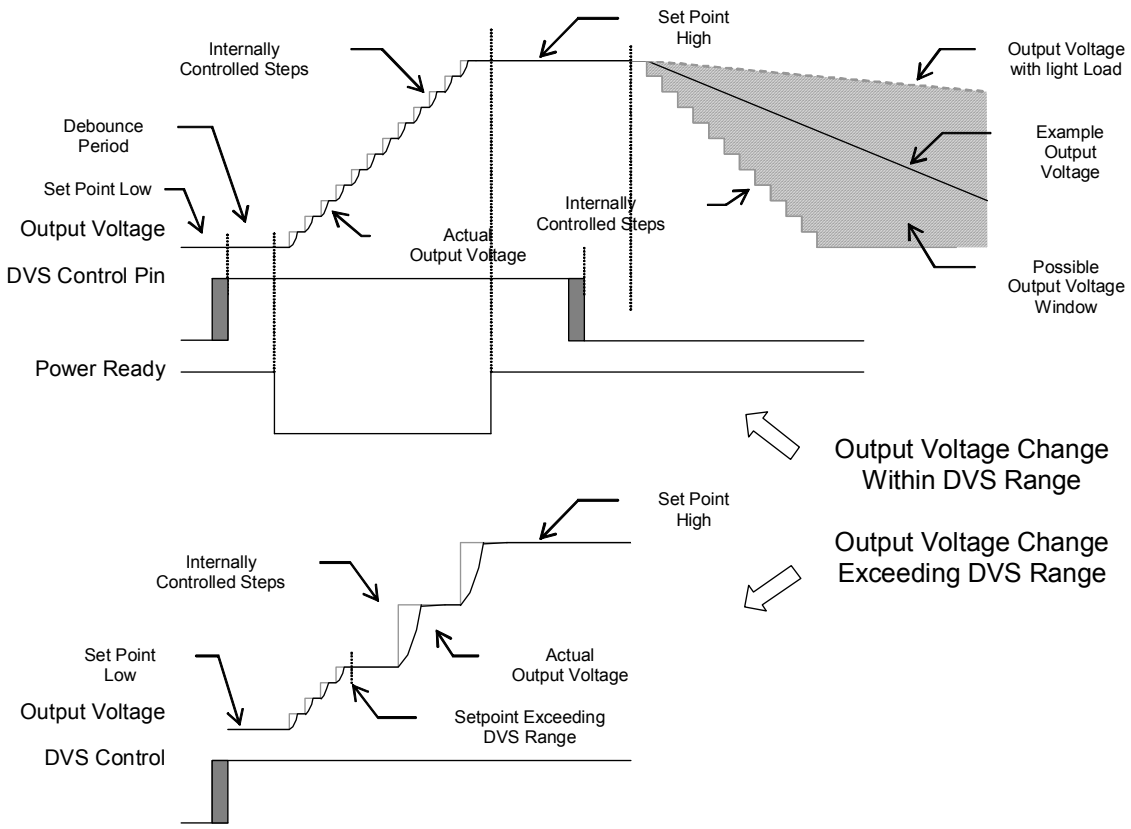


Figure 6-4. Global DVS Behavior

To inform the processor that the new set point is reached, a power ready signal is generated. In Figure 6-4, the timing of the internal power ready signal is indicated. The behavior of the power ready pin is dependent on the state of each of the switchers. When in PFM mode, a switcher module will always indicate a power ready. See Chapter 5, “Power Control System” for a detailed definition of the power ready signal.

Table 6-7 and Table 6-8 provide the key performance parameters and bit definitions for the DVS voltage manipulation registers. See Chapter 3, “Programmability and Chapter 5, “Power Control System” for the programming details for SPI arbitration, interrupt control and standby pin interactions.

Table 6-7. DVS Speed Selection

SWxyDVSSPEED[1:0]	Function
00	25 mV step each 4 us Power ready signal not influenced
01	25 mV step each 4 us
10	25 mV step each 8 us
11	25 mV step each 16 us

Table 6-8. Output Voltage Select Range

CODE	VOLTAGE SW1A, SW1B SW2A, SW2B	CODE (*)	VOLTAGE SW1A, SW1B	VOLTAGE SW2A, SW2B
000000	0.900	100000	1.700	
000001	0.925	100001	1.700	
000010	0.950	100010	1.700	
000011	0.975	100011	1.700	
000100	1.000	100100	1.800	
000101	1.025	100101	1.800	
000110	1.050	100110	1.800	
000111	1.075	100111	1.800	
001000	1.100	101000	1.850	1.900
001001	1.125	101001	1.850	1.900
001010	1.150	101010	1.850	1.900
001011	1.175	101011	1.850	1.900
001100	1.200	101100	2.000	
001101	1.225	101101	2.000	
001110	1.250	101110	2.000	
001111	1.275	101111	2.000	
010000	1.300	110000	2.100	
010001	1.325	110001	2.100	
010010	1.350	110010	2.100	
010011	1.375	110011	2.100	
010100	1.400	110100	2.200	
010101	1.425	110101	2.200	
010110	1.450	110110	2.200	
010111	1.475	110111	2.200	
011000	1.500	111000	2.200	
011001	1.525	111001	2.200	
011010	1.550	111010	2.200	
011011	1.575	111011	2.200	
011100	1.600	111100	2.200	
011101	1.625	111101	2.200	
011110	1.650	111110	2.200	
011111	1.675	111111	2.200	

6.2.6 Boost Switcher

SW3 is a boost supply, which can be programmed to a fixed output voltage level. SW3 supplies the backlights, and the regulators for the USB. Note that the parasitic leakage path for a boost switcher will cause the output voltage SW3OUT/SW3FB to rise along with the battery voltage whenever BP approaches or exceeds the programmed output level. The switching NMOS transistor is internal to the die. An external

flyback Schottky diode, inductor and capacitor are required. The boost switcher has a soft start mechanism which limits the peak currents when turned on. This reduces the inrush currents at for instance system startup. At the end of the turn on period the peak current limit comes back to its normal value.

The low-power mode of operation of SW3 set by the SW3MODE bit will not reduce the bias current for this block, as is the case for the buck switchers SW1 and SW2. However, it no longer makes use of the PLL, which can be turned off to save current. During this low-power mode, the output voltage will be maintained at its last standard mode setting through the use of an internal 32 kHz clock. When in low-power mode, the load current drive capability is reduced. SW3 must be enabled in normal mode of operation before enabling the low-power mode. The low-power mode can be entered automatically via standby, see Chapter 5, "Power Control System."

SW3 can be set to an adaptive mode for backlight headroom optimization, where it will provide constant voltage headroom for backlight LED drivers, see Chapter 11, "Lighting System". The adaptive mode programming is overruled by the standard output programming. The adaptive mode of operation will be disabled during a USB-OTG session. The adaptive mode of operation requires the PLL to be turned on to be active, and therefore the adaptive mode will be disabled during low-power mode.

Table 6-9. Switch Mode Supply #3 Control Function Summary

Parameter	Value	Function
SW3EN	0	SW3 OFF
	1	SW3 ON
SW3STBY[1]	0	SW3 mode not controlled by standby
	1	SW3 mode controlled by standby
SW3MODE[1]	0	SW3 low-power mode disabled
	1	SW3 low-power mode enabled
SW3[1:0]	00	Vout = 5.0 V
	01	Vout = 5.0 V
	10	Vout = 5.0 V
	11	Vout = 5.5 V

1 See Chapter 5, "Power Control System" for logic table.

Table 6-10. Switch Mode Supply #3 Characteristics

Parameter	Condition	Min	Typ	Max	Units
Average Output Voltage	Vinmin < Vin < Vinmax 0 < IL < ILmax	nom. -5%	nominal	nom. +5%	V
Output Ripple	Vinmin < Vin < Vinmax 0 < IL < ILmax Excluding reverse recovery of Schottky diode	—	—	120 mV	Vp-p
Operating Input Voltage Range Vinmin to Vinmax		3.0	—	4.65	V

Table 6-10. Switch Mode Supply #3 Characteristics (continued)

Parameter		Condition	Min	Typ	Max	Units
Extended Input Voltage Range		Performance may be out of specification	2.5	—	4.65	V
Average Load Regulation		Vin = 3.6 V 0 < IL < ILmax	—	—	0.5	mV/mA
Average Line Regulation		Vinmin < Vin < Vout – 0.3 V < Vinmax IL = IL max	—	—	50	mV
Maximum Continuous Load Current		Vinmin < Vin < Vout – 0.3 V < Vinmax	—	—	—	—
	ILmax	Normal Mode, Vout = 5.5 V	300	—	—	mA
	ILmax	Normal Mode, Vout = 5.0 V	350	—	—	mA
	ILmaxstby	Standby Mode	5	—	—	mA
Peak Current Limit		At SW3IN, Vin = 3.6 V	—	—	1500	mA
Start-Up Overshoot		IL = 0 mA	—	—	300	mV
Turn-on Time		Softstart active Enable to 90% of Vout IL = 0	—	—	2	ms
Mode Transition Time		From low-power to active IL = ILmaxstby	—	—	500	us
Transient Load Response		IL from 1 mA to 100 mA in 1 us	—	—	—	—
		Maximum transient Amplitude	—	—	300	mV
		Time to settle 80% of transient	—	—	500	us
Transient Load Response		IL from 100 mA to 1 mA in 1 us	—	—	—	—
		Maximum transient Amplitude	—	—	300	mV
		Time to settle 80% of transient	—	—	20	ms
Efficiency		IL = ILmax	65	80		%
Bias Current Consumption		Normal Mode	—	75	120	uA
		Standby Mode	—	75	120	uA
External Components		Used as a condition for all other parameters	—	—	—	—
		Inductor	-20%	4.7	+20%	uH
		Inductor Resistance	—	—	0.3	Ω
		Inductor saturation current at 30% loss in inductance value	1.1	—	—	A
		Bypass Capacitor	-35%	22	+35%	uF
		Bypass Capacitor ESR 100 kHz – 10 MHz	1	—	20	mΩ
		Diode current capability	850	—	—	mAdc
			1500	—	—	mApk

Table 6-10. Switch Mode Supply #3 Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
NMOS On Resistance	From SW3IN to GNDSW3	—	0.75	1.25	Ω
NMOS Off Leakage	SW3IN = Vinmax	—	1	5	uA
Duty Cycle Limit	Normal Mode	—	—	75	%
	Standby Mode	—	—	5	%
Note: Vin is the low side of the inductor that is connected to BP.					

6.3 Linear Regulators

As mentioned in the previous paragraph, the processor cores and memories are supposed to be supplied by the switchers. All other building blocks are supplied either directly from the battery or via a linear regulator. This paragraph lists all the general purpose linear regulators as used by the platform. For convenience these regulators are labeled to indicate their intended purpose. This concerns VRF1 and VRF2 for the transceiver transmit and receive supplies, VRFREF, VRFBG and VRFCP as the transceiver references, VRFDIG, VDIG and VGEN for the different digital sections of the platform, VIOHI, VIOLO for the different interfaces, VCAM for the camera module, VSIM1 for the SIM card, VESIM1 for the eSIM card, VMMC1 and VMCC2 for dual multimedia card support or peripheral supply such as Bluetooth PA.

A low-power standby mode controlled by the STANDBY pins is provided in which the bias current is greatly reduced. The output drive capability and performance are limited in this mode. For the standby control as well as the enable and low-power control, see Chapter 5, “Power Control System”.

Some dedicated regulators are not listed here but in their related chapters. This concerns the Audio regulator VAUDIO, see Chapter 7, “Audio”, and the USB regulators VBUS and VUSB, see Chapter 10, “Connectivity”.

Apart from the integrated linear regulators, also four generic outputs GPO1 to GPO4 are provided, intended to enable and disable discrete regulators.

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at REFATLAS. The main bandgap is supplied from VATLAS like the rest of the MC13783 core circuitry. No external DC loading is allowed at both VATLAS and REFATLAS. Table 6-11 captures the main characteristics of the core circuitry.

Table 6-11. MC13783 Core Main Characteristics

Parameter		Target
Core bias current	In Off mode	20 uA typ
VATLAS	Output voltage in ON mode	2.775 V
	Accuracy in ON mode	3%
	Output voltage in Off mode	2.45 V
	Bypass Capacitor	1 uF

Table 6-11. MC13783 Core Main Characteristics (continued)

Parameter		Target
REFATLAS	Output voltage in ON mode	1.20 V
	Output voltage in Off mode	0 V
	Absolute Accuracy	0.50%
	Temperature Drift	0.25%
	PSRR at BP = 3.0 V	90 dB
	Bypass Capacitor	100 nF

6.3.1 Regulators General Characteristics

The following applies to all linear regulators unless otherwise specified for a given circuit.

- Regulator output voltage will decrease toward zero as the current limit is exceeded. The output voltage will not sag below the specified voltage output limit with the specified maximum rated current being drawn. The current limit must be measured while remaining under the thermal limits of the package, so preferably at an input voltage of Vin = Vinmin.
- Specifications are for an ambient temperature of -30 °C to +85 °C.
- Parametric performance specifications assume the use of low ESR X5R ceramic capacitors with 20% accuracy and 15% temperature spread. Use of other types with wider temperature variation may require a larger room-temperature nominal capacitance value to meet performance specs over temperature. Especially the capacitor de-rating as a function of DC bias voltage requires special attention.
- The output voltage tolerance specified for each of the linear regulators include process variation, temperature range, static line regulation and static load regulation.
- The PSRR of the regulators is measured with the perturbating signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbated signal. During measurements care must be taken not to reach the drop out of the regulator under test.
- In the low-power mode the output performance is degraded, only those parameters listed in the low-power mode section are guaranteed. In this mode the output current is limited to much lower currents than in the active mode.
- For the lower input voltages covered only by the extended input voltage range the performance of the regulator is degraded. This means that the regulator still behaves as a regulator and will try to regulate the output voltage by turning the pass device fully on. As a result the bias current will increase and all performance parameters will be heavily degraded such as PSRR and load regulation. It is guaranteed though that no relaxation of the regulator system will occur.
- When a regulator gets disabled, the output will be pulled down to ground by an integrated pull down resistor. The pull down is also activated when RESETB goes low.

The transient load and line response are specified with the waveforms as depicted in Figure 6-5. Note that where the transient line response refers to the sum of both overshoot and DC shift, the transient load

response refers to the overshoot only, so excluding the DC shift itself. This is also valid for the mode transition response.

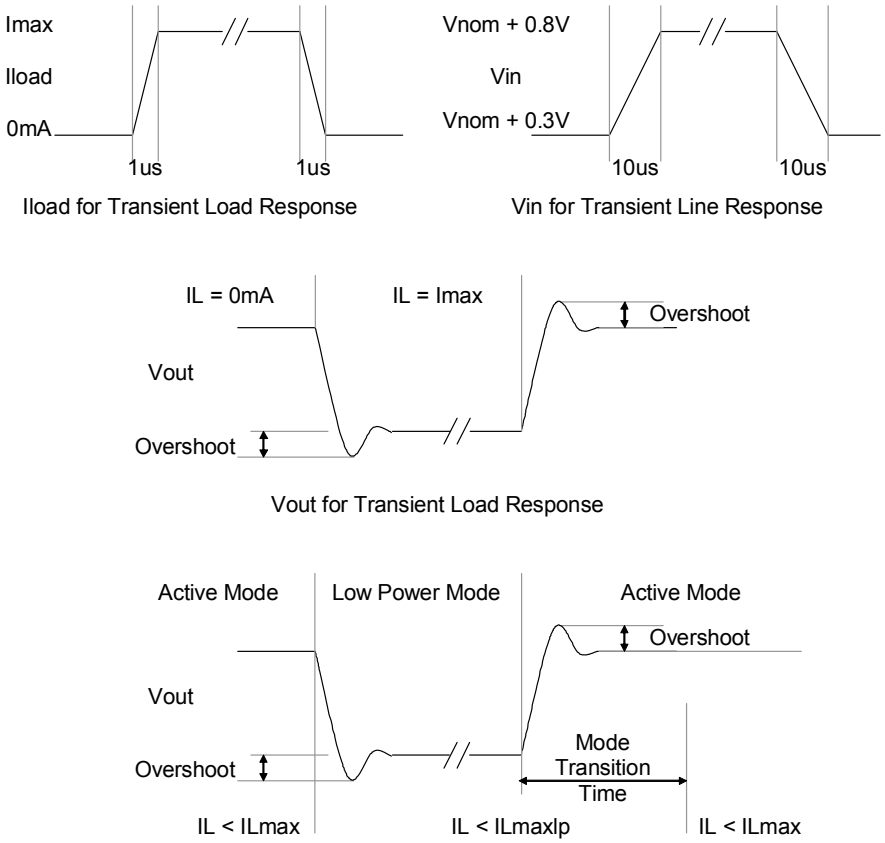


Figure 6-5. Transient Waveforms

6.3.2 Transceiver

The transceiver regulators VRF1 and VRF2 will provide isolated and low noise supplies to the transmitter and receiver. Low noise references VRFREF, VRFCP and VRFBG and a supply for the digital section VRFDIG are provided. VRFREF and VRFCP share the same input supply pin VINRFREF.

Due to the high current demands and possible significant voltage drop over VRF1 and VRF2 at high battery voltages, these are equipped with an external pass device, such as the Toshiba 2SA2056 or On Semiconductor NSL12AW. These are high gain (200-500), low VCEsat (0.2 V max.), small footprint, PNP devices. For stability reasons a small minimum ESR is required, for other non listed PNP devices stability may be obtained only after increasing the minimum ESR further or by increasing the value of the bypass capacitor, for instance a 100 mOhm ESR and 4.7 µF capacitor with the On Semiconductor MBT35200MT1. The use of external PMOS is not foreseen since no performance improvement is expected over the PNP while putting higher constraints on the regulator design. In the low-power mode for VRF1 and VRF2 an internal bypass path is used instead of the external PNP. External PNP devices are always to be connected to the BP line in the application.

Table 6-12 provides the characteristics for VRF1, VRF2, VRFREF, VRFCP and VRFBG. For digital regulators, VRFDIG, VDIG, and VGEN, see Table 6-16.

Table 6-12. VRF1, VRF2 and VRFREF Control Register Bit Assignments

Parameter	Value	Function	Iload Max.
VRF1[1:0]	00	output = 1.500 V	350 mA
	01	output = 1.875 V	350 mA
	10	output = 2.700 V	350 mA
	11	output = 2.775 V	350 mA
VRF2[1:0]	00	output = 1.500 V	350 mA
	01	output = 1.875 V	350 mA
	10	output = 2.700 V	350 mA
	11	output = 2.775 V	350 mA
VRFREF[1:0]	00	output = 2.475 V	50 mA
	01	output = 2.600 V	50 mA
	10	output = 2.700 V	50 mA
	11	output = 2.775 V	50 mA
VRFCP	0	output = 2.700 V	50 mA
	1	output = 2.775 V	50 mA

Table 6-13. Transmitter and Receiver Regulators VRF1 and VRF2 Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	—	Vnom + 0.25	—	4.65	V
Operating Current Load Range ILmin to ILmax	—	0	—	350	mA
Extended Input Voltage Range	Performance will be out of specification for output levels >2.4	2.5	—	4.65	V
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	2.2	+35%	uF
Bypass Capacitor ESR	10 kHz – 1 MHz	20	—	100	mΩ
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	—	—	—	—
	VRF1[1:0] = 00, 01, 10 VRF2[1:0] = 00, 01, 10	Vnom - 3%	Vnom	Vnom + 3%	V
	VRF1[1:0] = 11 VRF2[1:0] = 11	Vnom - 3%	Vnom	Vnom + 2%	V

Table 6-13. Transmitter and Receiver Regulators VRF1 and VRF2 Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Load Regulation	1 mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Base Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	5	—	10	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	30	45	uA
Low-Power Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	Vnom - 3%	Vnom	Vnom + 3%	V
Current Load Range ILminlp to ILmaxlp	—	0	—	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	55	60	—	dB
Output Noise	Vin = Vinmin IL = ILmax	—	—	—	—
	100 Hz – 1 kHz	—	—	-115	dBV/vHz
	1 kHz – 10 kHz	—	—	-126	dBV/vHz
	10 kHz – 1 MHz	—	—	-132	dBV/vHz
Spurs	32.768 kHz and harmonics	—	—	-120	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV

Table 6-13. Transmitter and Receiver Regulators VRF1 and VRF2 Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	100	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

Table 6-14. Reference Regulators VRFREF, VRFCP Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	—	2.5 < Vnom + 0.25	—	4.65	V
Operating Current Load Range ILmin to ILmax	—	0	—	50	mA
Extended Input Voltage Range	Performance may be out of specification	2.5		4.65	V
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	1.0	+35%	uF
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω
Active Mode – DC Only for 2.475, 2.7, 2.775 V steps					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom - 3%	Vnom	Vnom + 3%	V
Load Regulation	1 mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.25	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	100		150	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	uA
Low-Power Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	—	—	—	—
	VRFCP= 0, 1	Vnom - 3%	Vnom	Vnom + 3%	V
	VRFREF[1:0] = 00, 01, 10	Vnom - 3%	Vnom	Vnom + 3%	V
	VRFREF[1:0] = 11	2.700	2.775	2.850	V

Table 6-14. Reference Regulators VRFREF, VRFCP Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Current Load Range ILminlp to ILmaxlp		0	—	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	55	60	—	dB
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100 Hz – 1 kHz	—	20	—	dB/dec
	1 kHz – 1 MHz	—	—	0.2	uV/√Hz
Spurs	32.768 kHz and harmonics	—	—	-85	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	100	us
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	10	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

The VRFBG is a bandgap reference with very low noise and temperature drift used as a trimmed reference by the transceiver. The loading at this reference is therefore very small. VRFBG can be enabled and disabled via the standby pins, but it cannot be put in a low-power mode. VRFBG is supplied internally from VATLAS.

Table 6-15. VRFBG Main Characteristics

Parameter	Target
Output voltage	1.200 V
Bias Current	20 uA
Max Load Current	100 uA
Absolute Accuracy	0.50%
Temperature Drift	0.25%
PSRR at BP = 3.0 V	90 dB
Noise at 600 kHz	10 nVrms/√Hz
Bypass Capacitor	100 nF

6.3.3 Digital

The different digital sections in the platform need a dedicated supply in order to isolate them from the analog sections. For some digital sections the I/O regulators may be used. Table 6-16 provides the characteristics for VDIG, VGEN, and VRFDIG.

Table 6-16. VRFDIG, VDIG and VGEN Control Register Bit Assignments

Parameter	Value	Function	Iload Max.
VRFDIG[1:0]	00	output = 1.20 V	150 mA
	01	output = 1.50 V	150 mA
	10	output = 1.80 V	200 mA
	11	output = 1.875 V	200 mA
VDIG[1:0]	00	output = 1.20 V	150 mA
	01	output = 1.30 V	150 mA
	10	output = 1.50 V	200 mA
	11	output = 1.80 V	200 mA
VGEN[2:0]	000	output = 1.20 V	150 mA
	001	output = 1.30 V	150 mA
	010	output = 1.50 V	200 mA
	011	output = 1.80 V	200 mA
	100	output = 1.10 V	150 mA
	101	output = 2.00 V	200 mA
	110	output = 2.775 V	200 mA
	111	output = 2.40 V	200 mA

Table 6-17. Digital Regulators VRFDIG, VDIG and VGEN Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	VGEN[2:0]=100	Vnom + 0.4	—	4.65	V
	All other set points	Vnom + 0.3	—	4.65	V
Operating Current Load Range ILmin to ILmax	Vout < 1.50 V Vout>= 1.50 V	0	—	150 200	mA
Extended Input Voltage Range	Performance may be out of specification	—	—	—	—
	Battery Supplied	2.5	—	4.65	V
	Switcher Supplied	Vnom	—	4.65	V
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	2.2	+35%	uF
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	—	—	—	—
	Vnom > 1.6 V	Vnom - 3%	Vnom	Vnom + 3%	V
	Vnom ≤ 1.6 V	Vnom - 0.05	Vnom	Vnom + 0.05	V
Load Regulation	1mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	300	—	600	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	uA
Low-Power Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	—	—	—	—
	Vnom > 1.6 V	Vnom - 3%	Vnom	Vnom + 3%	V
	Vnom ≤ 1.6 V	Vnom - 0.05	Vnom	Vnom + 0.05	V
Current Load Range ILminlp to ILmaxlp		0	—	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					

Table 6-17. Digital Regulators VRFDIG, VDIG and VGEN Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	50	60	—	dB
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100 Hz – 1 kHz	—	20	—	dB/dec
	1 kHz – 1 MHz	—	—	1	uV/√Hz
Spurs	32.768 kHz and harmonics	—	—	-100	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	10	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

6.3.4 Interface

In total, two dedicated I/O supplies are provided, a high level VIOHI and a low level VIOLO. The input VINIOHI is always to be connected to BP, even if the VIOHI regulator is not used by the system. The input VINIOLO may run off of BP or one of the buck switchers.

Table 6-18. VIOHI and VIOLO Control Register Bit Assignments

Parameter	Value	Function	Iload Max.
VIOHI		output = 2.775 V	200 mA

Table 6-18. VIOHI and VIOLO Control Register Bit Assignments (continued)

Parameter	Value	Function	Iload Max.
VIOLO<1:0>	00	output = 1.20 V	150 mA
	01	output = 1.30 V	150 mA
	10	output = 1.50 V	200 mA
	11	output = 1.80 V	200 mA

Table 6-19. I/O High Level Regulator VIOHI Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	—	Vnom + 0.3	—	4.65	V
Operating Current Load Range ILmin to ILmax	—	0	—	200	mA
Extended Input Voltage Range	Performance may be out of specification	2.5	—	4.65	V
	Output voltage stays within 50 mV accuracy	Vnom+0.2	—	4.65	V
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	1.0	+35%	uF
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom - 3%	Vnom	Vnom + 3%	V
Load Regulation	1mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	300	—	600	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	uA
Low-Power Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	Vnom - 3%	Vnom	Vnom + 3%	V
Current Load Range ILminlp to ILmaxlp		0	—	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					

Table 6-19. I/O High Level Regulator VIOHI Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	50	60	—	dB
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100 Hz – 1 kHz	—	20	—	dB/dec
	1 kHz – 1 MHz	—	—	1	uV/√Hz
Spurs	32.768 kHz and harmonics	—	—	-100	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	10	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

Table 6-20. I/O Low Level Regulators VIOLO Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax		Vnom + 0.3	—	4.65	V
Operating Current Load Range ILmin to ILmax	Vout < 1.50 V Vout>= 1.50 V	0	—	150 200	mA

Table 6-20. I/O Low Level Regulators VIOLO Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Extended Input Voltage Range	Performance may be out of specification	—	—	—	—
	Battery Supplied	2.5	—	4.65	V
	Switcher Supplied	Vnom	—	4.65	V
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	2.2	+35%	uF
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	—	—	—	—
	Vnom > 1.6 V	Vnom - 3%	Vnom	Vnom + 3%	V
	Vnom ≤ 1.6 V	Vnom - 0.05	Vnom	Vnom + 0.05	V
Load Regulation	1 mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	300	—	600	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	uA
Low-Power Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	—	—	—	—
	Vnom > 1.6 V	Vnom - 3%	Vnom	Vnom + 3%	V
	Vnom ≤ 1.6 V	Vnom - 0.05	Vnom	Vnom + 0.05	V
Current Load Range ILminlp to ILmaxlp	—	0	—	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	55	60	—	dB

Table 6-20. I/O Low Level Regulators VIOLO Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100 Hz – 1 kHz	—	20	—	dB/dec
	1 kHz – 1 MHz	—	—	1	uV/√Hz
Spurs	32.768 kHz and harmonics	—	—	-100	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	10	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

6.3.5 Camera

The camera module is supplied by the regulator VCAM. This allows powering down the entire module independent of the rest of the application. In applications with a dual camera it is supposed only one of the two cameras is active at a time. The input VINCAM is always to be connected to BP, even if the VCAM regulator is not used by the system.

Table 6-21. VCAM Control Register Bit Assignments

Parameter	Value	Function	Iload Max.
VCAM[2:0]	000	output = 1.50 V	150 mA
	001	output = 1.80 V	150 mA
	010	output = 2.50 V	150 mA
	011	output = 2.55 V	150 mA
	100	output = 2.60 V	150 mA
	101	output = 2.75 V	150 mA
	110	output = 2.80 V	150 mA
	111	output = 3.00 V	150 mA

Table 6-22. Camera Regulator VCAM Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	—	2.5 < Vnom + 0.25	—	4.65	V
Operating Current Load Range ILmin to ILmax	—	0	—	150	mA
Extended Input Voltage Range	Performance may be out of specification	2.5	—	4.65	V
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	2.2	+35%	uF
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	—	—	—	—
	Vnom > 1.6V	Vnom - 3%	Vnom	Vnom + 3%	V
	Vnom ≤ 1.6V	Vnom - 0.05	Vnom	Vnom + 0.05	V
Load Regulation	1mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	300	—	600	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	uA
Low-Power Mode - DC					

Table 6-22. Camera Regulator VCAM Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	—	—	—	—
	Vnom > 1.6 V	Vnom - 3%	Vnom	Vnom + 3%	V
	Vnom ≤ 1.6 V	Vnom - 0.05	Vnom	Vnom + 0.05	V
Current Load Range ILminlp to ILmaxlp		0	—	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	50	60	—	dB
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100 Hz – 1 kHz	—	20	—	dB/dec
	1 kHz – 1 MHz	—	—	1	uV/√Hz
Spurs	32.768 kHz and harmonics	—	—	-100	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	10	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

6.3.6 SIM

The SIM card is supplied on demand by VSIM, where the eSIM card is supplied by VESIM. The interface to the SIM section on the processor is supplied from this regulator as well, which avoids the use of level shifters. The VSIM regulator can be enabled via the SIMEN pin and VESIM via the ESIMEN pin for latency free control. Since this enable signal is generated by the processor, this pin is to be supplied not in the same SIM module domain but in a general purpose I/O domain. For processors where this is not the case, additional circuitry will have to be added or, in a single SIM card application, VESIM can be used for permanently supplying the processor while using VSIM for the SIM card. VSIM and VESIM share the same input supply pin VINSIM.

By default, the SIM and ESIM regulators can only enabled via the corresponding enable pin if the respective VSIMEN and VESIMEN bit are set (so both the bit and the pin have to be high to enable the regulator). When VESIM is not assigned to the ESIMEN pin this regulator can be enabled via SPI only, see also Section 6.4, “Supply Control”, on page 6-33. Like for the other regulators, the read back of the VESIMEN and VESIMMODE bits reflect the actual state of the regulator, see Chapter 5, “Power Control System”, so including the influence of the ESIMEN pin. For the VSIM regulator bits however, the readback does not take into account the state of the SIMEN pin.

Table 6-23. VSIM and VESIM Control Register Bit Assignments

Parameter	Value	Function	Iload Max.
VSIM	0	output = 1.80 V	60 mA
	1	output = 2.90 V	60 mA
VESIM	0	output = 1.80 V	60 mA
	1	output = 2.90 V	60 mA

Table 6-24. Card Regulators VSIM and VESIM Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage range Vinmin to Vinmax	2.9 V Setting	3.1	3.6	4.65	V
	1.8V Setting	2.5	3.6	4.65	V
Operating Current Load Range ILmin to ILmax	VSIM	0	—	60	mA
	VESIM	0	—	80	mA
Min Bypass Capacitor Value	Used as a condition for all other parameters	-35%	1.0	+35%	uF
Bypass Capacitor ESR	10 kHz – 1 MHz	0	—	0.1	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom – 3%	Vnom	Vnom + 3%	V
Load Regulation	1 mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.40	mV/mA

Table 6-24. Card Regulators VSIM and VESIM Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Line Regulation	Vinmin < Vin < Vinmax For IL = 1 mA For any ILmin < IL < ILmax	—	2	5	mV
		—	5	8	
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	120	—	180	mA
Active mode quiescent current	Vinmin < Vin < Vinmax IL = 0	—	20	25	uA
Disabled mode leakage current	Vinmin < Vin < Vinmax Enable=0 / IL = 0	—	—	0.1	uA
Low-Power Mode – DC					
Output Voltage Vout (Accuracy)	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	Vnom – 50 mV	Vnom	Vnom + 50 mV	V
Current Load Range ILminlp to ILmaxlp	—	0	1	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					
PSRR	IL = 75% of Ilmax 20 Hz to 20 kHz Vin = Vinmin + 100 mV	35	40	—	dB
	IL =10 mA 20 Hz to 24 kHz Vin = 3.6 V	40	45	—	dB
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100 Hz – 1 kHz	—	20	—	dB/dec
	1 kHz – 1 MHz	—	—	1	uV/√Hz
Spurs	32.768 kHz and harmonics	—	—	-100	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax 0 < IL < ILmax	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax / IL = 0	0.1	—	5	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax / IL = 0	—	1	2	%
Transient Load Response	0 to ILmax / ILmax to 0 in 1us Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	Vnom+0.3 V to Vnom+0.8 V in 10 us Vnom+0.8 V to Vnom+0.3 V in 10 us IL = 75% of ILmax	—	5	8	mV

Table 6-24. Card Regulators VSIM and VESIM Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	10	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

6.3.7 MMC

The MMC card can be either a hot swap MMC or SD card or an extension module. The supply capability must therefore be significant. To avoid a too high dissipation on-chip, the pass device is therefore kept externally. Like for VRF2 and VRF1 the Toshiba 2SA2056 is used. For stability reasons a small minimum ESR is required, for other non listed PNP devices stability may be obtained only after increasing the minimum ESR further or by increasing the value of the bypass capacitor. The external PNP device is always connected to the BP line in the application. VMMC1 and VMMC2 can also be used to supply other peripherals like a Bluetooth or WLAN. VMMC1 and VMMC2 can be enabled via the ESIMEN pin, see Section 6.4, “Supply Control”, on page 6-33.

Table 6-25. VMMC1 and VMMC2 Control Register Bit Assignments

Parameter	Value	Function on	Iload Max.
VMMC1[2:0]	000	output = 1.60 V	350 mA
	001	output = 1.80 V	350 mA
	010	output = 2.00 V	350 mA
	011	output = 2.60 V	350 mA
	100	output = 2.70 V	350 mA
	101	output = 2.80 V	350 mA
	110	output = 2.90 V	350 mA
	111	output = 3.00 V	350 mA

Table 6-25. VMMC1 and VMMC2 Control Register Bit Assignments (continued)

Parameter	Value	Function on	Iload Max.
VMMC2[2:0]	000	output = 1.60 V	350 mA
	001	output = 1.80 V	350 mA
	010	output = 2.00 V	350 mA
	011	output = 2.60 V	350 mA
	100	output = 2.70 V	350 mA
	101	output = 2.80 V	350 mA
	110	output = 2.90 V	350 mA
	111	output = 3.00 V	350 mA

Table 6-26. Smart Card Regulators VMMC1 and VMMC2 Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	—	2.5 < Vnom + 0.25	—	4.65	V
Operating Current Load Range ILmin to ILmax	—	0	—	350	mA
Extended Input Voltage Range	Performance will be out of specification for output levels >2.4	2.5	—	4.65	V
Minimum Bypass Capacitor Value	Used as a condition for all other parameters	-35%	2.2	+35%	uF
Bypass Capacitor ESR	10 kHz – 1 MHz	20	—	100	mΩ
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom - 3%	Vnom	Vnom + 3%	V
Load Regulation	1mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Base Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	5	—	10	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	30	45	uA
Low-Power Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	Vnom - 3%	Vnom	Vnom + 3%	V
Current Load Range ILminlp to ILmaxlp	—	0	—	3	mA

Table 6-26. Smart Card Regulators VMMC1 and VMMC2 Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	55	60	—	dB
Output Noise	Vin = Vinmin IL = ILmax	—	—	—	—
	100 Hz – 1 kHz	—	—	-115	dBV/vHz
	1 kHz – 10 kHz	—	—	-126	dBV/vHz
	10 kHz – 1 MHz	—	—	-132	dBV/vHz
Spurs	32.768 kHz and harmonics	—	—	-120	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Mode Transition Time	See waveform From low-power to active Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	100	us
Mode Transition Response	See waveform From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

6.3.8 Vibrator Motor Driver

The VVIB regulator drives a vibrator motor for alert functions. Since the vibrator motor will present an equivalent load capacitance of 1nF, no additional external bypass capacitor is required for this output. The input VINVIB is always to be connected to BP, even if the VVIB regulator is not used by the system. The

vibrator regulator is enabled when the SPI bit VVIBEN is set. When the bit VIBPINCTRL is set to a 1, the VVIB regulator can also be enabled by pulling the VIBEN pin high. Table 6-27 summarizes this behavior.

Table 6-27. VVIB Enabling Logic

Bit VVIBEN (Write)	Bit VIBPINCTRL	Pin VIBEN	Regulator VVIB[1]	Bit VVIBEN (Read)
0	0	X	Off	0
0	1	0	Off	0
0	1	1	On	1
1	X	X	On	1

[1] In case of dual SPI control over VVIB, the highest power mode is selected.

Table 6-28. VVIB Control Register Bit Assignments

Parameter	Value	Function	Iload Max.
VVIB[1:0]	00	output = 1.30 V	200 mA
	01	output = 1.80 V	200 mA
	10	output = 2.00 V	200 mA
	11	output = 3.00 V	200 mA

Table 6-29. Vibrator Motor Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range	Highest Setting	3.3	—	4.65	V
Vinmin to Vinmax	Other Settings	3.1	—	4.65	V
Operating Current Load Range ILmin to ILmax	Other Settings	10	—	200	mA
Extended Input Voltage Range	Performance may be out of specification	2.5	—	4.65	V
Bypass Capacitor Value	Presented by Vibrator motor	—	1	—	nF
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	1.23 1.72 1.91 2.88	1.30 1.80 2.00 3.00	1.34 1.85 2.06 3.09	V
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	360	—	600	mA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 1 kHz	—	—	—	—
	Vin = 3.6 V	20	—	—	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	0.5	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	—	—	10	ms

6.4 Supply Control

6.4.1 Power Gating

For reduced current drain in low-power modes, parts of a processor may be power gated, that is to say, the supply to that part of the processor is disabled. To simplify the supply tree and to reduce the number of external components while maintaining flexibility, power gate switch drivers are included.

The power gate switch drivers consist of a fully integrated charge pump which provides a low-power output to drive the gate of external NFETs (for example, Fairchild FDZ298N) placed between a power supply and the processor. A total of two outputs are provided, driven by the power gate enable inputs or via the power gate enable SPI bits PWGTxSPIEN shown in Table 6-30. The read back of the PWGTxSPIEN bits reflects the actual state of PWGTxDRV pin. The power control state machine does influence the behavior of the power gating notably at start up and the user off and memory hold modes, see the Section 5.4, “Memory Hold” in Chapter 5, “Power Control System”.

Table 6-30. Power Gating Logic

Bit PWGTxSPIEN 0 = default	Pin PWGTxEN	PWGTxDRV	Read Back PWGTxSPIEN
1	X	Low	0
0	0	High	1
0	1	Low	0
Note: Applicable for Watchdog, On and User off Wait modes only. If PWGT1SPIEN=PWGT2SPIEN =1 then the charge pump is disabled.			

The charge pump system makes use of the available battery voltage for precharge and a combination of low and high frequency clocking in order to obtain fast turn on times while keeping the power consumption low.

To inform the processor that the power gate is fully conducting, meaning PWGTxDRV is above the power gating ready threshold, a power ready signal is generated. When enabling two outputs at the same time, the power ready signal is only generated when both outputs are above this threshold. See Chapter 5, "Power Control System" for more details on the power ready signal.

Figure 6-6 depicts the power gating function with the NMOS placed such that a part of a processor supply can be isolated from the switcher with the switcher being active. When using power gating for power cut operation, source and drain of the NMOS must be inverted, see Chapter 5, "Power Control System".

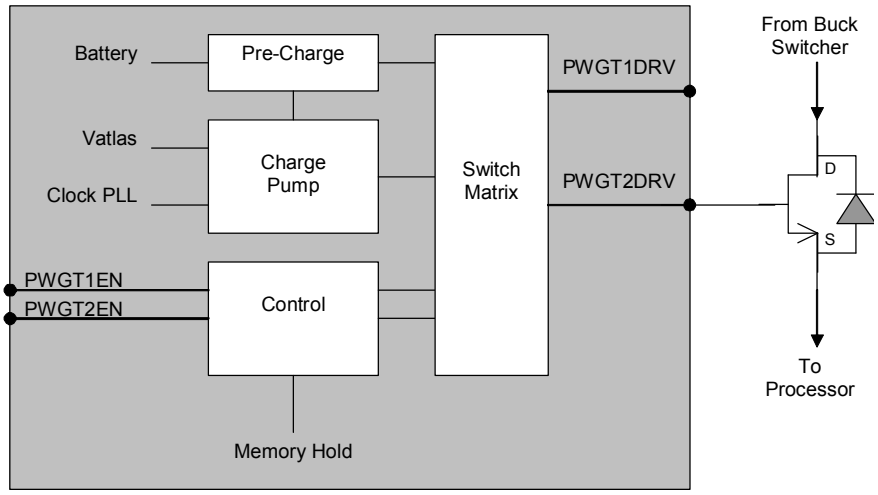


Figure 6-6. Power Gating Diagram

Table 6-31. Power Gating Characteristics

Parameter	Condition	Min	Typ	Max	Units
Output Voltage Vout	Output High	5.0	5.40	5.70	V
	Output Low	—	—	100	mV

Table 6-31. Power Gating Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Turn-on Time	Enable to Vout = Voutmin – 250 mV	—	—	—	—
	1 Output at a time, non overlapping enables	—	50	100	us
	1 Output at a time, overlapping enables	—	—	250[1]	us
	2 Outputs at the same time	—	—	200	us
Power Gating Ready Threshold	Enable to PWRRDY goes high	4.60	4.80	5.00	V
Turn Off Time	Disable to Vout < 1 V	—	—	1	us
Average Bias Current	t > 500 us after Enable	—	1	5	uA
Transient Voltage Slump	Enable an additional output while the other output is active	—	—	250	mV
Processor Supply Voltage		0.8	—	3.0	V
DC Load Current	Per output	—	—	100	nA
Load Capacitance[2]	Used as a condition for the other parameters	0.5	—	1.0	nF

1 To avoid undesired pulses on the power ready signal when two power gates are used, do not enable and/or disable a channel for periods shorter than this maximum turn on time.

2 Larger values will lead to longer turn on times exceeding the given limits, smaller values will lead to larger ripple at the output.

Table 6-32. Power Gating Bits

PWGT1SPIEN	Power gate 1 enable
PWGT2SPIEN	Power gate 2 enable

6.4.2 General Purpose Outputs

In some applications the need for regulators will exceed the number of regulators available on the MC13783. In order to provide a seamless control over these regulators, four general purpose outputs GPO1, GPO2, GPO3, GPO4 are provided at a VIOHI logic high level. The outputs are to be connected to the enable line of a discrete regulator. The enable bits for the outputs reside in the regulator control register. Like the embedded regulators, the GPOx outputs can be controlled by the standby pins.

Table 6-33. General Purpose Outputs Bits

GPO1EN	General Purpose Output 1 enable
GPO2EN	General Purpose Output 2 enable
GPO3EN	General Purpose Output 3 enable
GPO4EN	General Purpose Output 4 enable
GPO1STBY	GPO1 controlled by standby
GPO2STBY	GPO2 controlled by standby
GPO3STBY	GPO3 controlled by standby
GPO4STBY	GPO4 controlled by standby

Table 6-34. General Purpose Outputs Standby Control

GPOxEN	GPOxSTBY	STANDBY Pin	Output GPOx
0	X	X	Low
1	0	X	High
1	1	0	High
1	1	1	Low

6.4.3 External Enables

The REGEN pin allows to enable or disable one or more regulators and switchers of choice. The REGEN function can be used in two ways. It can be used as a regulator enable pin like with SIMEN where the SPI programming is static and the REGEN pin is dynamic. It can also be used in a static fashion where REGEN is maintained high while the regulators get enabled and disabled dynamically via SPI. In that case REGEN functions as a master enable.

The polarity of the REGEN pin is programmable with the REGENINV bit, when set to “0” it is active high, when set to a “1” it is active low. The REGEN function is only available in the active modes (Watchdog, On and User Off Wait), its state is ignored in any other mode. The REGEN does not overrule the mode selection or standby function. Only the primary SPI has access to the REGEN mapping. No sequencing of regulators will occur, all regulators and switchers enabled via REGEN are enabled without further delay.

The ESIMEN pin allows to enable VESIM, VMMC1, and VMMC2 by assigning these regulators to the ESIMEN pin by setting the VESIMESIMEN (Defaults to 1), VMMC1ESIMEN, and VMMC2ESIMEN bits. By default the VESIM is assigned to the ESIMEN pin. When ESIMEN is assigned to VESIM, both the VESIMEN bit and the ESIMEN pin have to be high to enable VESIM. In case ESIMEN is no longer assigned to VESIM, then the VESIM regulator can be enabled by setting the VESIMEN bit only. The same counts for VMMC1 and VMMC2.

Table 6-35. ESIMEN Pin Enable Function Logic

VxEN	VxESIMEN	ESIMEN pin	Regulator Vx
0	X	X	Off
1	0	X	Active[1]
1	1	0	Off
1	1	1	Active[1]

[1] On / Low-Power / Off determined by VxMODE, VxSTBY and STANDBY pin. Vx stands for VESIM, VMMC1, VMMC2.

6.4.4 SPI Register Summary

See individual paragraphs in this chapter, Chapter 5, “Power Control System” and Chapter 13, “SPI Bitmap.”

Chapter 7
Audio

7.1 Dual Digital Audio Bus

7.1.1 Interface

The MC13783 is equipped with two independent digital audio busses. Both busses consist of a bit clock, word clock, receive data and transmit data signal lines. Both busses can be redirected to either the voice CODEC or the stereo DAC and can be operated simultaneously. In addition to the afore mentioned signal lines, two system clock inputs are provided which can be selected to drive the voice CODEC or the stereo DAC. In the latter case a PLL is used to generate the proper internal frequencies. During simultaneous use of the both busses, two different system clocks can be selected by the voice CODEC and the stereo DAC.

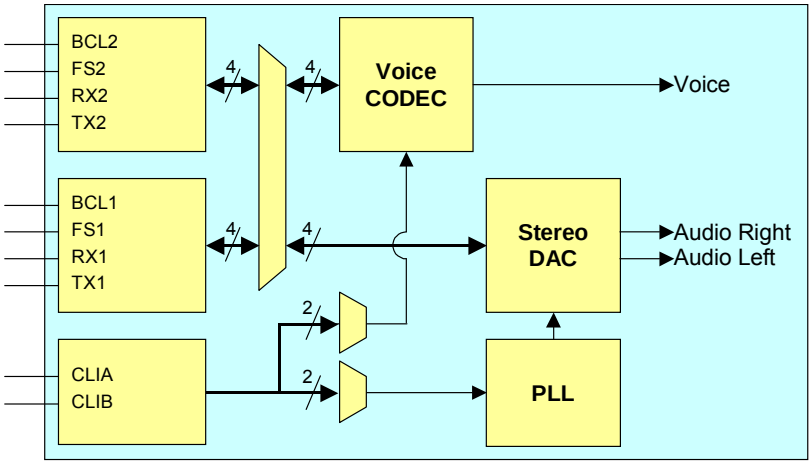


Figure 7-1. Dual Digital Audio Bus Interface

The audio bus interface with suffix 1 is intended to be connected to the applications processor and is default routed to the stereo DAC. The audio bus with suffix 2 is then connected to the call processor and is default routed to the voice CODEC. The I/O level for audio bus 1 is PRIVCC and for audio bus 2 SECVCC. The CLIA and CLIB clock inputs are AC coupled and internally sliced with an input level tolerant up to VAUDIO. There is no notion of priority between both busses at a MC13783 level so are completely interchangeable.

The clock input to the telephone CODEC and the stereo DAC is a direct-coupled, sinusoidal signal from CLI (or may be an arbitrary waveform from CLI with a duty cycle of 40/60 or better, such as a triangle wave). CLI is rising edge triggered. CLI must always be present unless the telephone CODEC and stereo DAC cores are reset or powered down and all audio outputs are disabled.

Table 7-1. CLKIN Input Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
CLIA/B Frequency	—		1.0	—	33.6	MHz
CLIA/B Duty Cycle	—		40	—	60	%
CLIA/B AC Level	—		300	—	VAUDIO	mV_{PP}
CLIA/B Jitter[1]	For stereo DAC use	White Noise	—	—	900	ps_{RMS}
		1 kHz Modulated	—	—	200	ps_{RMS}
	For Voice CODEC use	White Noise	—	—	100	ps_{RMS}

1 Higher jitter levels will raise the noise floor of the convertors and as a result reduce the dynamic range.

Table 7-2. Logic I/O Specifications

Parameter	Condition	Min	Typ	Max	Units
Input High BCL1, FS1, RX1	—	0.7*PRIVCC	—	PRIVCC	V
Input Low BCL1, FS1, RX1	—	0	—	0.3*PRIVCC	V
Input High BCL2, FS2, RX2	—	0.7*SECVCC	—	SECVCC	V
Input Low BCL2, FS2, RX2	—	0	—	0.3*SECVCC	V
Output Low BCL1, FS1, TX1	Output sink 100 uA	0	—	0.2	V
Output High BCL1, FS1, TX1	Output source 100 uA	PRIVCC-0.2	—	PRIVCC	V
Output Low BCL2, FS2, TX2	Output sink 100 uA	0	—	0.2	V
Output High BCL2, FS2, TX2	Output source 100 uA	SECVCC-0.2	—	SECVCC	V

7.1.2 Voice CODEC Protocol

The serial interface protocol for the voice CODEC can be used in master and in slave mode. In both modes it can operate with a short or a long frame sync and data is transmitted and received in a two's compliment format.

In slave mode and with CDCFS[1:0]=01 or 10, after a rising edge, the FS pin must be held high for at least one falling BCL edge. The PCM data word is then made available on the TX pin, beginning with the following rising edge of BCL. Data is transmitted beginning with the MSB. Since the CODEC is 13 bits, the last three bits are zero. To allow multiple devices to be connected to the audio bus, each occupying an assigned time slot, the LSB for transmit occupies only half a BCL period to avoid a bus conflict around the next following rising edge of BCL. The TX output will then remain high impediment until the beginning of the MSB of the next data word.

In case of multiple devices on the bus, the MC13783 TX and RX will by default occupy the first time slot. However, the TX and RX can be assigned together to one of the other time slots 2, 3 and 4 by SPI programming for a more flexible use of the network mode. The bit clock provided must be sufficiently high to support the number of desired time slots.

When the second ADC channel is activated, the second channel TX data is to be transmitted in a different time slot then the first channel. In case the second ADC channel is not active, the TX data will contain all zero's. In this specific case, the second channel can be assigned to the same slot as the first channel without affecting the data in the first channel. The second channel TX data can be assigned to any of the remaining slots. There is no RX data associated to this.

The receive data on RX from two time slots can be added, see the audio port mixing section.

After the CODEC has been enabled (CDCEN=1), and with CDCFS[1:0]=01 or 10, receive data will be valid only after the first falling edge of FS. If FS is then high for at least one falling edge of BCL, then the MC13783 will start latching the 16bit serial word into the receive data input on the following 16 falling edges of BCL. The MC13783 will count the BCL cycles and transfer the PCM data word to the D/A converter on the rising BCL edge after the LSB has been latched. Since the CODEC is 13 bits, the last three received bits of the 16 are a don't care.

Figure 7-2 depicts behavior described above.

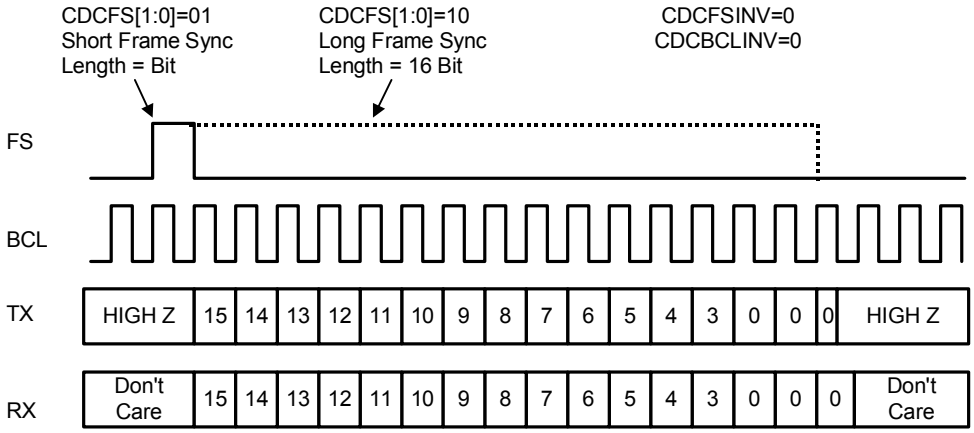


Figure 7-2. Voice CODEC Timing Diagram Example 1

When the voice CODEC is in slave mode, the FS input must remain synchronous to the CLI frequency.

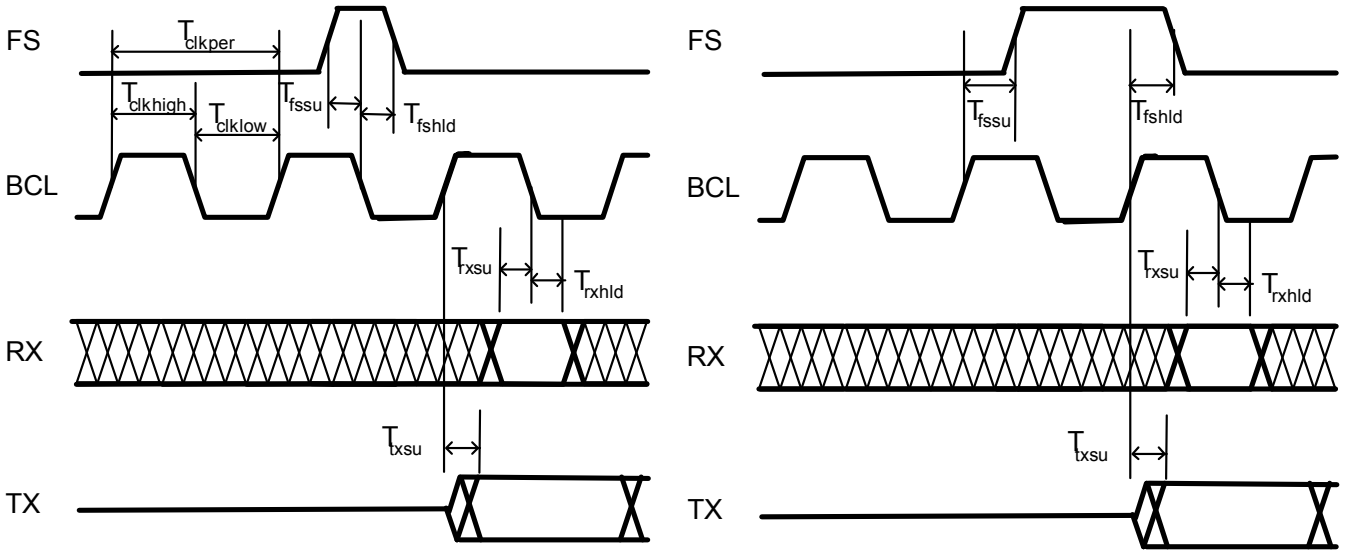


Figure 7-3. Audio Interface Timing Diagram

Table 7-3. Audio Interface Timing Specifications

Parameter	Description	Min T (ns)	Max T (ns)
T_{fssu}	Period FS has to be active before the latching edge of BCL (slave)	20	—
	Period after which FSYNC will be stable after the non latching edge of BCL (master)	—	20
T_{fshld}	Period FS has to remain active after the latching edge of BCL (slave)	20	—
	Period after which FSYNC will be stable after the latching edge of BCL (master)	—	20
T_{fsdly}	Additional FS delay when CDCFSDLY=1	15	40
T_{clkper}	Clock period of BCL[1]	325	—
$T_{clkhigh}$	Part of the clock period where BCL has to remain high	130	—
T_{clklow}	Part of the clock period where BCL has to remain low	130	—
T_{rxsu}	Period RX has to be stable before the next latching edge of BCL	20	—
T_{rxhld}	Period RX has to remain stable after the latching edge of BCL	30	—
T_{txsu}	Period after which TX will be stable after the non latching edge of BCL	—	100

[1] Equivalent to a maximum bit clock frequency of 3.072 MHz.

Some processors rely on the framesync arriving at the same time or being slightly delayed with respect to the bit clock. In practical phone board layouts the delay on the clock lines may not be matched and the framesync may accidentally arrive before the bit clock causing audible issues. In such cases the CDCFSDLY bit can be set to a 1 which will delay the framesync of the SSI used by the Voice CODEC. If set to a 0 (default), no delay is applied.

The previously described behavior in slave mode is also applicable for the master mode except that now all clocks are internally generated based on the CLI signal. The MC13783 will not use a PLL but only dividers, so depending on the number of time slots and CLI frequency used, the BCL will not always be

an integer multiple of FS. However, since the devices on the bus will count only the bits in their assigned time slot, this will not cause a practical issue. When operating the MC13783 in a master mode it will always provide 4 time slots.

Additional programmability of the interface for both master and slave mode include bus protocol selection via CDCFS[1:0], see Table 7-4, and FS and BCL inversion. There is also the possibility to activate the clocking circuitry independent from the voice CODEC.

Table 7-4. Voice CODEC Bus Protocol Selection

CDCFS[1:0][1]	FS	Offset	Protocol Use[2]
00	Long	0	Not supported
01	Short	-1	Network
10	Long	-1	I2S[3]
11	Short	0	Not supported

1 Assignment equivalent to Stereo DAC bus protocol setting via STDCFS[1:0].

2 FS and BCL inversion have to be set separately.

3 At least 64 BCL clocks are generated per FS, only the first 32 clocks are used in I2S.

Figure 7-4 gives an example with the MC13783 in Master Mode (CDCSM=0), CLI at 13 MHz, a long inverted FS (CDCFSINV=1) with a -1 offset (CDCFS[1:0]=10), BCL Inverted (CDCBCLINV=1), and the TX and RX in time slot 0 (CDCTXRXSLOT[1:0]=00). As the diagram shows, the setting of the CDCFSINV bit for a long framesync is different than for the stereo DAC bit STDCFSINV. For a short framesync though it will work the same.

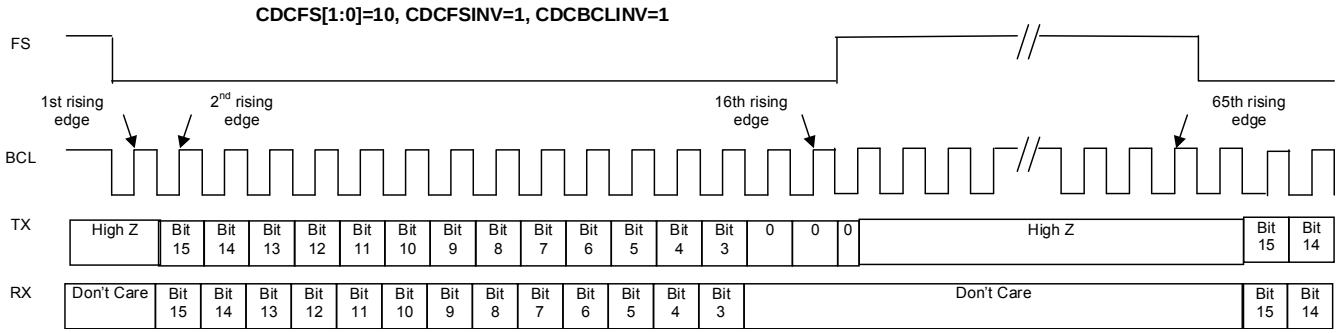


Figure 7-4. Voice CODEC Timing Diagram Example 2

7.1.3 Stereo DAC Protocol

The serial interface protocol for the stereo DAC supports the industry standard MSB justified mode and an I2S mode. In industry standard mode, FS will be held high for one 16-bit data word and low for the next 16 bits. I2S mode is similar to industry standard mode except that the serial data is delayed one BCL period. Data is received in a two's compliment format.

A network mode is also available where the stereo DAC will operate in its assigned time slot. A total of maximum 4 time slot pairs are supported depending on the settings of the clock speed. In this case, the sync signal is no longer a word select but a short frame sync.

In all modes, the polarity of both FS and BCL is programmable by SPI. There is also the possibility to activate the clocking circuitry independent from the stereo DAC.

Table 7-5. Stereo DAC Bus Protocol Selection

STDCCFS[1:0]	FS	Offset	Protocol Use[1]
00	Long	0	Normal
01	Short	-1	Network
10	Long	-1	I2S
11	Short	0	—

1 FS and BCL inversion have to be set separately.

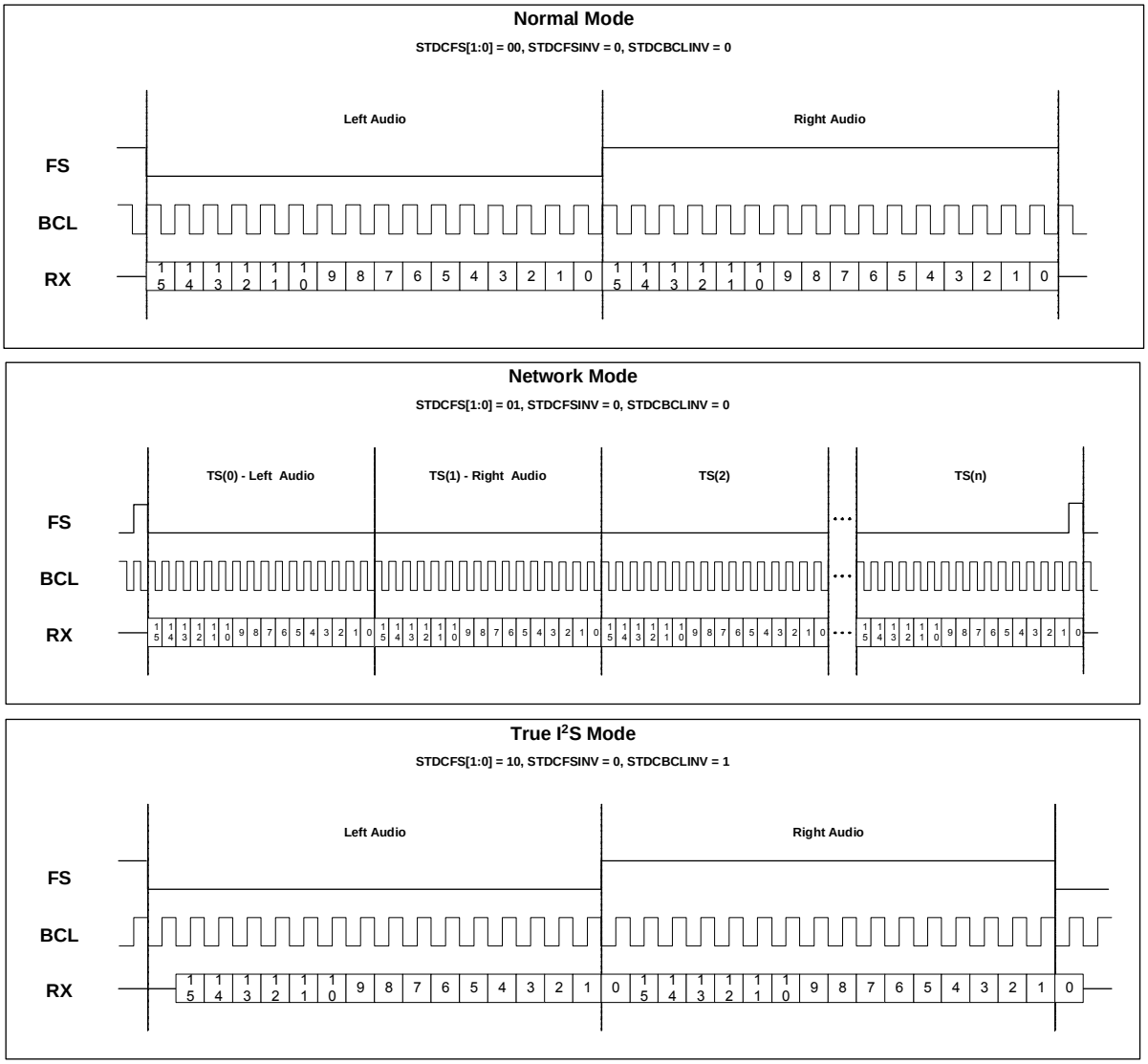


Figure 7-5. Stereo DAC Timing Diagram Examples

The following timing information is applicable for slave mode (STDCSM =1). Figure 7-6 illustrates the meaning of each timing parameter for each polarity configuration.

Table 7-6. Stereo DAC DAI Timing Performance Specifications (Slave Mode)

Parameter	Symbol	Min	Typ	Max	Unit
FS setup to BCL latching edge.	t_{FS}	10	—	—	ns
BCL non-latching edge to RX Data valid.	t_{dv}	—	—	20	ns
RX data hold time from BCL latching edge	t_{dh}	20	—	—	ns

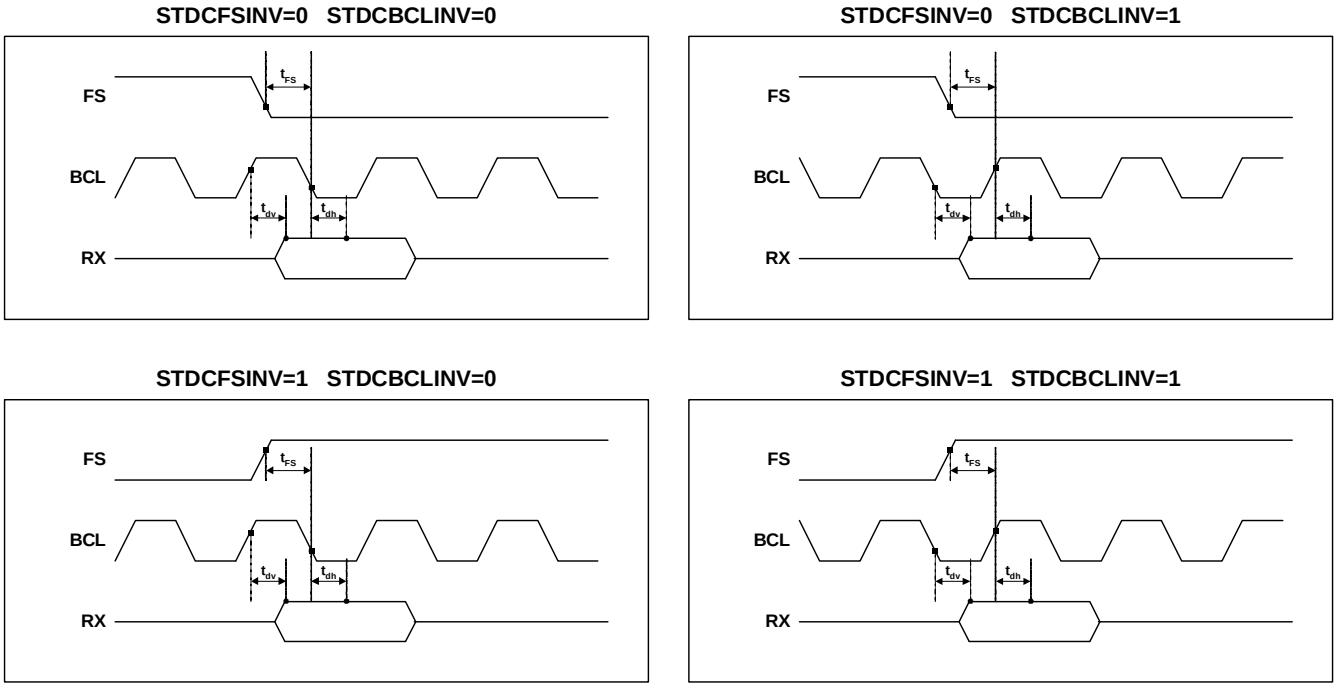


Figure 7-6. Stereo DAC DAI Timing Diagrams (Slave Mode)

The following timing information is applicable for master mode (STDCSM=0). Figure 7-7 illustrates the meaning of each timing parameter for each polarity configuration.

Table 7-7. Stereo DAC DAI Timing Performance Specifications (Master Mode)

Parameter	Symbol	Min	Typ	Max	Unit
BCL non-latching edge to FS out (STDCFSDLYB=1)	t_{FS}	—	—	10	ns
Additional FS delay when STDCFSDLYB=0	t_{FSdly}	9	—	22	ns
BCL non-latching edge to RX Data valid	t_{dv}	—	—	20	ns
RX data hold time from BCL latching edge	t_{dh}	20	—	—	ns

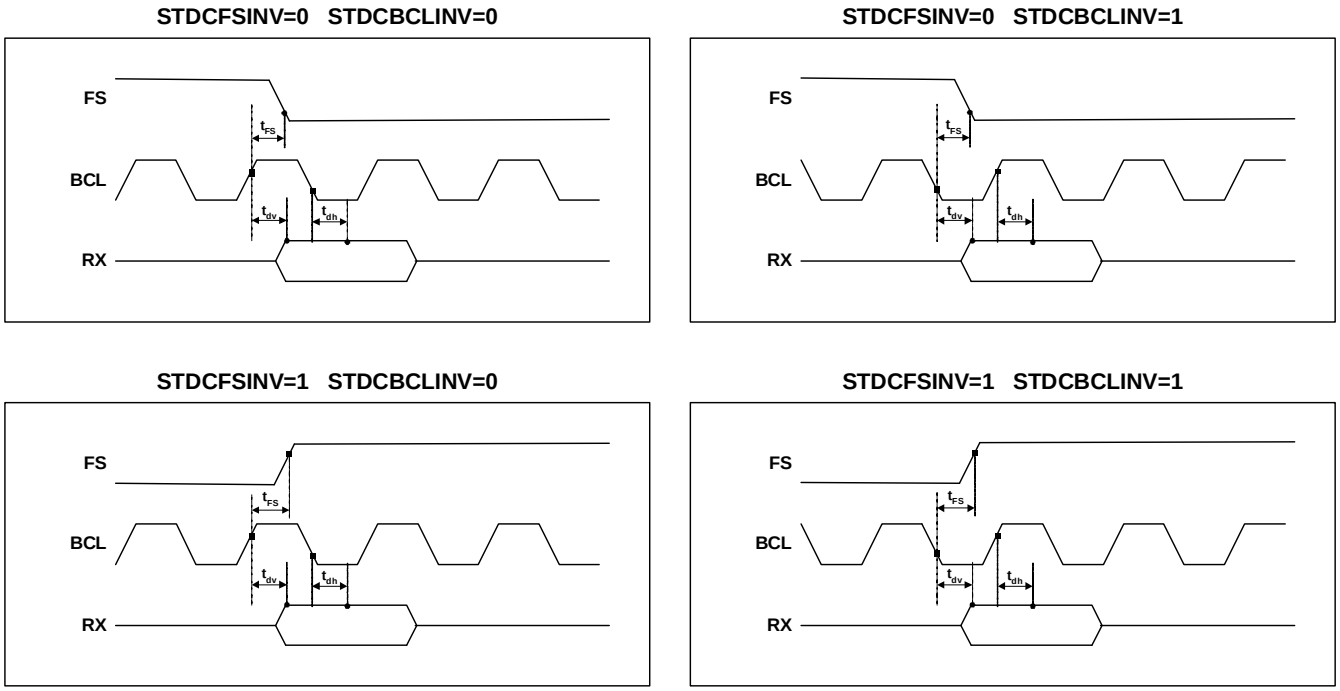


Figure 7-7. Stereo DAC DAI Timing Diagrams (Master Mode)

Some processors rely on the framesync arriving at the same time or being slightly delayed with respect to the bit clock. In practical phone board layouts the delay on the clock lines may not be matched and the framesync may accidentally arrive before the bit clock causing audible issues. In such cases the STDCFSDLYB bit can be set to a 0 (default) which will delay the framesync of the SSI used by the stereo DAC. If set to a 1, no delay is applied.

7.1.4 Audio Port Mixing and Assignment

In network mode, the receive data from two right channel time slots and of two left channel time slots can be added. One left/right time slot pair is considered to represent the main audio flow whereas the other time slot pair represents the secondary flow. The secondary flow can be attenuated with respect to the main flow by 0 dB, 6 dB and 12 dB which must be sufficient to avoid clipping of the composite signal. In addition, the composite signal can be attenuated with 0 dB or 6 dB.

Table 7-8. Stereo DAC SSI Mixing Control and Assignment

Bit Name	Description
STDCRXSLOT[1:0][1]	Defines the primary receive time slots: 00: TS0 and TS1 01: TS2 and TS3 10: TS4 and TS5 11: TS6 and TS7
STDCRXSECSLOT[1:0][1]	Defines the secondary receive time slots: 00: TS0 and TS1 01: TS2 and TS3 10: TS4 and TS5 11: TS6 and TS7
STDCRXSECGAIN[1:0]	Defines the gain applied to the secondary receive time slots: 00: No mixing 01: 0 dB 10 -6 dB 11: -12 dB
STDCSUMGAIN	Defines the gain applied to the summed time slots: 0: 0 dB 1: -6 dB If STDCRXDECGAIN[1:0] = 00 then the applied gain is 0 dB.

1 STDCRXSLOT[1:0] and STDCRXSECSLOT[1:0] must fit in the STDCSLOTS[1:0] setting else no output signal is generated.

Table 7-9. Voice CODEC SSI Mixing Control and Assignment

Bit Name	Description
CDCTXRXSLOT[1:0][1]	Defines the primary receive time slot: 00: TS0 01: TS1 10: TS2 11: TS3
CDCRXSECSLOT[1:0][1]	Defines the secondary receive time slot: 00: TS0 01: TS1 10: TS2 11: TS3
CDCTXSECSLOT[1:0][1]	Defines the secondary transmit time slot: 00: TS0 01: TS1 10: TS2 11: TS3

Table 7-9. Voice CODEC SSI Mixing Control and Assignment (continued)

Bit Name	Description
CDCRXSECGAIN[1:0]	Defines the gain applied to the secondary receive time slots: 00: No mixing 01: 0 dB 10 -6 dB 11: -12 dB
CDCSUMGAIN	Defines the gain applied to the summed time slots: 0: 0 dB 1: -6 dB If CDCRXDECGAIN[1:0] = 00 then the applied gain is 0 dB.

1 In master mode CDCTXRXSLOT[1:0] and CDCRXSECSLOT[1:0] will fit with the generated bit clock, in slave mode the applied bit clock has to be high enough to support the requested settings.

7.2 Voice CODEC

The voice CODEC is based on a 13-bit linear dual A/D and single D/A converter with integrated filtering. It supports several different clocking modes.

7.2.1 Common Characteristics

The voice CODEC is supplied by VAUDIO and its reference is REFC, which is a filtered version of REFA.

Table 7-10. Telephone CODEC Main Common Specifications

Parameter	Condition	Min	Typ	Max	Unit
REFC	—	—	1.3875	—	V
Voice CODEC Bias Current	—	—	3.0	4.0	mA

7.2.2 A/D Converters

The A/D portion of the voice CODEC consists of two A/D converters which convert two incoming analog audio signals into 13-bit linear PCM words at a rate of 8 kHz or 16 kHz. Following the A/D conversion, the audio signal is digitally band pass filtered. The converted voice is available on the audio bus. If both A/D channels are active the audio bus is operated in a network mode. The most direct analog input to the voice CODEC A/D portion is TXIN and this signal passes via the PGA, see audio input section, and therefore is an integral part of the CODEC A/D performance.

Table 7-11. Telephone CODEC A/D Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Peak Input (+3dBm0)	Single ended	REFC-0.68	—	REFC+0.68	V
CODEC PSRR	With respect to BP, 0 to 20 kHz	80	90	—	dB_P
Absolute Gain	0 dBm0 at 1.02 kHz, Gain = 0 dB	-1	—	1	dB

Table 7-11. Telephone CODEC A/D Performance Specifications (continued)

Parameter	Condition		Min	Typ	Max	Units
Gain vs. Signal	relative to -10 dBm0 at 1.02 kHz	+2 to -40 dBm0	-0.25	—	0.25	dB
		-40 to -50 dBm0	-1.2	—	1.2	dB
		-50 to -55 dBm0	-1.3	—	1.3	dB
Total Distortion (noise and harmonic)	at 1.02 kHz (linear) 20 kHz Noise BW in 8.0 kHz measurement BW out	+2 dBm0	60	70	—	dB_P
		0 dBm0	60	70	—	dB_P
		-6 dBm0	60	70	—	dB_P
		-10 dBm0	55	65	—	dB_P
		-20 dBm0	45	55	—	dB_P
		-30 dBm0	35	45	—	dB_P
		-40 dBm0	25	35	—	dB_P
		-45 dBm0	20	30	—	dB_P
		-55 dBm0	15	20	—	dB_P
Idle Channel Noise	0 db PGA gain, incl. microphone amp		—	—	-72	$dBm0_P$
Digital Offset	—		—	—	-60	LSBs
Inband Spurious	0 dBm0 at 1.02 kHz input, 300 Hz to 3.0 kHz (8 kHz sample rate)		—	—	-48	dB
Intermodulation Distortion	SMTPE method 50 Hz/1020 Hz, 4:1 0 dBm0 total input level		—	—	-40	dB
Crosstalk A/D to D/A	A/D = 0 dBm0 at 1.02 kHz, D/A stimulated with -0 dBm0 at 1.02 kHz		—	—	-75	dB
Enable Time	Bias was not enabled		—	—	50	ms
	Bias was enabled and established		—	—	4.5	ms

Table Footnotes:

1. Unless otherwise noted in Table 7-11, all analog signals are referenced to REFC.
2. Unless otherwise noted in Table 7-11, the AUDIG SPI bits are set for is set for 0 dB gain.
3. Unless otherwise noted in Table 7-11, the analog input is 340 mVRMS.
4. A 340 mVRMS analog input into telephone CODEC produces a digital output of 0 dBm0.

If the analog audio level into the CODEC is set such that the digital output is +3 dBm0 (digital word 0FFF), any variation in gain can cause the output to exceed +3 dBm0. This will cause large amounts of distortion. Therefore, to minimize distortion, the maximum analog input signal into the CODEC must be set such that the digital output is + 3dBm0- (Absolute Gain Error) = + 2dBm0.

7.2.3 D/A Converter

The D/A portion of the voice CODEC converts 13-bit linear PCM words entering at a rate of 8 kHz and 16 kHz into analog audio signals. Prior to this D/A conversion, the audio signal is digitally band-pass filtered. The most direct analog output from the voice CODEC D/A portion passes via the PGA, see audio output section, and therefore is an integral part of the CODEC D/A performance.

Table 7-12. Telephone CODEC D/A Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Peak Output (+3dBm0)	Single ended output		REFC - 1	—	REFC + 1	V
Crosstalk between outputs	0 dBm0 at 1.02 kHz		—	—	-60	dB
Output Source Impedance	At 1.02 kHz		—	—	100	Ω
CODEC PSRR	With respect to B+, 20 Hz to 20 kHz,		80	90	—	dB
Gain vs. Signal	Relative to -10 dBm0 at 1.02 kHz	+3 to -40 dBm0	-0.25	—	0.25	dB
		-40 to -50 dBm0	-1.2	—	1.2	dB
		-50 to -55 dBm0	-1.3	—	1.3	dB
Absolute Gain	0 dBm0 at 1.02 kHz,	Gain = 0 dB	-1	—	1	dB
Total Distortion (noise and harmonic)	At 1.02 kHz, 4 kHz Noise BW in, 20 kHz measurement BW out	+2 dBm0	65	77	—	dB
		0 dBm0	65	75	—	dB
		-6 dBm0	60	69	—	dB
		-10 dBm0	55	65	—	dB
		-20 dBm0	45	55	—	dB
		-30 dBm0	35	45	—	dB
		-40 dBm0	25	35	—	dB
		-45 dBm0	20	30	—	dB
		-55 dBm0	15	20	—	dB
Idle Channel Noise	At CODEC output, Bwout = 20 kHz A weighted		—	-78	-74	dBm0
Inband Spurious	0 dBm0 at 1.02 kHz to 3.4 kHz input. 300 Hz to 20.0k Hz		—	—	-50	dB
Intermodulation Distortion	SMTPE method 50Hz/1020Hz, 4:1 –3 dBFS total input level		—	—	-40	dB
Crosstalk D/A to A/D	A/D stimulated with 0dBm0 at 1.02 kHz		—	—	-75	dB
Enable Time	Bias was not enabled		—	—	50	ms
	Bias was enabled and established		—	—	4.5	ms

Table Footnotes:

1. Unless otherwise noted in Table 7-12, all analog signals are referenced to REFC.
2. Unless otherwise noted in Table 7-12, the AUDOG SPI bits are set for is set for 0 db gain.
3. Unless otherwise noted in Table 7-12, the digital input is 0 dBm0.
4. A 0 dBm0 digital input into telephone CODEC produces an analog output of 500 mVRMS.

If the digital input signal into the CODEC is +3 dBm0 (digital word 0FFF), any variation in gain can cause this signal to exceed +3 dBm0. This will cause large amounts of distortion. Therefore, to minimize distortion, the maximum digital input signal into the CODEC must be +3 dBm0- (Absolute Gain Error) = +2 dBm0.

7.2.4 Clock Modes

In master mode the CLI is divided internally to generate the BCL and FS signals. In slave mode these clocks have to be supplied and in that case there is no imposed relationship between BCL and the other clocks as long as it is high enough to support the number of time slots requested.

Table 7-13. Telephone CODEC Input Clock Selection SPI Bits

CDCFS8K16K	CDCCLK2	CDCCLK1	CDCCLK0	CLI (MHz)	FS (kHz)	BCLMaster (kHz)
0	0	0	0	13.0	8	520
0	0	0	1	15.36	8	512
0	0	1	0	16.8	8	560
0	0	1	1	NA	—	—
0	1	0	0	26.0	8	520
0	1	0	1	NA	—	—
0	1	1	0	NA	—	—
0	1	1	1	33.6	8	560
1	0	0	0	13	16	1040
1	0	0	1	15.36	16	1024
1	0	1	0	16.8	16	1120
1	0	1	1	NA	—	—
1	1	0	0	26.0	16	1040
1	1	0	1	NA	—	—
1	1	1	0	NA	—	—
1	1	1	1	33.6	16	1120

7.2.5 Control Bits

Table 7-14. Telephone CODEC Input Clock Selection SPI Bits

Name	# of Bits	Description
AUDOHPF	1	Audio Output High Pass Filter. Logic high enables the filter.
AUDIHPF	1	Audio Input High Pass Filter. Logic high enables the filter.
CDCALM	1	A logic high, loops Sigma Delta output of the A/D path back to the input of the analog part of D/A path (bit stream analog D to A converter). Analog loop-back mode is used for testing. When CDCALM is reset to logic low, Analog loop-back is disabled.
CDCDLM	1	A logic high, loops the 13 bit DIGITAL output of the A/D converter back to the 13 bit DIGITAL input of the D/A converter. Digital loop-back mode is used for testing. When CDCDLM is reset to logic low, Digital loop-back is disabled.
CDCCLKSEL	1	CODEC CLI clock selection. Logic 0 select CLIA. Logic 1 select CLIB
CDCCLK	3	Selects the CODEC clock input and output frequencies
CDCBCLINV	1	A logic high inverts the serial interface clock (IN or OUT)
CDCFSINV	1	A logic high inverts the frame sync (IN or OUT)
CDCRESET	1	CDCRESET resets the digital filter in the CODEC. This bit must be set to one when BCL, AUDOHPF, or AUDIHPF are changed. This is a self-clearing bit that will clear at the falling edge of SPI CE.
CDCEN	1	Selects CODEC power up states. Power up default is 0. Enables the voice CODEC core and convertors except for the left channel voice CODEC ADC for which also AMC1LEN has to be set to a 1.
CDCCLKEN	1	If programmed high and CDCTS is low, FS and BCL outputs are enabled when in master mode. Outputs enabled only for digital audio I/O path selected by CDCSSISEL bit. If programmed low, FS and BCL outputs are tri-stated. Provides master clock capability when CODEC D/A converter, A/D converter and digital filters are powered down by CDCEN.
CDCTS	1	If programmed high then FS, TX and BCL are tri-stated. Note that this control function will occur asynchronously.
CDCSM	1	If programmed high then the CODEC acts as a slave with BCL and FS driven as inputs. If programmed low then the CODEC acts as a master with BCL and FS driven as outputs.
CDCSSISEL	1	A logic high (default) enables FS2, BCL2 and RX2 digital audio I/O paths. A logic low enables FS1, BCL1 and RX1 digital audio I/O paths.
CDCFS8K16K	1	A logic 0 selects 8kHz sampling, a logic 1 selects 16kHz sampling.
CDCFS[1:0]	2	Bus protocol selection (Network, I2S)
CDCFSDLY	1	A logic high delays the FS with respect to the BCL
CDCTXRXSLOT[1:0]	2	CODEC time slot assignment
CDCTXSECSLOT[1:0]	2	CODEC secondary transmit time slot
CDCRXSECSLOT[1:0]	2	CODEC secondary receive time slot
CDCRXSECGAIN[1:0]	2	CODEC secondary receive channel gain setting
CDCSUMGAIN	1	CODEC summed receive signal gain setting

Table 7-14. Telephone CODEC Input Clock Selection SPI Bits (continued)

Name	# of Bits	Description
CDCBYP	1	CODEC bypass. When High, the whole CODEC is bypassed and the signal coming from the microphone amplifiers is injected to the PGA
CDCDITH	1	When the output dither bit, CDCADITH, is reset to a logic low, dithering is enabled. Dithering de-correlates the periodic modulator quantization noise of the output converter. If CDCADITH is set to a logic high, dithering is disabled.

7.3 Stereo DAC

7.3.1 Common Characteristics

The stereo DAC is supplied by VAUDIO, its reference is REFD and its common mode voltage is REFA, see bias and anti pop section.

Table 7-15. Stereo DAC Main Common Specifications

Parameter	Condition	Min	Typ	Max	Unit
REFD		—	2.775	—	V
PSRR REFD	With respect to BP	90	100	—	dB
DAC Bias Current	Excluding PLL, STDCCLK = 101, STDCSM = 1	—	4	5	mA
DAC Bias Current	Including PLL, STDCCLK = 000, STDCSM = 0	—	6	7	mA

7.3.2 D/A Converter

The stereo DAC is based on a 16-bit linear left and right channel D/A converter with integrated filtering.

Table 7-16. Stereo DAC Main Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Absolute Gain	Input at 0 dBFS, from 20 Hz to 20 kHz		-0.5	—	+0.5	dB
Gain vs. Signal	Relative to input at -10 dBFS, 1.02 kHz	input from -1 to -40 dBFS	-0.25	—	+0.25	dB
		input from -40 to -50 dBFS	-0.7	—	+0.7	dB
		input from -50 to -55 dBFS	-1.3	—	+1.3	dB
L/R Gain Mismatch	Input at -3 dBFS, 1.02 kHz		—	0.2	0.3	dB
Total Distortion THD+N (noise and harmonics)	Input at 0 dBFS from 20 Hz to 20 kHz	Fs ≥ 44.1 kHz	—	-85	-80	dB
		Fs = 32 kHz	—	—	-70	dB
		Fs ≤ 24 kHz	—	—	-65	dB

Table 7-16. Stereo DAC Main Performance Specifications (continued)

Parameter	Condition		Min	Typ	Max	Units
Total Distortion THD+N (noise and harmonics)	Input at 1.02 kHz, 20 kHz BW out	input at -1 dBFS	—	-90	-85	dB
		input at -3 dBFS	—	-87	-83	dB
		input at -10 dBFS	—	-80	-77	dB
		input at -20 dBFS	—	-70	-67	dB
		input at -30 dBFS	—	-60	-57	dB
		input at -40 dBFS	—	-50	-47	dB
		Input at -60 dBFS	—	-30	-25	dB
Dynamic Range	(SNDR at -60 dBFS and 1.02 kHz) + 60 dB, 20 kHz BW out, A weighted	Stereo DAC only	92	96	—	dB
		Stereo DAC plus PGA, Ahsr, Ahsl	86	—	—	dB
Signal to Noise Ratio	Input 0 dBFS, 1.02 kHz, 20 kHz BW out, A weighted	Stereo DAC only	92	96	—	dB
		Stereo DAC plus PGA, Ahsr, Ahsl	86	—	—	dB
Output PSRR	With respect to battery, input at 0 dBFS, from 20 Hz to 20 kHz, A weighted		90	—	—	dB
L/R Output Crosstalk	Input at -3 dBFS, 1.02 kHz		—	-100	-80	dB
Intermodulation Distortion	SMTPE method 50 Hz/1020 Hz, 4:1 -3 dBFS total input level Measured at headset amplifier outputs		—	—	-75	dB
Spurious	Input at -3 dBFS, from 20 Hz to 20 kHz, 20 kHz BW out, includes idle tones		—	—	-75	dB
Enable Time	Including PLL		—	—	—	—
	Bias was not enabled		—	—	50	ms
	Bias was enabled and established		—	—	4.5	ms
Digital Filter Performances						
Pass Band			0.4535	—	—	Fs
Stop Band			—	—	0.5465	Fs
Stop Band Attenuation			65	—	—	dB
Pass Band Ripple	In pass band		-0.25	—	0.25	dB
Group Delay	In pass band	Fs = 44.1 kHz	—	—	400	us
		Fs = 8 kHz	—	—	2	ms
Linear Phase (see plot)	In pass band		-20	—	+20	°

Table Footnotes:

1. Unless otherwise noted, these performances are specified at the stereo DAC output and do not include the contribution of the PGAs and driver amplifiers connected at the output the stereo DAC.
2. Unless otherwise noted, all analog signals are referenced to REFD, bypassed with 1 uF.

3. The common mode voltage REFA is bypassed with 100 nF.
4. Unless otherwise noted, the digital input is -3 dBFS (0 dBm0).
5. A nominal digital input into the stereo DAC of -3 dBFS (0d Bm0) produces an analog output of 500 mVrms.
6. A maximum digital input into stereo DAC of 0 dBFS (+3 dBm0) produces an analog output of 707 mVrms or 1 Vp.
7. The Table 7-16 is applicable for all sample frequencies and all modes of operation.
8. The usable part of the 20 Hz–20 kHz input bandwidth is limited by the sample frequency used.
9. The 20 kHz output bandwidth is applicable for all sample frequencies.

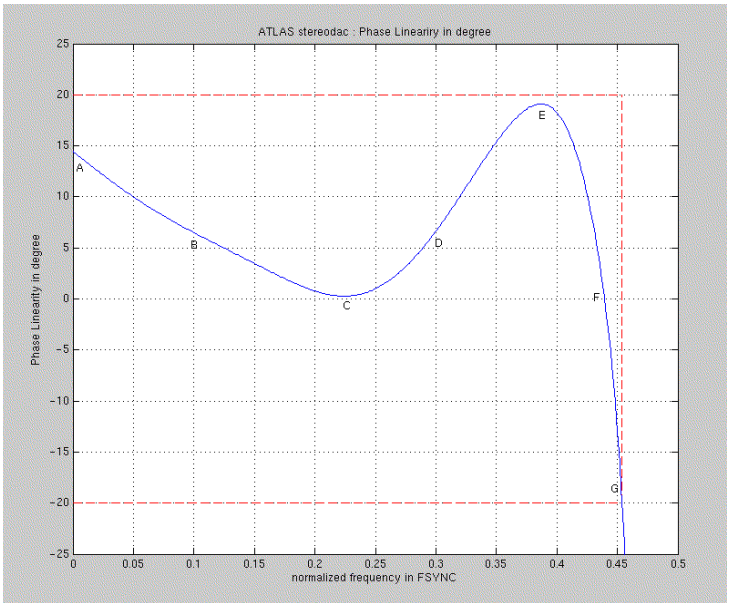


Figure 7-8. Stereo DAC Phase Linearity

7.3.3 Clock Modes

The stereo DAC incorporates a PLL to generate the proper clocks in master and in slave modes. The PLL requires an external C//RC loopfilter.

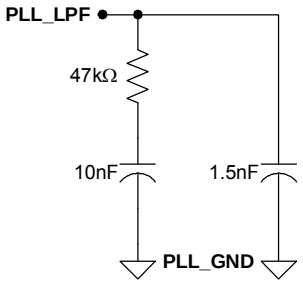


Figure 7-9. Stereo DAC PLL External Loop Filter Diagram

In Master Mode, the PLL of the Stereo DAC generates FS and BCL signal based on the reference frequency applied through one of the CLI inputs. The CLI frequencies supported are 3.6864 MHz,

12 MHz, 13 MHz, 15.36 MHz, 16.8 MHz, 26 MHz and 33.6 MHz. The PLL will also generate its own master clock MCL used by the stereo DAC itself.

In Slave Mode, FS and BCL are applied to the MC13783 and the MCL is internally generated by the PLL based on either FS or BCL.

The sample rates supported are 32kHz, 44.1kHz and 48kHz divided by 1, 2, and 4, plus 64 kHz and 96 kHz. There is a fixed relationship between the different clock signals where BCL = 32*FS and MCL is FS times 512, 256, 128 or 64 depending on the sample rate. In network mode the BCL to FS ratio will be raised to 64 (for 2 time slot pairs) or 128 (for 4 time slot pairs) while the MCL to FS ratio remains constant.

A special mode is foreseen where the PLL is bypassed and CLI can be used as the MCL signal. In this mode, MCLK must be provided with the exact ratio to FS, depending on the sample rate selected. In this mode, the BCL does not necessarily have to be exactly an integer multiple of 32*FS. Higher BCL rates are accepted as well.

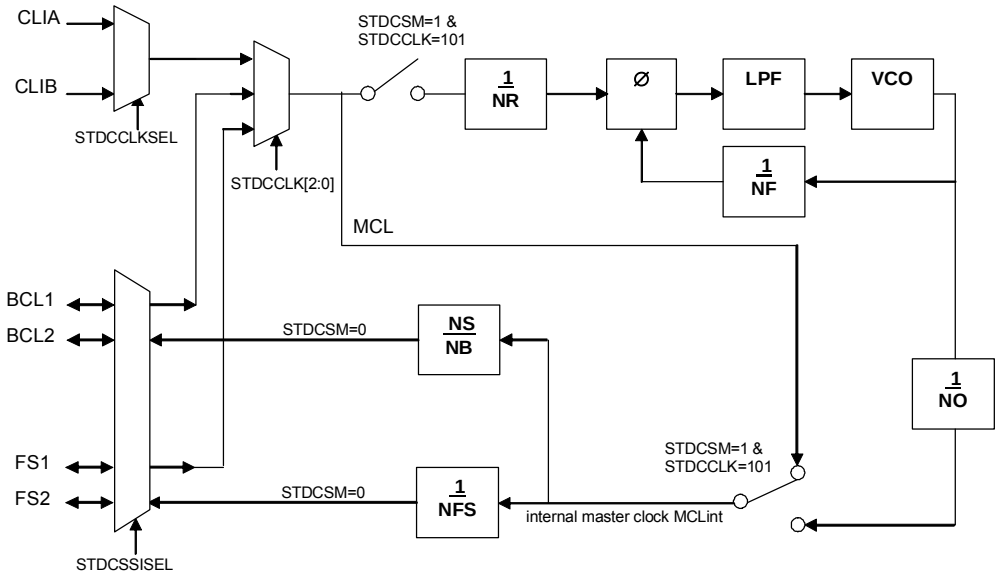


Figure 7-10. Stereo DAC PLL Block Diagram

Table 7-17. Stereo DAC Input Clock Selection SPI Bits

STDCSM	STDCCLK2	STDCCLK1	STDCCLK0	PLL input
0 = Master	0	0	0	CLI = 13.0 MHz
0 = Master	0	0	1	CLI = 15.36 MHz
0 = Master	0	1	0	CLI = 16.8 MHz
0 = Master	0	1	1	NA
0 = Master	1	0	0	CLI = 26.0 MHz
0 = Master	1	0	1	CLI = 12.0 MHz
0 = Master	1	1	0	CLI = 3.6864 MHz
0 = Master	1	1	1	CLI = 33.6 MHz
1 = Slave	0	X	X	NA
1 = Slave	1	0	0	NA

Table 7-17. Stereo DAC Input Clock Selection SPI Bits (continued)

STDCSM	STDCCLK2	STDCCLK1	STDCCLK0	PLL input
1 = Slave	1	0	1	CLI = MCL, PLL disabled
1 = Slave	1	1	0	FS
1 = Slave	1	1	1	BCL

Table 7-18. Stereo DAC Sample Rate Selection SPI Bit

SR3	SR2	SR1	SR0	FS	N_{FS}	MCL	N_B	BCL
0	0	0	0	8000	512	4096 k	16	256 k
0	0	0	1	11025	512	5644.8 k	16	352.8 k
0	0	1	0	12000	512	6144 k	16	384 k
0	0	1	1	16000	256	4096 k	8	512 k
0	1	0	0	22050	256	5644.8 k	8	705.6 k
0	1	0	1	24000	256	6144 k	8	768 k
0	1	1	0	32000	128	4096 k	4	1024k
0	1	1	1	44100	128	5644.8 k	4	1411.2 k
1	0	0	0	48000	128	6144k	4	1536 k
1	0	0	1	64000	64	4096 k	2	2048 k
1	0	1	0	96000	64	6144k	2	3072 k
1011 to 1111 are reserved combinations								
Note: These values are valid for a single time slot pair.								

In the network mode, it's possible to select more than two time slots by using the selection bits STDCSLOTS[1:0]. In this case, the divider coefficients NFS and NB, and the master clock MCL remain unchanged. Only the divider coefficient NS changes in order to adapt the BCL frequency to the selected time slots number.

In the modes using only two time slots (normal and I2S modes), the bits STDCSLOTS[1:0] must be set to 11.

Table 7-19. Stereo DAC MCL Divider Selection SPI Bits

STDCSLOTS1	STDCSLOTS0	N_S (or BCL/FS/32)	Possible Time Slots
0	0	4	8
0	1	4[1]	8 (Left, Right, 6 other)
1	0	2	4 (Left, Right, 2 other)
1	1	1	2 (Left, Right)

[1] Not available for 64 kHz and 96 kHz sample rates.

Since both the stereo DAC and the voice CODEC can be assigned to the same SSI bus, conflicts may arise during concurrent use cases. In case of slave modes, this does not cause any physical issue but can cause

undesired signals to be generated due to improper clock frequencies and must therefore be avoided. In clock master modes however, bus drive conflicts can occur when no measures are taken. For that reason, only one of the clock drivers gets enabled under these circumstances according to Table 7-20.

Table 7-20. SSI Master Clocking Contingency Matrix

	CDCEN = 0	CDCEN = 1
STDCEN = 0	CODEC Clocks	CODEC Clocks
STDCEN = 1	Stereo DAC Clocks	No Clocks
Conditions: CDCSM = 0, CDCCLKEN = 1, CDCTS = 0, STDCSM = 0, STDCCLKEN = 1		

7.3.4 Control Bits

Table 7-21. Stereo DAC Control SPI Bits

Name	# of Bits	Description
STDCEN	1	Controls power up state of the stereo DAC. A logic 1 enables the DAC.
STDCSSISEL	1	A logic 0 enables FS1, BCL1 and RX1 digital audio I/O paths. A logic 1 enables FS2, BCL2 and RX2 digital audio I/O paths.
STDCCLKSEL	1	A logic 0 enables CLIA audio clock. A logic 1 enables CLIB audio clock
STDCCLK[2:0]	3	Selects the PLL clock input frequencies: CLI, MCL, FS or BCL.
STDCSM	1	If programmed low then the DAC acts as a master with BCL and FS driven as outputs. If programmed high then the DAC acts as a slave with BCL and FS driven as inputs.
SR[3:0]	4	Selects the sample rate FS of the stereo DAC
STDCCLKEN	1	If programmed high, FS and BCL outputs are enabled when in master mode. Outputs enabled only for digital audio I/O path selected by STDCSSISEL bit. If programmed low, FS and BCL outputs are tri-stated. Provides master clock capability when ST_DAC D/A converter, and digital filters are powered down by STDCEN.
STDCRESET	1	Resets the digital filters in the DAC. This bit must be set to a one when BCL or SR are changed. This will be a self-clearing bit that will clear at the falling edge of SPI CE.
STDCBCLINV	1	A logic high inverts BCL (input or output)
STDCFSINV	1	A logic high inverts FS (input or output)
STDCFS[1:0]	2	Bus protocol selection (Normal, Network, I2S)
STDCFSDLYB	1	A logic low delays the FS with respect to the BCL (default state)
SPDIF	1	Selects the SPDIF mode. This mode is no longer available. This bit has to be programmed to 0.
STDCSLOTS[1:0]	2	Defines relationship between BCL and FS and determine the number of time slots when operating the Stereo DAC in a network mode.
STDCRXSLOT[1:0]	2	In network mode, defines the time slot pair used for the primary audio stream
STDCRXSECSLOTS[1:0]	2	In network mode, defines the time slot pair used as secondary audio stream.

Table 7-21. Stereo DAC Control SPI Bits (continued)

Name	# of Bits	Description
STDCRXSECGAIN[1:0]	2	In network mode, defines the gain applied to the time slot pair of the secondary audio stream.
STDCSUMGAIN	1	In network mode, defines the gain applied to the summed time slot pairs.

7.4 Audio Input Section

7.4.1 Microphone Bias

Two microphone bias circuits are provided. One circuit supplies up to two handset microphones via the two outputs MC1RB and MC1LB. The second circuit supplies the headset microphone via MC2B. The microphone bias resistors are included. The bias circuits can be enabled and disabled.

The bias MC2B includes a microphone detect circuit which monitors the current flow through the output both when the bias is disabled or enabled. This will generate an interrupt to the processor. In this way the attach and removal of a headset microphone is detected. Also it allows to include a send/end series switch with the microphone for signalling purposes. When the output of the MC2B gets out of regulation, an interrupt is generated. This allows for connecting a switch in parallel to the microphone. These detect functions can be enabled by setting the MC2BDETEN bit while the audio bias is not enabled. If VAUDIO or the MC13783 are turned off, no detection will take place.

Table 7-22. MC1RB, MC1LB and MC2B Parametric Specifications

Parameter	Condition	Min	Typ	Max	Units
Microphone Bias Output Voltage	MC1RB, MC1LB, No Load	2.23	2.38	2.53	V
	MC2B, No Load	2.00	2.10	2.20	V
Microphone Bias Internal Voltage Load Regulation	0 < IL < 1mA	—	—	50	mV
Output Current	Source only	0	—	500	uA
Bias Current	No Load	—	—	250	uA
Bias Resistor	MC1RB, MC1LB	1.20	1.33	1.63	kOhm
	MC2B	2.09	2.20	2.31	kOhm
Microphone Detect Current	MC2B	30	—	50	uA
Microphone Detect Voltage	MC2B not active[1]	—	2.1	—	V
	MC2B active[2]	0.40	—	0.80	V
PSRR	With respect to BP 20 Hz - 10 kHz	90	—	—	dB
Output Noise	Includes REFA noise CCITT psophometricly weighted	—	1.5	3.0	uVrms

1 Internal pull up to VAUDIO.

2 Corresponds to a parallel switch with an impedance of 500 Ohm max

Table 7-23. Microphone Detect

	No Headset	Headset without Mic	Headset with Mic	Headset with Mic Serial Switch Closed	Headset with Mic Serial Switch Opened	Headset with Mic Parallel Switch Open	Headset with Mic Parallel Switch Closed
MC2B Not Active							
MC2B Voltage	High	High	Low	Low	High	Low	Low
MC2BS Bit	0	0	1	1	0	1	1
MC2B Active							
MC2B Current	Low	Low	High	High	Low	High	High
MC2B Voltage	High	High	High	High	High	High	Low
MC2BS Bit	0	0	1	1	0	1	0
HSDETS Bit	0	1	1	1	1	1	1

When MC2B is not active and the MC2BDETEN bit is set, a microphone detect MC2BI is generated when the voltage read changes state. The actual state can be read out via the corresponding MC2BS bit. When MC2B is active and the MC2BDETEN bit is set, a microphone detect MC2BI is generated when the MC2BS bit changes state, meaning the current read or voltage read changes state.

In order to distinguish a headset removal from a send/end command, the state of the headset detect is also taken into account before generating the MC2BI interrupt. If the HSDETI is a 0, the headset was not removed at the same time a send/end command was detected, and as a result the MC2BI is generated upon each state change of MC2BS. If the HSDETI is a 1, the headset was removed at the same time and therefore the state change in MC2BS was not due to a press on the send/end button. In that case a MC2BI is not generated. Besides this hardware mechanism, the headset detect bits can always be verified while reading the microphone detect and sense bits.

While most interrupts due to external events are debounced by 30 ms, the microphone detect interrupt MC2BI is optionally debounced for a total of 100 ms when the MC2BDETDBNC bit is set to a 1. When the HSDETAUTOB bit is set, upon a headset removal the Amc2 amplifier will automatically be disabled, see headset detection.

7.4.2 Microphone Amplifiers

Figure 7-11 is a block diagram of the microphone amplifier section. A selection can be made between one of the three amplified inputs: the handset microphone connected to MC1RIN, the headset microphone connected to MC2IN, and the line input TXIN. The selected channel can be fed into the receive channel for test purposes. In addition a second amplified input channel can be selected for the second handset microphone connected to MC1LIN.

The microphone signal amplifiers can be configured as V to V and as I to V amplifiers while the TXIN signal is buffered. The amplified signal is fed to a first PGA with a course gain setting and then fed to a second PGA which is embedded in the voice CODEC. This second PGA has a fine gain control. For the I to V mode, the overall gain accuracy is trimmed during production by adjusting the microphone amplifiers

feedback resistor. All signal inputs must be AC connected. The applied topology selects the amplified input signals instead of selecting the non amplified input signals which provides EMI robustness.

NOTE

Note the fine gain programming (2nd PGA) is performed by the CODEC section. This insures 0 to +7 dB in 1 dB steps. The course gain programming is ensured by the first PGA section. Steps are -8 dB, 0 dB, +8 dB and +16 dB. By combining these two stages, gain programmability from -8 dB to +23 dB is performed by the TX section.

In order to support the CEA-936-A carkit specification, see also Chapter 10, "Connectivity", the TXOUT pin provides a non amplified version of the carkit microphone signal channel as present on the USB interface D+ line. The bias is not equivalent to the MC13783 audio reference REFA. The output signal at TXOUT therefore has to be AC coupled to the TXIN input for further processing by the voice CODEC. To enable the signal path from USB interface to TXOUT, only the USB interface and routing has to be set. See Chapter 10, "Connectivity" for details.

In addition to the microphone amplifier paths, there is also the possibility to route the stereo line in signal from RXINR and RXINL to the voice CODEC dual ADC section. This allows for 13-bit, 16 kHz sampled stereo recording of an analog source such as FM radio. In combination with the PGA gain setting possibilities this will give sufficient performance for this type of application. The line in routing is enabled by setting the RXINREC bit high while all other inputs are deselected, see contingency matrix. The line in is taken directly at the pins RXINR and RXINL which means that any user volume or balance control has no influence on the recording levels.

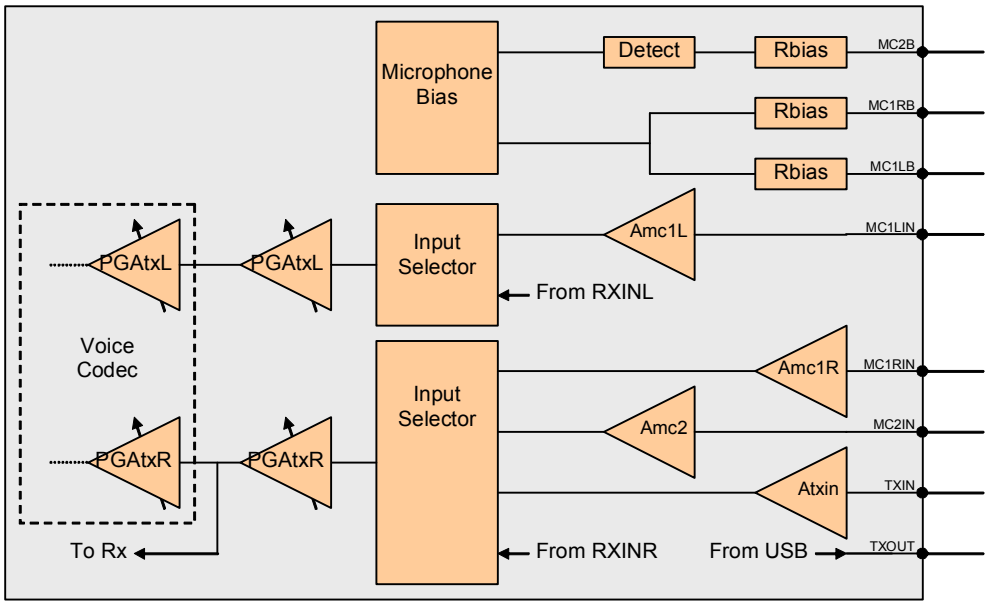


Figure 7-11. Audio Input Section Diagram

Table 7-24. Amplifiers Amc1L, Amc1R, Amc2, Atxin Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Input Bias Current	Input to REFA		—	1	—	uA
Input Offset Voltage			—	—	5	mV
Supply Current			—	—	200	uA
Gain (V to V)	At 1.0 kHz, Vin = 100 mVpp		11.8	12	12.2	dB
Input Impedance (V to V)	Amc1L, Amc1R, Amc2		8.5	10	11.7	kΩ
	Atxin		—	40	—	kΩ
Gain (I to V)	Equivalent Feedback Resistor to 24 dB (after trimming)		33	35	37	kΩ
Gain (Atxin)	TXIN to Voice CODEC		-0.2	0	0.2	dB
	UDP to TXOUT to TXIN to Voice CODEC		-0.9	-0.4	+0.1	dB
THD (2^{nd} and 3^{rd})	At 1.0 kHz	V_{OUT} = 1 V_{PP}	—	—	0.1	%
		V_{OUT} = 10 mV_{RMS}	—	—	0.1	%
		V_{OUT} = 1 mV_{RMS}	—	—	0.1	%
PSRR	With respect to BP, 20 Hz – 10 kHz, inputs AC grounded		—	90	—	dB
Input Noise	Input to REFA CCITT psophometricly weighted		—	—	1	uV_{RMS}
Closed Loop–3 dB Point			20	—	—	kHz

Table 7-25. Control Bit Definition

Bit	Description
PGATXR[4 :0]	Transmit gain setting right from –8 dB to +23 dB. 00000 lowest gain, 11111 highest gain, 01000 default (0 dB).
PGATXL[4:0]	Transmit gain setting left from –8 dB to +23 dB. 00000 lowest gain, 11111 highest gain, 01000 default (0 dB).
MC1BEN	Microphone bias 1 enable.
MC2BEN	Microphone bias 2 enable.
MC2BDETEN	Microphone bias 2 detect enable.
MC2BDETDBNC	Selects the debounce time for the MC2BI interrupt.
AMC1REN	Amplifier Amc1R enable.
AMC1RITOV	Amplifier Amc1R current to voltage mode enable.
AMC1LEN	Amplifier Amc1L enable, automatically enables the left channel ADC section of the voice CODEC if the voice CODEC was enabled via CDCEN.
AMC1LITOV	Amplifier Amc1L current to voltage mode enable.
AMC2EN	Amplifier Amc2 enable.

Table 7-25. Control Bit Definition (continued)

Bit	Description
AMC2ITOV	Amplifier Amc2 current to voltage mode enable.
ATXINEN	Amplifier Atxin enable.
ATXOUTEN	Reserved for output TXOUT enable, currently not used.
RXINREC	RXINR/RXINL to voice CODEC ADC routing enable, automatically enables the left channel ADC section of the voice CODEC if the voice CODEC was enabled via CDCEN.

Table 7-26. Input Selection Contingency Matrix

AMC1REN	AMC2EN	ATXINEN	RXINREC	Input selected	AMC1LEN	RXINREC	Input selected
1	x	x	x	MC1RIN	1	x	MC1LIN
0	1	x	x	MC2IN	0	1	RXINL[1]
0	0	1	x	TXIN	0	0	None
0	0	0	1	RXINR	—	—	—
0	0	0	0	None	—	—	—
Note: Voice CODEC right channel enabled when CDCEN = 1. Voice CODEC left channel enabled when CDCEN AND (AMC1LEN OR RXINREC) = 1.							

[1] Only valid if right input selected is RXINR, else None.

Table 7-27. Audio Input Parametric Specifications

Parameter	Condition	Min	Typ	Max	Units
PGA Gain Setting Accuracy	Relative to 0 dB setting	-0.5	—	+0.5	dB
Crosstalk between inputs	0 dBm0 at 1.02 kHz	—	—	-60	dB

7.5 Audio Output Section

7.5.1 Audio Signal Routing

Figure 7-12 shows the audio output section indicating the routing possibilities.

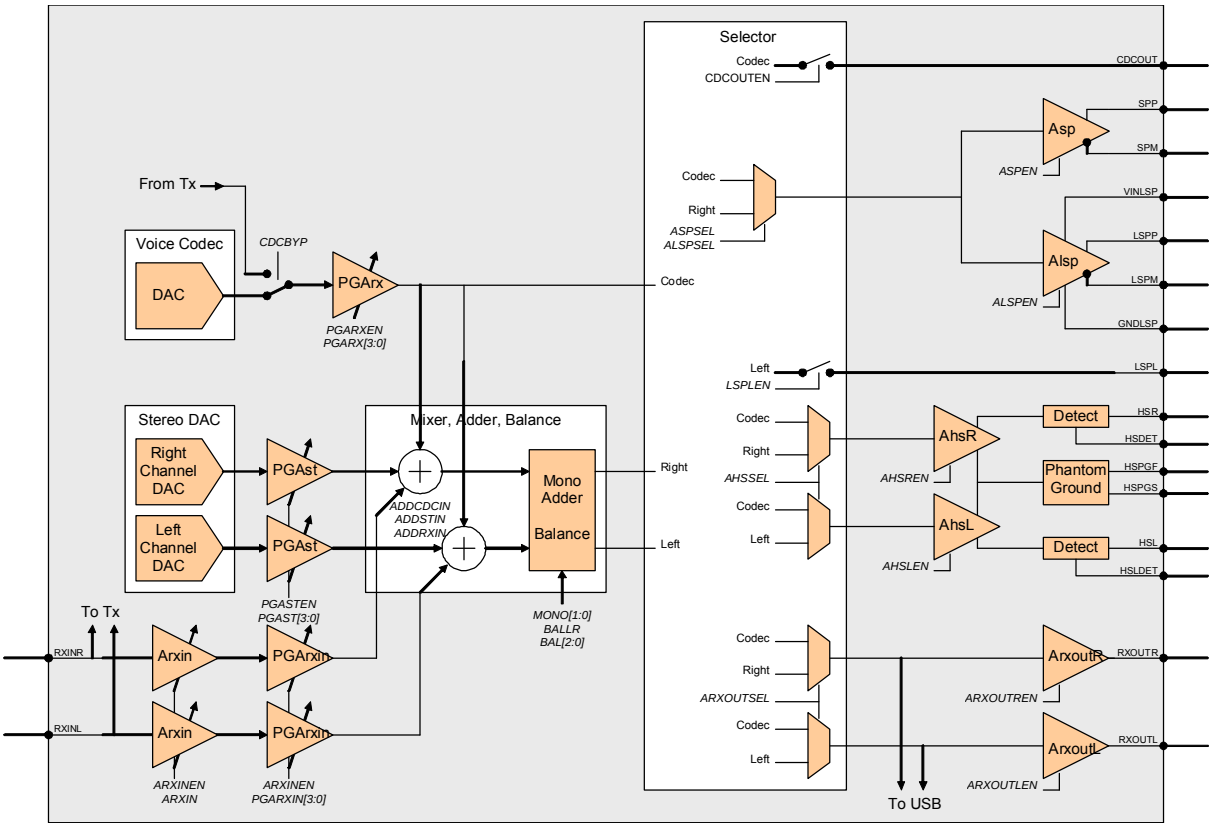


Figure 7-12. Audio Output Section Diagram

Four signal sources can be used in the receive path. The voice CODEC receive signal, the voice CODEC transmit signal (for test purposes), the stereo DAC and an external stereo source like an FM radio. The latter can also be routed to the voice CODEC ADC section for recording purposes. Each of the input source signals is amplified via an independently programmable gain amplifier. The amplified signals are fed into a mixer where the different signals can be mixed. The mixed signal goes through a mono adder and balance circuit which can create a mono signal out of the stereo input signals, and allows for balance control. Via the selector, the composite signal is then directed to one or more of the outputs. These are the regular phone ear piece (Asp), the loudspeaker for hands free or ringing (Alsp), the stereo headset (Ahsr, Ahsl) and the stereo line out. The voice CODEC output signal can also follow an independent route to all of the amplifiers via the additional selector inputs. In addition to the amplifiers, low-power outputs are available at LSPL and CDCOUT.

7.5.2 Programmable Gain Amplifiers

The gain of the audio in both left and right channels is independently controlled in the programmable gain amplifiers to allow for balance control. The input level from the external stereo source can be pre-amplified by Arxin and the programmable gain amplifier PGArxin to get it at the same level as the other sources before going into the audio input mixer block.

Table 7-28. PGA Control Bit Definition

Name	Description
PGARXEN	CODEC Receive PGA enable
PGARX[3:0]	CODEC Receive PGA gain (-33 dB to +6 dB by 3 dB steps)
PGASTEN	Stereo DAC PGA enable
PGAST[3:0]	Stereo DAC PGA gain (-33 dB to +6 dB by 3 dB steps)
ARXINEN	Arxin and PGArxin enable
ARXIN	Arx gain (+0 dB or +18 dB)
PGARXIN[3:0]	PGArxin gain (-33 dB to +6 db by 3 dB steps)

Table 7-29. PGA Gain Setting

PGAxy3	PGAxy2	PGAxy1	PGAxy0	Gain (in dB)
0	0	0	0	-33
0	0	0	1	-33
0	0	1	0	-33
0	0	1	1	-30
0	1	0	0	-27
0	1	0	1	-24
0	1	1	0	-21
0	1	1	1	-18
1	0	0	0	-15
1	0	0	1	-12
1	0	1	0	-9
1	0	1	1	-6
1	1	0	0	-3
1	1	0	1	0
1	1	1	0	+3
1	1	1	1	+6
PGAxy stands for PGARX, PGAST, PGARXIN. Default value is 1101 or 0 dB.				

Table 7-30. PGA Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
PGA Gain Setting Accuracy	Relative to 0 dB setting		-0.3	—	+0.3	dB
PSRR	With respect to BP 20 Hz – 20 kHz inputs AC grounded, A Weighted		90	—	—	dB
THD (2^{nd} and 3^{rd})	gain = 0 dB	V_{OUT} = $1V_{PP}$	—	—	0.1	%
		V_{OUT} = 100 mV_{RMS}	—	—	0.1	%
		V_{OUT} = 10 mV_{RMS}	—	—	0.1	%
Supply Current	Per Channel		—	—	300	uA
Output Noise	gain = 0 dB, A weighted 20 Hz - 20 kHz Per output		—	15	20	uV_{RMS}
Input Impedance	RXINR, RXINL		40	50	60	kΩ

7.5.3 Balance, Mixer, Mono Adder and Selector Block

The mixer is basically a summing amplifier where the different input signals can be summed. The relative level between the input signals is to be controlled via the PGArx, PGAst, and PGArxin amplifiers respectively.

The mono adder in the stereo channel can be used in four different modes: stereo (right and left channel independent), stereo opposite (left channel in opposite phase), mono (right and left channel added), mono opposite (as mono but with outputs in opposite phase).

The balance control allows for attenuating either the right or the left channel with respect to the other channel. The balance control setting is applied independent of which input channel is selected.

The selector opens the audio path to the audio amplifiers and can be seen as an analog switch. Summing of the output signals from the mono selector and the stereo selector is not allowed at this point, that must be done in the mixer stage. Each selector allows enabling up to two output amplifiers at each channel at the same time for the same input source. When routing to multiple amplifiers, for instance the voice CODEC signal to the ear piece amplifier Asp and the stereo DAC signal to the stereo headset amplifiers Ahsr and Ahsl, care has to be taken not to exceed the load current capability of the VAUDIO regulator.

Table 7-31. Balance, Mono Adder and Mixer Block Main Performance Specifications

Parameter	Target
Balance Control	-21 dB to 0 dB in 3 dB steps, left or right channel selection
Gain spread	0.3 dB
Bias Current	300 uA per channel

Table 7-32. Balance, Mono Adder and Mixer Block Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
PGA Gain Setting Accuracy	Relative to 0 dB setting		-0.3	—	+0.3	dB
PSRR	With respect to BP 20 Hz – 20 kHz, inputs AC grounded, A Weighted		90	—	—	dB
THD (2^{nd} and 3^{rd})	Gain = 0 dB	V_{OUT} = 1 V_{PP}	—	—	0.1	%
		V_{OUT} = 100 mV_{RMS}	—	—	0.1	%
		V_{OUT} = 10 mV_{RMS}	—	—	0.1	%
Supply Current	Per Channel		—	—	300	uA
Output Noise	Gain = 0 dB, A weighted 20 Hz - 20k Hz Per output		—	7	10	uV_{RMS}

Table 7-33. PGA Control Bit Definition

Name	Description
ADDCDCIN	Selects PGARX Voice CODEC Output
ADDSTIN	Selects PGAST Stereo DAC Outputs
ADDRXIN	Selects PGArxIn Line in Outputs
MONO[1:0]	00: Left and Right Channels independent 01: Stereo Opposite (Left Channel in opposite phase) 10: Stereo to Mono Conversion (Left and Right Channels added and routed to both outputs. The channel addition only applies to Stereo DAC and RXIN inputs.) 11: Mono Opposite (Left and Right channels added and routed to right output, the opposite routed to left output. The channel addition only applies to Stereo DAC and RXIN inputs.)
BAL[2:0]	Balance attenuation setting: -21 dB to 0 dB in 3 dB steps
BALLR	Channel selection for attenuation 0: Right Channel 1: Left Channel

Table 7-34. Balance Control Settings

BALLR	BAL2	BAL1	BAL0	Attenuation (in dB)
0	0	0	0	0
0	0	0	1	-3
0	0	1	0	-6
0	0	1	1	-9
0	1	0	0	-12
0	1	0	1	-15
0	1	1	0	-18
0	1	1	1	-21

Table 7-34. Balance Control Settings (continued)

BALLR	BAL2	BAL1	BAL0	Attenuation (in dB)
1	0	0	0	0
1	0	0	1	-3
1	0	1	0	-6
1	0	1	1	-9
1	1	0	0	-12
1	1	0	1	-15
1	1	1	0	-18
1	1	1	1	-21
Default value is 0000 or 0 dB				

Table 7-35. Amplifiers Control Bit Definition

Name	Description
ASPSEL	Asp input selector 0 = CODEC, 1 = Right
ALSPSEL	Alsp input selector 0 = CODEC, 1 = Right
AHSSEL	Ahs input selector 0 = CODEC, 1 = Right / Left
ARXOUTSEL	Arxout input selector 0 = CODEC, 1 = Right / Left
ASPEN	Amplifier Asp enable
ALSPEN	Amplifier Alsp enable
ALSPREF	Bias Alsp at common audio reference
LSPLEN	Output LSPL enable
AHSREN	Amplifier AhsR enable
AHSLEN	Amplifier AhsL enable
HSPGDIS	Phantom ground disable
HSDETEN	Headset detect enable
HSDETAUTOB	Amplifier state determined by headset detect 0 = function enabled, 1 = function disabled
ARXOUTREN	Output RXOUTR enable
ARXOUTLEN	Output RXOUTL enable
CDCOUTEN	Output CDCOUT enable

Table 7-36. Output Contingency Matrix

ASPEN	ALSPEN	Selector	Routing
0	0	None	None
0	1	ALSPSEL	Alsp
1	0	ASPSEL	Asp
1	1	ASPSEL	Asp

7.5.4 Ear Piece Speaker Amplifier Asp

The Asp amplifier drives the ear piece of the phone in a bridge tied load configuration. The feedback network of the Asp amplifier is fully integrated.

Table 7-37. Amplifier Asp Performance Specifications

Parameter	Condition		Minimum	Typical	Maximum	Units
Differential Output Swing			4.0	—	—	V_{PP}
Supply Current	No load Including Single to Differential Stage		—	2.25	2.75	mA
Bias Center Voltage			—	REFA	—	V
Input Referred Offset Voltage	Single Ended Includes Single to Differential Stage		—	—	2	mV
Isolation in OFF mode			80	—	—	dB
Gain	Single Ended, 1.0 kHz, Vin = 100 mVpp		3.8	4.0	4.2	dB
THD (2^{nd} and 3^{rd})	1.0 kHz	V_{OUT} = 2 Vp	—	—	0.1	%
		V_{OUT} = 100 mVp	—	—	0.1	%
		V_{OUT} = 10 mVp	—	—	0.1	%
PSRR	With respect to BP, 20 Hz – 20 kHz inputs AC grounded, A Weighted		90	—	—	dB
Slew rate			0.4	—	—	V/µs
Startup Time			—	—	1	ms
Input Noise	A weighted, Including PGA Noise		—	—	20	μV_{RMS}
Closed Loop -3dB Point			40	—	—	kHz
Load Impedance	Resistance Inductance Capacitance		— — —	16 — —	— 1 100	Ω mH pF

7.5.5 Loudspeaker Amplifier Alsp

The concept of the Alsp amplifier is especially developed to be able to drive one loudspeaker during handset, speakerphone and alert modes. It adopts a fully differential topology in order to be able to reach high PSRR performance while Alsp is powered directly by the telephone battery. In order to get the

maximum swing in speakerphone operation, Alsp uses a dedicated common mode voltage equal to the battery voltage divided by two. Optionally, the reference REFA can be used. The feedback network of the Alsp amplifier is fully integrated.

A low-power output is available at LSPL with the left channel signal. This allows for stereo loud speaking applications in conjunction with an additional discrete loudspeaker amplifier. By default, the LSPL output is in opposite phase of the loudspeaker amplifier ALSP. Therefore, when using a discrete inverting loudspeaker connected to LSPL, its positive output will get in phase with the ALSP outputs.

A low-power output is available at CDCOUT with the voice CODEC signal. This allows for connecting to an additional discrete amplifier for driving a speaker vibrator or other transducer.

Under worst case conditions the dissipation of Alsp is considerable. To protect the amplifier against overheating, a thermal protection is included which clears the ALSPEN bit, and therefore effectively shuts down the amplifier, when the maximum allowable junction temperature within Alsp is reached. An interrupt ALSPTHI is generated at the same time. The thermal protection is not debounced.

Table 7-38. Amplifier Alsp Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Differential Output Swing	BP = 3.05 V		5.0	—	—	V_{PP}
	BP = 3.4 V in 8 Ω[1]		5.6	—	—	V_{PP}
Supply Voltage			3.05	—	4.65	V
Supply Current	No load Including Single to Differential Stage		—	4	7	mA
Bias Center Voltage	ALSPREF = 0		—	BP/2	—	V
	ALSPREF = 1		—	REFA	—	V
Temperature ShutDown Interrupt			125	—	—	°C
Input Referred Offset Voltage	Single Ended Includes Single to Differential Stage		—	—	2	mV
Isolation in OFF Mode[2]			80	—	—	dB
Gain[3]	1.0 kHz, Vin = 100 mVpp		5.8	6	6.2	dB
THD (2nd and 3rd)	1.0 kHz, BP = 3.4 V	V_{OUT} = 5 Vpp	—	3	5	%
	1.0 kHz, BP = 4 V	V_{OUT} = 5 Vpp	—	1	3	%
	1.0 kHz	V_{OUT} = 1 Vpp	—	—	0.1	%
	1.0 kHz	Vout = 10 mVrms	—	—	0.1	%
PSRR	With respect to BP, 20 Hz – 20 kHz inputs AC grounded, A Weighted		90	—	—	dB
Slew Rate[3]	—		0.4	—	—	V/µs
Startup Time[3]	—		—	—	1	ms
Input Noise	A weighted		—	—	20	$µV_{RMS}$

Table 7-38. Amplifier Alsp Performance Specifications (continued)

Parameter	Condition	Min	Typ	Max	Units
Closed Loop -3dB Point [3]		40	—	—	kHz
Load Impedance	Resistance Inductance Capacitance	6.4 — —	8 — —	38 400 200	Ω µH pF
Note: Unless otherwise noted, the load impedance is 6.8 Ω bridged. Unless otherwise noted, the measurements are made differentially.					

1 Equivalent to 500 mW.

2 Measured as the difference between the amplifier being on and off, includes PGA.

3 Measured single ended.

Table 7-39. LSPL, CDCOUT Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Gain	1.0 kHz, Vin = 100 mVpp		-0.3	0	+0.3	dB
Single Ended Output Swing			2	2.2	—	Vpp
PSRR	with respect to BP 20 Hz – 20 kHz inputs AC grounded, A Weighted		90	—	—	dB
THD (2^{nd} and 3^{rd})	Gain = 0dB	V_{OUT} = 1 V_{PP}	—	—	0.1	%
		V_{OUT} = 100 mV_{RMS}	—	—	0.1	%
		V_{OUT} = 10 mV_{RMS}	—	—	0.1	%
External Load Impedance	At any PGA output		10 —	—	— 50	kΩ pF
Supply Current			—	—	300	uA
Output Noise	Gain = 0 dB, A weighted 20 Hz - 20 kHz. Per output		—	15	20	uV_{RMS}

7.5.6 Headset Amplifiers Ahsr/Ahsl

The Ahsr and Ahsl amplifiers are dedicated for amplification to a stereo headset, the Ahsr for the right channel and Ahsl for the left channel. Ahsr and Ahsl can also be configured for a bridged tied mono operation. In that case, the mono adder is used to generate the opposite phase signals. The feedback networks are fully integrated.

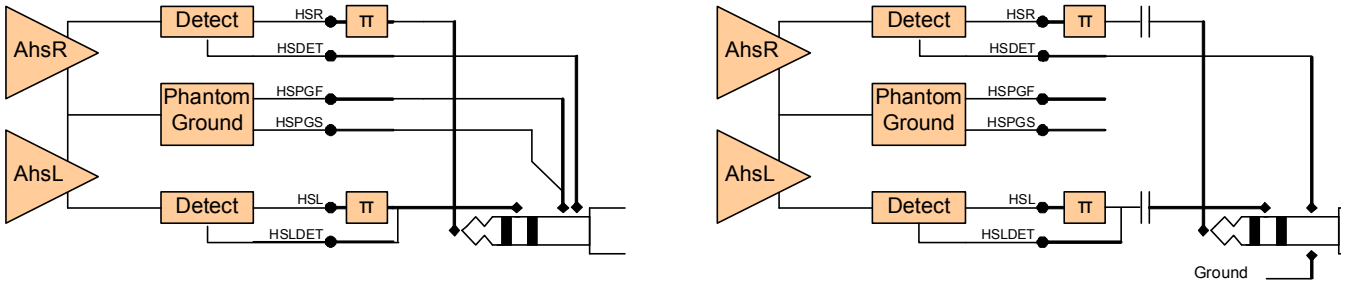
The return path of the headset is provided by the phantom ground which is at the same DC voltage as the bias of the headset amplifiers. This avoids the use of large sized capacitors in series with the headset speakers. To obtain the proper performance, the phantom ground has a force and sense arrangement. To avoid excessive current drain, the right and left channels can be driven in opposite phase in one of the mono adder modes. All outputs withstand shorting to ground or to phantom ground which is detected as an overload condition if this lasts longer than the debounce time. In that case, the logic will disable the amplifier by clearing the AHSREN and AHSLEN bits, including phantom ground generation, and an interrupt AHSSHORTI is generated.

Table 7-40. Amplifiers Ahsr and Ahsl Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Singled-Ended Output Swing	32 Ohm load		2	2.2	—	V_{PP}
	16 Ohm load		1.6	1.8	—	V_{PP}
Bias Center Voltage	—		—	REFA	—	V
Supply Current per Amplifier	—		—	750	1000	uA
Isolation in OFF mode[1]	—		80	—	—	dB
Gain	1.0 kHz, Vin = 100 mVpp		-0.2	0	0.2	dB
THD (2^{nd} and 3^{rd})	1.0 kHz	V_{OUT} = 1 V_{PP}	—	0.03	0.1	%
		V_{OUT} = 10 mV_{RMS}	—	0.03	0.1	%
PSRR	With respect to BP, 20 Hz – 20 kHz inputs AC grounded, A Weighted		90	—	—	dB
Slew Rate	—		1.0	—	—	V/us
Input Noise	A weighted		—	—	20	μV_{RMS}
Closed Loop -3dB Point	—		40	—	—	kHz
Load Impedance	Resistance Inductance Capacitance Single Ended Capacitance Bridged		12.8 — — —	16 — — —	38 400 1.5 750	Ω µH nF pF
Overload Detection Level	—		—	150	—	mA
Overload Detection Debounce Time	—		—	30	—	ms

1 Measured as the output signal difference between the amplifier being on and off.

In non phantom ground type of applications, so with the headset AC coupled and referenced to the phone ground, the phantom ground outputs HSPGF and HSPFS can be left open while setting the HSPGDIS bit to 1. Figure 7-13 shows the connection scheme for these two applications including the EMI Pi filter placement.



Headset Connection with Phantom Ground

Headset Connection with System Ground

Figure 7-13. Headset Connection

Different type of headsets and wiring schemes do exist for mobile phones. The three main headset types are the mono headset or ear bud, the stereo headset, and stereo headphones. The wiring schemes have a very wide variety ranging from 3-wire to 5-wire for the standard headsets and even more for non standard headsets with supply and command lines. The MC13783 provides a headset detection scheme based on the sleeve detection, left channel impedance detection and microphone bias detection which is valid for headsets with or without phantom ground connection. It is compatible with mono headsets where the left channel is connected to ground.

First of all, the insertion and removal of a headset is monitored by a built in DC circuit which is triggered by the HSDET pin without the need of additional external components. An internal pull up will make HSDET equals VAUDIO when no headset is present. If HSDET goes low, meaning to ground or to phantom ground, a headset is present. The state of the HSDET is monitored via the HSDETS sense bit. Any change in HSDETS, so upon detection of insertion and removal, an interrupt HSDETI is generated after the standard debounce time, see Chapter 3, “Programmability”.

After a headset is detected, two scenarios are possible to detect if the present headset is mono or stereo, dependent upon the fact if the audio bias was already enabled or not. If the audio bias was already enabled, a low-power detector is enabled at the left channel via the output HSLDET if programming the bit HSLDETEN=1. The output HSLDET is to be connected to the left channel output right after the EMI filter but before the coupling capacitor (if any). If an impedance is detected, DC or AC, an interrupt HSLI is generated. The detector is disabled only after programming HSLDETEN=0. If the audio bias was not yet enabled, software has to do so via SPI by setting bit BIASEN=1 while at the same time setting HSLDETEN=1. Then right at the end of the ramping, the MC13783 will perform the left channel impedance detection. In both cases the detection can only be done when the Ahsl amplifier is disabled.

If a stereo headset is detected the HSLS will become 1 and an interrupt HSLI is generated. The HSLS bit reflects the state of the detection and will revert to zero when the detector is disabled. This will generate again a HSLI interrupt which must be ignored by software. Upon headset removal a HSDETI is generated because HSDETS goes low, however not a new HSLI is generated since HSLS was already low and will not change state. There is no debounce on the HSLI interrupt.

In order to save current the audio bias does not have to be enabled for detection as long as VAUDIO is enabled (in low-power mode). When the HSDETEN bit is not set, or when the MC13783 is powered down, no detection is active.

When a headset is removed, and HSDETS goes low, the headset speaker amplifiers Ahsr and Ahsl are automatically turned off if the HSDETAUTOB bit is a zero (default). The enable bits AHSREN and AHSLEN however, are not reset until the debounce timer expires - which coincides with the generation of the HSDETI. When the HSDETS goes high within the debounce period, and stays high, the amplifiers will be enabled again immediately. The amplifiers are not automatically turned on upon detection. The phantom ground generation is automatically disabled upon headset removal as long as HSDETS remains low but the HSPGDIS bit is not automatically reset, even when the debounce period expires. If the HSDETAUTOB bit is set to a one, this function is disabled.

7.5.7 Line Output Amplifier Arxout

The Arxout amplifier combination is a low-power stereo amplifier. It can provide the stereo signal to for instance an accessory connector. The same output of the selector block is used for the internal connection to the USB transceiver for CEA-936-A Carkit support. The selection of the USB source therefore is done with the ARXOUTSEL bit. For more details see Chapter 10, "Connectivity".

Table 7-41. Arx Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Gain	1.0 kHz, Vin = 100 mVpp		-0.2	0	+0.2	dB
Single Ended Output Swing	Includes reverse bias protection purpose		1.8	2	—	Vpp
PSRR	With respect to BP 20 Hz – 20 kHz inputs AC grounded, A Weighted		90	—	—	dB
THD (2^{nd} and 3^{rd})	Gain = 0 dB	V_{OUT} = 1 V_{PP}	—	—	0.1	%
		V_{OUT} = 100 mV_{RMS}	—	—	0.1	%
		V_{OUT} = 10 mV_{RMS}	—	—	0.1	%
External Load Impedance	At any PGA output		1 —	— —	— 500	kΩ pF
Supply Current	—		—	—	500	uA
Output Noise	Gain = 0 dB, A weighted 20 Hz–20 kHz per output		—	15	20	uV_{RMS}

7.6 Audio Control

7.6.1 Supply

The audio section is supplied from a dedicated regulator VAUDIO, except for the loudspeaker amplifier Alsp which is directly supplied from the battery. A low-power standby mode controlled by the standby pins is provided for VAUDIO in which the bias current is reduced. The output drive capability and performance are limited in this mode. The nominal output voltage for VAUDIO is 2.775 V.

Table 7-42. Audio Regulator VAUDIO Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	—	Vnom + 0.3	—	4.65	V
Operating Current Load Range ILmin to ILmax	—	0	—	200	mA
Extended Input Voltage Range	Performance may be out of specification	2.5	—	4.65	V
	Output voltage stays within +/-50 mV accuracy	Vnom+0.2	—	4.65	V
Bypass Capacitor Value	—	-35%	1.0	+35%	uF

Table 7-42. Audio Regulator VAUDIO Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom – 3%	Vnom	Vnom + 3%	V
Load Regulation	1 mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	5	8	mV
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	300	—	600	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	uA
Low-Power Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILminlp < IL < ILmaxlp	Vnom - 3%	Vnom	Vnom + 3%	
Current Load Range ILminlp to ILmaxlp	—		—	3	mA
Low-Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	uA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	50	60	—	dB
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100Hz – 1kHz	—	20	—	dB/dec
	1kHz – 1MHz	—	—	1	uV/√Hz
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%

Table 7-42. Audio Regulator VAUDIO Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Mode Transition Time	From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	—	10	us
Mode Transition Response	From low-power to active and from active to low-power Vin = Vinmin, Vinmax IL = ILmaxlp	—	1	2	%

7.6.2 Bias and Anti Pop

The audio blocks have a bias which can be enabled separately from the rest of the MC13783 by setting the BIASEN bit. When enabled, the audio bias voltage REFA can be ramped fast or slow to make any pop sub audio and therefore not audible. While the audio bias is ramping up, the audio blocks using the audio bias will not be enabled. When the audio references reach their end value, audio amplifiers are enabled. Only after this the programmed audio signal path will be established. For headset detection the bias can be left disabled as long as VAUDIO is enabled in normal or low-power mode.

A quick rising bias can cause an audible pop at the transducers. Mechanisms are in place to avoid such pops. For the ear piece and speaker amplifiers Asp and Alsp the speakers are connected in bridge and the fully differential structure will avoid pops. The headset amplifiers Ahsr and Ahsl, when used with a phantom ground, are connected as a bridge as well. In case of non phantom ground use the outputs follow the ramping bias. The line outputs Arxout and the loudspeaker left channel preamplifier output Alsps will also follow the ramping bias voltage. This will make that the output capacitor will be charged slowly which avoids audible pops.

The voice CODEC and the stereo DAC must not be programmed before the bias at REFA has been established, otherwise its programming is not taken into account properly.

To avoid pops and significant DC current flow though the transducers, the output offset of the voice CODEC and the stereo DAC is minimized by an offset correction.

Table 7-43. Audio Bias and Anti Pop Main Performance Specifications

Parameter	Target
Reference for Analog blocks in audio path, REFA	1.3875 V
Local bandgap reference for Audio blocks, REFB	1.200 V
Turn On time (BIASEN 0 ◊ 1), Capacitors at REFA and REFC are 100 nF BIASSPEED = 0 (default) BIASSPEED = 1	 100 ms min – 250 ms max 25 ms max

Table 7-43. Audio Bias and Anti Pop Main Performance Specifications (continued)

Parameter	Target
Bias Current References including VAUDIO	200 uA typ
Residual offset per (differential) amplifier output Stereo DAC path Voice CODEC path Line in path	 20 mV max 20 mV max 40 mV max

7.6.3 Arbitration Logic

The audio functions can be operated by both the primary and secondary SPI. At startup the primary SPI may assign the audio registers to the secondary SPI. The options for the audio amplifier non vector bits are primary SPI only, secondary SPI only, dual control with OR function (one or both SPIs can enable a function by setting the bit to 1), and dual control with AND function (both SPIs have to set a 1). Vector bits are assigned to one of the SPI busses independent of the rest of the register. The voice CODEC and stereo DAC functions do not have dual control capability and have to be assigned to the primary or secondary SPI.

Table 7-44. Audio Arbitration Bits

Bits	Description	Bits Concerned
AUDIOTXSEL[1:0]	Transmit audio amplifiers assignment 00 = Primary SPI only 01 = Secondary SPI only 10 = OR-ing of both SPIs 11 = AND-ing of both SPIs	Reg 38, bits 0-13
TXGAINSEL	Transmit gain assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 38, bits 14-23
AUDIORXSEL[1:0]	Receive audio amplifiers assignment 00 = Primary SPI only 01 = Secondary SPI only 10 = OR-ing of both SPIs 11 = AND-ing of both SPIs	Reg 36, bits 3-23
RXGAINSEL	Receive gain assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 37, bits 0-21
AUDIOCDCSEL	CODEC assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 40, bits 0-20 Reg 39, bits 0-11

Table 7-44. Audio Arbitration Bits (continued)

Bits	Description	Bits Concerned
AUDIOSTDCSEL	Stereo DAC assignment 0 = Primary SPI only 1 = Secondary SPI only	Reg 41, bits 0-20 Reg 39, bits 12-21
BIASSEL[1:0]	Audio bias assignment 00 = Primary SPI only 01 = Secondary SPI only 10 = OR-ing of both SPIs 11 = AND-ing of both SPIs	Reg 36, bits 0-2

An additional arbitration mechanism is implemented for the enabling of VAUDIO by means of the VAUDIOON bit which resides in the audio control registers. If this bit is set to a 0 then the power mode for VAUDIO is selected based on the setting of VAUDIOEN, VAUDIOMODE and VAUDIOSTBY bits. If this bit is set to a 1 then regardless of the other bit settings, the VAUDIO is forced in on mode. Table 7-45 provides a summary of the VAUDIOON bit function for a single SPI control. In case of dual SPI control the highest power mode as requested by both SPI busses is applied, see Chapter 5, “Power Control System”.

Table 7-45. VAUDIO Forced Enable Function

VAUDIOEN	VAUDIOMODE	VAUDIOSTBY	STANDBY pin	AUDIOON	VAUDIO
0	X	X	X	0	Off
1	0	0	X	0	On
1	1	0	X	0	Low-Power
1	X	1	0	0	On
1	0	1	1	0	Off
1	1	1	1	0	Low-Power
X	X	X	X	1	On

7.6.4 Audio Register Summary

Table 7-46. Register 36, Audio Rx 0

Name	Bit #	R/W	Reset	Default	Description
VAUDIOON	0	R/W	RESETB	0	Forces VAUDIO in active on mode
BIASEN	1	R/W	RESETB	0	Audio bias enable
BIASSPEED	2	R/W	RESETB	0	Turn on ramp speed of the audio bias
ASPEN	3	R/W	RESETB	0	Amplifier Asp enable
ASPSEL	4	R/W	RESETB	0	Asp input selector
ALSPEN	5	R/W	RESETB	0	Amplifier Alsp enable
ALSPREF	6	R/W	RESETB	0	Bias Alsp at common audio reference

Table 7-46. Register 36, Audio Rx 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
ALSPSEL	7	R/W	RESETB	0	Alsp input selector
LSPLEN	8	R/W	RESETB	0	Output LSPL enable
AHSREN	9	R/W	RESETB	0	Amplifier AhsR enable
AHSLEN	10	R/W	RESETB	0	Amplifier AhsL enable
AHSSEL	11	R/W	RESETB	0	Ahsr and Ahsl input selector
HSPGDIS	12	R/W	RESETB	1	Phantom ground disable
HSDETEN	13	R/W	RESETB	0	Headset detect enable
HSDETAUTOB	14	R/W	RESETB	0	Amplifier state determined by headset detect
ARXOUTREN	15	R/W	RESETB	0	Output RXOUTR enable
ARXOUTLEN	16	R/W	RESETB	0	Output RXOUTL enable
ARXOUTSEL	17	R/W	RESETB	0	Arxout input selector
CDCOUTEN	18	R/W	RESETB	0	Output CDCOUT enable
HSLDETEN	19	R/W	RESETB	0	Headset left channel detect enable
Reserved	20	R/W	RESETB	0	For future use
ADDCDC	21	R/W	RESETB	0	Adder channel CODEC selection
ADDSTDC	22	R/W	RESETB	0	Adder channel stereo DAC selection
ADDRXIN	23	R/W	RESETB	0	Adder channel line in selection

Table 7-47. Register 37, Audio Rx 1

Name	Bit #	R/W	Reset	Default	Description
PGARXEN	0	R/W	RESETB	0	CODEC receive PGA enable
PGARX0	1	R/W	RESETB	1	CODEC receive gain setting
PGARX1	2	R/W	RESETB	0	
PGARX2	3	R/W	RESETB	1	
PGARX3	4	R/W	RESETB	1	
PGASTEN	5	R/W	RESETB	0	Stereo DAC PGA enable
PGAST0	6	R/W	RESETB	1	Stereo DAC gain setting
PGAST1	7	R/W	RESETB	0	
PGAST2	8	R/W	RESETB	1	
PGAST3	9	R/W	RESETB	1	
ARXINEN	10	R/W	RESETB	0	Amplifier Arx enable
ARXIN	11	R/W	RESETB	0	Amplifier Arx additional gain setting

Table 7-47. Register 37, Audio Rx 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
PGARXIN0	12	R/W	RESETB	1	PGArxin gain setting
PGARXIN1	13	R/W	RESETB	0	
PGARXIN2	14	R/W	RESETB	1	
PGARXIN3	15	R/W	RESETB	1	
MONO0	16	R/W	RESETB	0	Mono adder setting
MONO1	17	R/W	RESETB	0	
BAL0	18	R/W	RESETB	0	Balance control
BAL1	19	R/W	RESETB	0	
BAL2	20	R/W	RESETB	0	
BALLR	21	R/W	RESETB	0	Left / right balance
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 7-48. Register 38, Audio Tx

Name	Bit #	R/W	Reset	Default	Description
MC1BEN	0	R/W	RESETB	0	Microphone bias 1 enable
MC2BEN	1	R/W	RESETB	0	Microphone bias 2 enable
MC2BDETDBNC	2	R/W	RESETB	0	Microphone bias detect debounce setting
MC2BDETEN	3	R/W	RESETB	0	Microphone bias 2 detect enable
Reserved	4	R/W	RESETB	0	For future use
AMC1REN	5	R/W	RESETB	0	Amplifier Amc1R enable
AMC1RITOV	6	R/W	RESETB	0	Amplifier Amc1R current to voltage mode enable
AMC1LEN	7	R/W	RESETB	0	Amplifier Amc1L enable
AMC1LITOV	8	R/W	RESETB	0	Amplifier Amc1L current to voltage mode enable
AMC2EN	9	R/W	RESETB	0	Amplifier Amc2 enable
AMC2ITOV	10	R/W	RESETB	0	Amplifier Amc2 current to voltage mode enable
ATXINEN	11	R/W	RESETB	0	Amplifier Atxin enable
ATXOUTEN	12	R/W	RESETB	0	Reserved for output TXOUT enable, currently not used
RXINREC	13	R/W	RESETB	0	RXINR/RXINL to voice CODEC ADC routing enable

Table 7-48. Register 38, Audio Tx (continued)

Name	Bit #	R/W	Reset	Default	Description
PGATXR0	14	R/W	RESETB	0	Transmit gain setting right
PGATXR1	15	R/W	RESETB	0	
PGATXR2	16	R/W	RESETB	0	
PGATXR3	17	R/W	RESETB	1	
PGATXR4	18	R/W	RESETB	0	
PGATXL0	19	R/W	RESETB	0	Transmit gain setting left
PGATXL1	20	R/W	RESETB	0	
PGATXL2	21	R/W	RESETB	0	
PGATXL3	22	R/W	RESETB	1	
PGATXL4	23	R/W	RESETB	0	

Table 7-49. Register 39, SSI Network

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R/W	RESETB	0	For future use
Reserved	1	R/W	RESETB	0	For future use
CDCTXRXSLOT0	2	R/W	RESETB	0	CODEC time slot assignment
CDCTXRXSLOT1	3	R/W	RESETB	0	
CDCTXSECSLOT0	4	R/W	RESETB	0	CODEC secondary transmit time slot
CDCTXSECSLOT1	5	R/W	RESETB	1	
CDCRXSECSLOT0	6	R/W	RESETB	1	CODEC secondary receive time slot
CDCRXSECSLOT1	7	R/W	RESETB	0	
CDCRXSECGAIN0	8	R/W	RESETB	0	CODEC secondary receive channel gain setting
CDCRXSECGAIN1	9	R/W	RESETB	0	
CDCSUMGAIN	10	R/W	RESETB	0	CODEC summed receive signal gain setting
CDCFSDLY	11	R/W	RESETB	0	CODEC framesync delay
STDCSLOTS0	12	R/W	RESETB	1	Stereo DAC number of time slots select
STDCSLOTS1	13	R/W	RESETB	1	
STDCRXSLOT0	14	R/W	RESETB	0	Stereo DAC time slot assignment
STDCRXSLOT1	15	R/W	RESETB	0	
STDCRXSECSLOT0	16	R/W	RESETB	1	Stereo DAC secondary receive time slot
STDCRXSECSLOT1	17	R/W	RESETB	0	
STDCRXSECGAIN0	18	R/W	RESETB	0	Stereo DAC secondary receive channel gain setting
STDCRXSECGAIN1	19	R/W	RESETB	0	

Table 7-49. Register 39, SSI Network (continued)

Name	Bit #	R/W	Reset	Default	Description
STDCSUMGAIN	20	R/W	RESETB	0	Stereo DAC summed receive signal gain setting
Reserved	21	R/W	RESETB	0	For future use
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 7-50. Register 40, Audio CODEC

Name	Bit #	R/W	Reset	Default	Description
CDCSSISEL	0	R/W	RESETB	1	CODEC SSI bus select
CDCCLKSEL	1	R/W	RESETB	1	CODEC clock input select
CDCSM	2	R/W	RESETB	1	CODEC slave / master select
CDCBCLINV	3	R/W	RESETB	0	CODEC bit clock inversion
CDCFSINV	4	R/W	RESETB	0	CODEC framesync inversion
CDCFS0	5	R/W	RESETB	1	Bus protocol selection
CDCFS1	6	R/W	RESETB	0	
CDCCLK0	7	R/W	RESETB	0	CODEC clock setting
CDCCLK1	8	R/W	RESETB	0	
CDCCLK2	9	R/W	RESETB	0	
CDCFS8K16K	10	R/W	RESETB	0	CODEC framesync select
CDCEN	11	R/W	RESETB	0	CODEC enable
CDCCLKEN	12	R/W	RESETB	0	CODEC clocking enable
CDCTS	13	R/W	RESETB	0	CODEC SSI tristate
CDCDITH	14	R/W	RESETB	0	CODEC dithering
CDCRESET	15	R/W	RESETB	0	CODEC filter reset
CDCBYP	16	R/W	RESETB	0	CODEC bypass
CDCALM	17	R/W	RESETB	0	CODEC analog loopback
CDCDLM	18	R/W	RESETB	0	CODEC digital loopback
AUDIHPF	19	R/W	RESETB	1	Transmit high pass filter enable
AUDOHPF	20	R/W	RESETB	1	Receive high pass filter enable
Unused	21	R/W	RESETB	0	Not available
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Table 7-51. Register 41, Audio Stereo DAC

Name	Bit #	R/W	Reset	Default	Description
STDCSSISEL	0	R/W	RESETB	0	Stereo DAC SSI bus select
STDCCLKSEL	1	R/W	RESETB	0	Stereo DAC clock input select
STDCSM	2	R/W	RESETB	1	Stereo DAC slave / master select
STDCBCLINV	3	R/W	RESETB	0	Stereo DAC bit clock inversion
STDCFSINV	4	R/W	RESETB	0	Stereo DAC framesync inversion
STDCFS0	5	R/W	RESETB	0	Bus protocol selection
STDCFS1	6	R/W	RESETB	0	
STDCCLK0	7	R/W	RESETB	0	Stereo DAC clock setting
STDCCLK1	8	R/W	RESETB	0	
STDCCLK2	9	R/W	RESETB	0	
STDCFSDLYB	10	R/W	RESETB	0	Stereo DAC framesync delay bar
STDCEN	11	R/W	RESETB	0	Stereo DAC enable
STDCCLKEN	12	R/W	RESETB	0	Stereo DAC clocking enable
Reserved	13	R/W	RESETB	0	For future use
Reserved	14	R/W	RESETB	0	For future use
STDCRESET	15	R/W	RESETB	0	Stereo DAC filter reset
SPDIF	16	R/W	RESETB	0	Stereo DAC SSI SPDIF mode. Mode no longer available.
SR0	17	R/W	RESETB	1	Stereo DAC sample rate
SR1	18	R/W	RESETB	1	
SR2	19	R/W	RESETB	1	
SR3	20	R/W	RESETB	0	
Unused	21	R/W	RESETB	0	Not available
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Chapter 8
Battery Interface and Control

8.1 Introduction

The battery interface is optimized for single charger input coming from a standard wall charger or from a USB bus. The MC13783 charger has been designed to support three different configurations where the charger and USB bus share the same input pin (CHRGRAW): these are Dual Path Charging, Serial Path Charging, and Single Path Charging. In addition, Separate Input configurations are provided where the Charger and USB supply are on separate inputs. In this case charging from only the wall charger unit is supported. In all cases except for Single Path Charging, the battery interface allows for so called dead battery operation.

The mode of operation for the charger interface is selected via the CHRGMOD1 and CHRGMOD0 pins as given in Table 8-1.

Table 8-1. Charger Mode Selection

CHRGMOD1	CHRGMOD0	Charger Mode	OVCTRL[1:0]
Hi Z	GND	Dual Path	00
Hi Z	Hi Z	Single Path	
Hi Z	VATLAS	Serial Path	
VATLAS	GND	Separate Input Dual Path	01
VATLAS	Hi Z	Separate Input Single Path	
VATLAS	VATLAS	Separate Input Serial Path	
GND	GND	Reserved	—
GND	Hi Z	Reserved	—
GND	VATLAS	Reserved	—

NOTE

CHRGMOD*x* pins left Hi Z must be left completely unconnected (preferred), or at least have minimal traces with a stray capacitance not to exceed 2 pF. Other traces must not be routed close to any CHRGMOD*x* minimal trace or pin so as to prevent voltage or current coupling onto the Hi Z CHRGMOD*x* pin.

The following sections each contain a high-level overview of the functionality of each configuration. The overviews include block diagrams to illustrate the routing. For details on the discrete components used, see the detailed description of each of the building blocks in this chapter. In Figure 8-1 through Figure 8-4, M1 through M4 are PMOS FETS. Refer to the Freescale document: *External Component Recommendations*

for the MC13783 *Reference Design Applications Note* (document order number: AN3295) for additional information.

8.1.1 Dual Path Charging

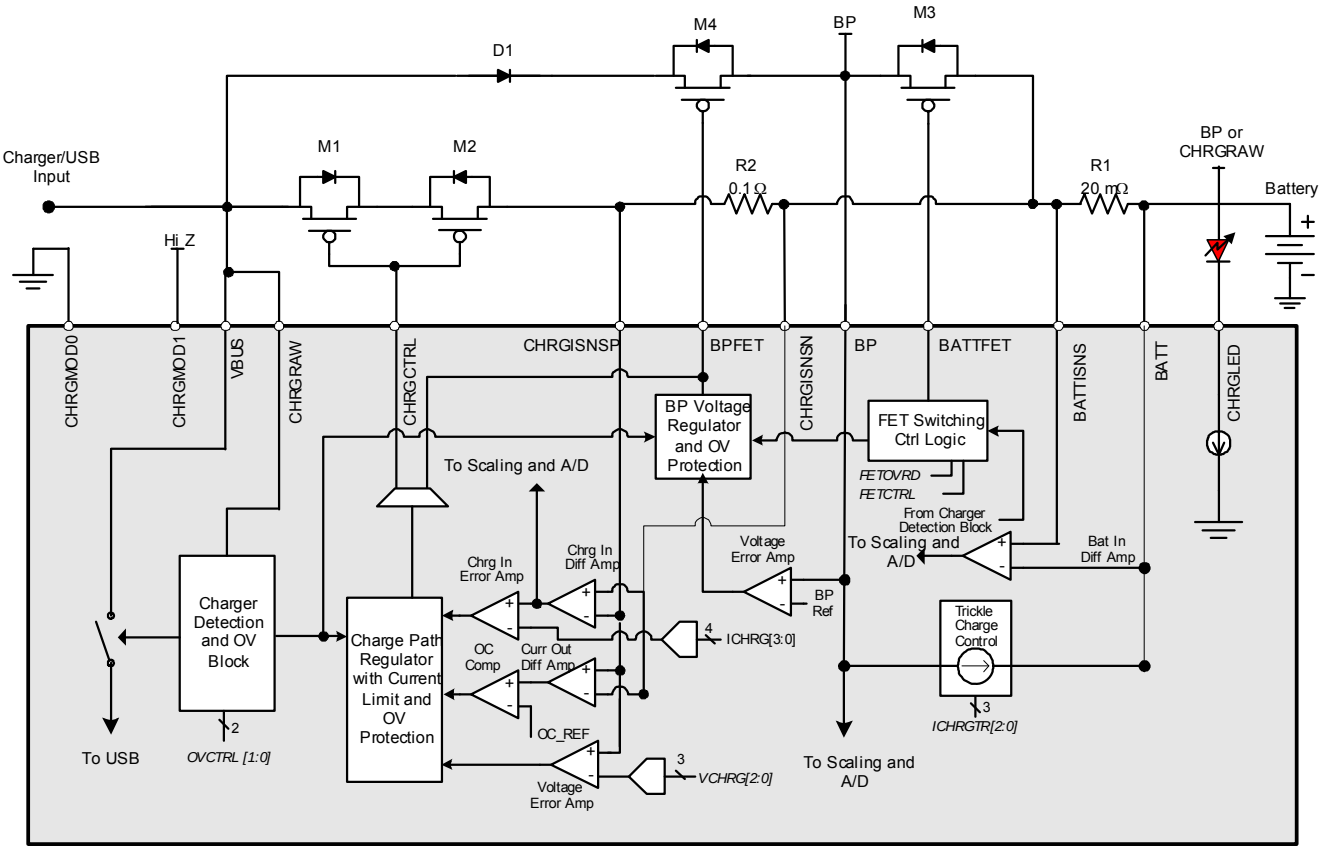


Figure 8-1. Dual Path Interface Block Diagram

In dual path configuration, the current path used for charging the battery is different than supply path from charger to radio B+. Transistors M1 and M2 control the charge path to the battery pack and operates as a voltage regulator with programmable current limit. M4 operates as a voltage regulator and controls the supply from the Charger/USB input to radio B+ supply. In addition, transistor M3 operates as a switch that connects Battery to B+.

In dual path configuration, depending on the amount of reverse leakage of the Schottky diode D1, the VBUS may be pulled high when no charger or USB bus is present at the input. To avoid false detection of charger present, a pull down is automatically enabled at the CHRGRAW input when the MC13783 is inactive (RESETB is low), in dual path configuration and with CHRGRAW below 4.1 V. The pull down can also be enabled when the MC13783 is active by setting the CHRGRAWPDEN bit. When the VBUS regulator is enabled, the pull down is automatically disconnected.

8.1.2 Serial Path Configuration

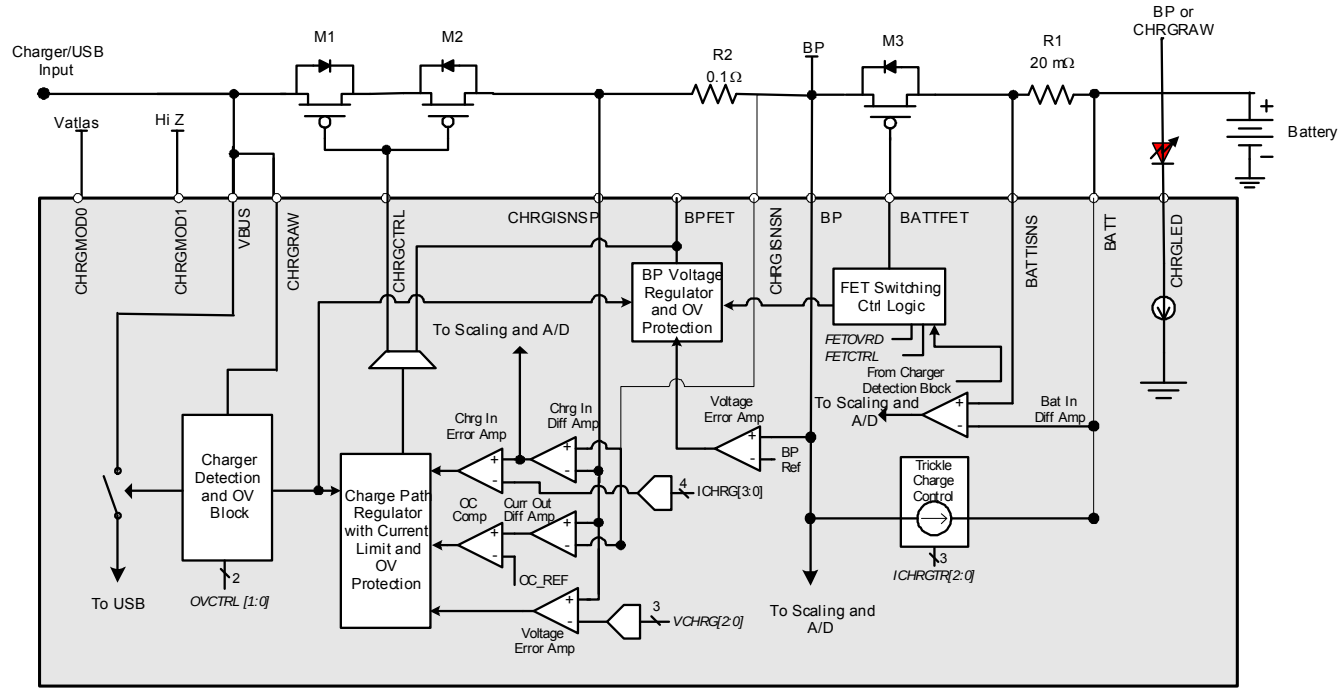


Figure 8-2. Serial Path Interface Block Diagram

In serial path configuration, the current path used for charging the battery is the same as the supply path from charger to radio B+. Transistors M1 and M2 control the charge current and provide a voltage clamping function in case of no battery or in case of a dead battery to allow the application to operate. In both cases transistor M3 is non-conducting and the battery is charged with a trickle charge current internal to the MC13783. The transistor M3 is conducting in case the battery has to be connected to the application like for normal operation or for standalone trickle charging. Transistors M1 and M2 are non-conducting in case the charger voltage is too high. A current can be supplied from the battery to an accessory with all transistors M1, M2 and M3 conducting by enabling the reverse supply mode.

8.1.3 Single Path Configuration

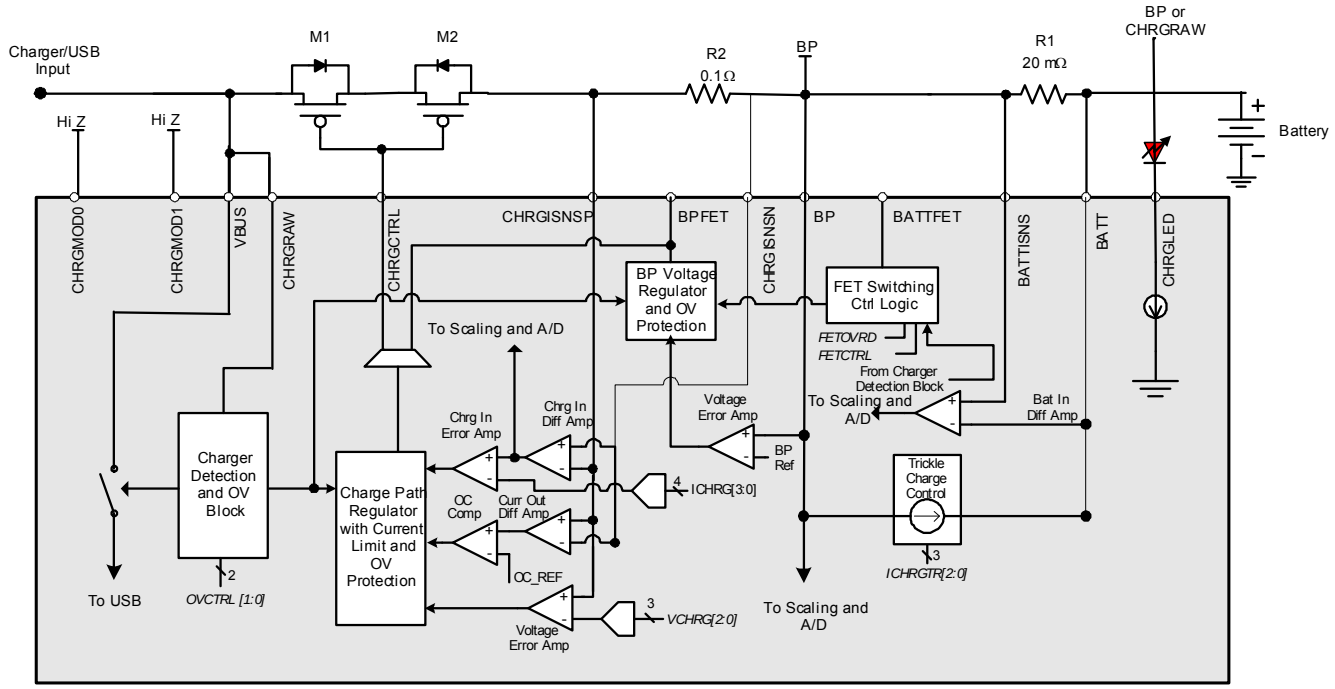


Figure 8-3. Single Path Interface Block Diagram

In the single path configuration, the charge current path is the same as serial path configuration except that transistor M3 is not mounted and therefore, dead battery operation is not supported.

8.1.4 Separate Input Dual Path Configuration

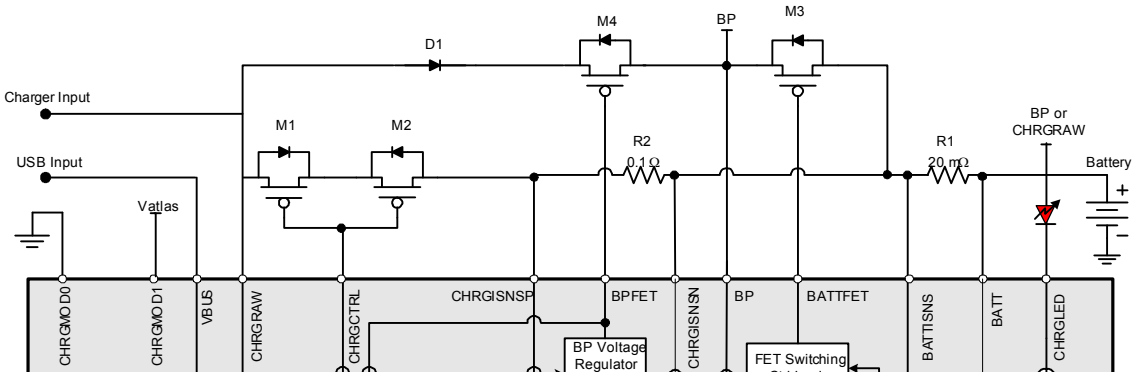


Figure 8-4. Separate Input Dual Path Interface Block Diagram

In the separate input charger configurations, the VBUS and CHRGRAW pins are not connected together in the application. As a result, the USB host cannot be used to charge the battery. The operation of the dual path itself is identical to that of the common input dual path configuration.

8.1.5 Separate Input Serial Path Configuration

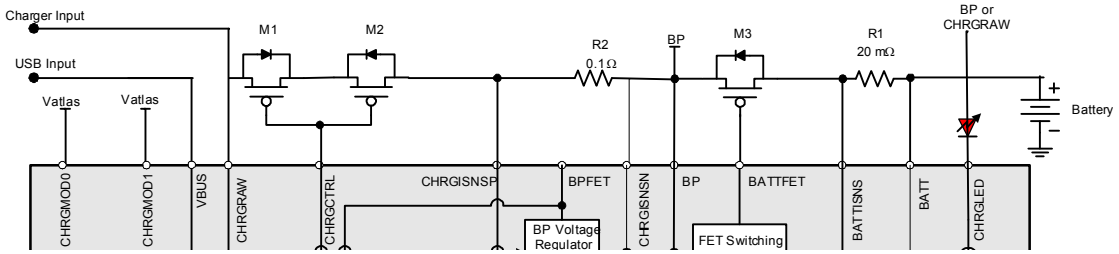


Figure 8-5. Separate Input Serial Path Interface Block Diagram

In the separate input charger configurations, the VBUS and CHRGRAW pins are not connected together in the application. As a result, the USB host cannot be used to charge the battery. The operation of the serial path itself is identical to that of the common input serial path configuration.

8.1.6 Separate Input Single Path Configuration

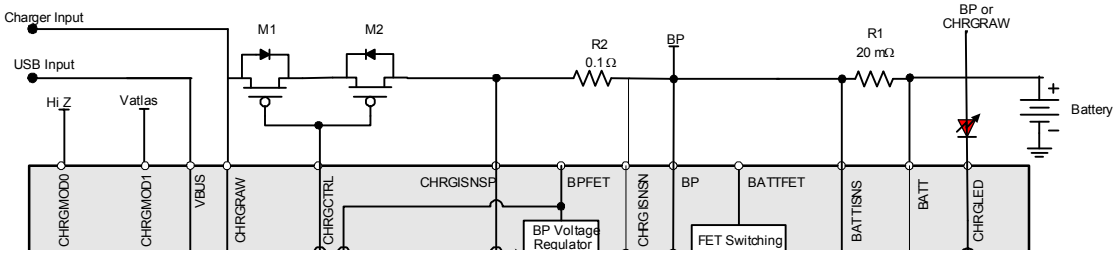


Figure 8-6. Separate Input Single Path Interface Block Diagram

In the separate input charger configurations, the VBUS and CHRGRAW pins are not connected together in the application. As a result, the USB host cannot be used to charge the battery. The operation of the single path itself is identical to that of the common input single path configuration.

8.2 Building Blocks and Functions

The battery interface consists of several building blocks and functions as depicted in the diagrams Figure 8-1 through Figure 8-6. The building blocks and functions are described in the following sections, except for the charger detection, standalone trickle charging and external charger interface which are described in Section 8.3.3, “Charger Detection,” and Section 8.3.4, “Standalone Trickle Charging.”

8.2.1 Unregulated Charging

The unregulated charge path is established by M1 and M2 fully turned on by their gates pulled low. The amount of charge current is limited by what the charger can deliver. The current can be read out via the ADC by monitoring the voltage drop over the sense resistor. The unregulated charge path is enabled and disabled via the UCHEN bit. The gate drive of M1 and M2 is intentionally slow to avoid high current spikes when turning on the charge path. It is assumed that in an unregulated charge mode the charger voltage collapses to the battery voltage and that the dissipation in the charge path remains low. In case of battery removal, the BP is limited by the charge path regulator in the following section.

8.2.2 Charge Path Regulator

The M1 and M2 are permanently used as a combined pass device for a super regulator, that will have programmable output voltage set by the VCHRG[2:0] bits and programmable current limit set by the ICHRG[3:0] bits. The voltage loop consists of M1, M2 and the amplifier with voltage feedback taken from the CHRGISNS pin. The value of the sense resistor is of no influence. Since this voltage clamp will operate in the linear region, the dissipation can be significant and care must be taken to ensure that external pass FETs are not over dissipating when charging. The power dissipation can be estimated by software by reading the charger input voltage, the charge current, and the voltage drop over the M1, M2 and resistor combination. The clamp voltage is programmable to adapt it to the different battery chemistries and use cases. The lowest set point VCHRG[2:0]=110 can be used as a safety setting in case of extreme charging conditions. The highest set point VCHRG[2:0]=111 can be used to create a charging scheme for Nickel based batteries.

Table 8-2. Charge Path Regulator Voltage Characteristics

Parameter	Value	Charge Regulator Output Voltage (V)
VCHRG[2:0]	000	4.050
	001	4.375
	010	4.150
	011	4.200
	100	4.250
	101	4.300
	110	3.800
	111	4.500

The current loop is composed of the M1 and M2 as control elements, the external sense resistor, a 4-bit current limit and the amplifier. The control loop will limit the voltage drop over the sense resistor equals the output value of the 4-bit current limit as set via the ICHRG[3:0] control bits. The resulting maximum current is therefore a function of the value of the sense resistor. The regulator can be shut off by setting the ICHRG[3:0] control bits to 0. By periodically setting and clearing these bits, pulsed charging at a defined current level can be obtained. If the UCHEN bit is set, the setting of the ICHRG[3:0] bits is overruled.

Table 8-3. Charge Path Regulator Current Limit Characteristics

Parameter	Value	Charge Current (in mA)[1]		
		Min[2]	Nom[3]	Max[2]
ICHRG[3:0]	0000	0	0	0
	0001	55	70	85
	0010	161	177	195
	0011	242	266	293
	0100	322	355	390
	0101	403	443	488
	0110	484	532	585
	0111	564	621	683
	1000	645	709	780
	1001	725	798	878
	1010	806	886	975
	1011	886	975	1073
	1100	967	1064	1170
	1101	1048	1152	1268
	1110	1450	1596	1755
	1111	Fully On—Disallow battery fet to be turned on in hardware		

1 The charge current is the current through the sense resistor.

2 The spread is 10% with respect to nominal except for code 0001.

3 The nominal value is a multiple of 88.65 mA except for code 0001.

As indicated in Table 8-3, the ICHRG[3:0] bits set the current limit for the main charge path. A specific setting is ICHRG[3:0] = 1111 which disables the current limit. As a safety feature however, the output of the BATTFET driver is maintained high which will make that in serial path, the BP can be supplied in the fully on mode without any risk of exceeding the maximum allowable battery charge current. This safety feature can be disabled by setting the UCHEN bit. Now the BATTFET signal can be forced low by setting FETOVRD and FETCTRL to 1.

Table 8-4. Charge Path Regulator Characteristics

Parameter	Condition	Min	Typ	Max	Units
Configuration Specifications[1]					
Input/Output voltage range	CHRGRAW	3	—	20	Volts
Input Capacitance	CHRGRAW=5V	1.3	2.2	—	uF
Input Capacitance ESR		0.47	—	—	Ω
Load Capacitor, CL	Regulating the BP node	5	10	30	uF
Load Capacitor, CL	Regulating the BATT node	5	10	30	uF
Load Capacitor ESR	At capacitor resonance	4	—	30	mΩ
Performance Specifications					
Output Voltage	BP/BATT, 100 uA < IL < 100 mA, (Vout +500 mV) < Vin	Nom - 1.25%	Nom	Nom + 1%	—
Output Voltage	BP/ BATT, 100 mA < IL < 1.5 A, (Vout +500 mV) < Vin	Nom - 5%	Nom	Nom + 1%	—
PSRR	Vin = Vout +1 V IL = 75% of Imax	20	—	—	dB
Start-Up Overshoot	IL = 0	—	1	—	%
Turn-on Time	ENABLE to 90% of Vout	—		100	ms
Transient Response	IL = 10 mA to 1.5 A, Tr = 5 us	—	1	—	%

[1] M1, M2 Preferred device: Vishay Si8401 or equivalent like Fairchild FDZ293P.

8.2.3 BP Voltage Regulator

In the dual path configuration, M4 will regulate and therefore limit the voltage on BP.

Table 8-5. BP Voltage Regulator Characteristics

Parameter	Condition	Min	Typ	Max	Units
Configuration Specifications[1, 2]					
Load Cap, CL		5	10	—	uF
Load Capacitor ESR	At capacitor resonance	10	—	30	mΩ
USB Cable Length		—	—	3	m
Performance Specifications					
Output Voltage	100 uA < IL < 1 A, (Vout +500 mV) < Vin[3]	4.1	4.3	4.5	V

Table 8-5. BP Voltage Regulator Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
PSRR	Vin = Vout +1 V IL = 75% of Imax	20	—	—	dB
Start-Up Overshoot	IL = 0	—	1		%
Turn-on Time	ENABLE to 90% of Vout	—	—	1	ms
Transient Response	IL = 0 mA to Imax, Tr = 10 us	—	1	—	%
Pull Down	At CHRGRAW pin, CHRGRAWPDEN = 1	1.75	3.50	5.25	kΩ

1 M4 Preferred device: Vishay Si8401 or equivalent like Fairchild FDZ293P.

2 D1 Preferred device: On Semi MBRM120 or equivalent.

3 In absence of D1.

Chargers with too high output voltages will be rejected by the system by shutting off the charge path regulator by opening M1 and M2 and for dual path, shutting off the BP regulator by opening M4. In order to prevent inadvertent shut off of the charge path regulator or the BP regulator, this comparator is rising edge debounced. If an over voltage condition is detected, an interrupt CHOVI is generated.

By taking the necessary precautions, the charger over voltage protection is programmable via OVCTRL[1:0]. For the non separate input modes the default is 00 and any of the other settings can be selected. In case of separate input modes the default is 01 and can be reprogrammed through SPI to 10 and 11. It must not be programmed to 00, this will disable the over voltage detection circuit which may lead to severe damage. In any case, when reprogramming for higher voltages, the dissipation in the charger path might become excessive so must be carefully monitored or limited by design.

In common input configurations, so VBUS and CHRGRAW connected together, the lowest threshold is also used to protect the USB module. When exceeding OVLO, internally the USB circuitry is disconnected. A debounce is not applied in this case. In separate input configurations, this protection mechanism is not operational.

Table 8-6. Charger Over Voltage Protection Setting

OVCTRL1	OVCTRL0	Over Voltage Setting[1]	OV Comparator
0	0	5.83 V[2]	OVLO
0	1	6.90 V	OVHI
1	0	9.80 V	—
1	1	19.6 V	—

1 Rising edge.

2 Must not be used in separate input configurations, this will disable the over voltage setting.

Table 8-7. Charger Over Voltage Protection Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
Input/output voltage range	CHRGRAW, CHRGCTRL, BPFET	3.0	—	20	V
Input voltage slew rate [dv/dt]Rise	0 V< CHRGRAW < 20 V, at power up	0.00125	—	360	V/µs

Table 8-7. Charger Over Voltage Protection Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Input voltage slew rate [dv/dt]Rise	3 V< CHRGRAW < 20 V, While in normal operation	0.00125	—	12	V/µs
OVLO comparator voltage threshold (VTh)	High to Low, Low to High	5.6	—	5.9	V
OVLO comparator voltage hysteresis (VHyst)	—	50	—	200	mV
OVHI comparator voltage threshold (VTh)	Low to High	Vnom-2%	Vnom	Vnom + 2%	V
OVHI comparator voltage hysteresis (VHyst)	—	25	—	225	mV
OV comparator debounce time	Rising edge	7.8	—	11.7	ms
Turn-off delay (TOFF)	CL = 6 nF, VBUS > VTh to CHRGCTRL= CHRGRAW and BPFET=VBUS	—	—	1	us

When plugging in a charger which is above the over voltage threshold, with a battery above BATTON, the MC13783 will power up and both a charger detection CHGDETI and an CHOVI are generated. Based on ADC reading, software can decide to try to use the higher voltage charger in which case it has to raise the over voltage threshold. The charger output characteristics can be tested via short charge current pulses for instance without causing dissipation issues before using it at full rate.

8.2.4 Reverse Supply Mode

The battery voltage can be applied to an external accessory via the charge path. This can be done by setting the RVRSMODE bit high. The path is only established if the normal charge path is disabled. The turn on of M1 and M2 is intentionally slow. The current through the accessory supply path is monitored via the sense resistor. It can be read out via the ADC. The accessory supply path is disabled and an interrupt CHSHORTI is generated when the slow threshold or the fast threshold is crossed. The reverse path is disabled when a current reversal occurs, so from accessory to phone, and an interrupt CHREVI is generated.

Table 8-8. Accessory Supply Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
Reverse path pull down strength	CHRGCTRL sink current	0.5	—	1.5	uA
Short circuit current threshold CSHORT1, slow	—	725	800	1010	mA
Short circuit current threshold CSHORT2, fast	—	1.7	2	2.3	A
Current reversal threshold CREV	—	1	20	30	mA
CSHORT1 debounce time	—	1	—	5	mS
CSHORT2 debounce time	—	100	—	200	uS
CREV debounce time	—	1	—	5	mS

8.2.5 Internal Trickle Charge Current Source

An internal current source between BP and BATT provides small currents to the battery in case of trickle charging a dead battery. As can be seen under the description of the trickle charging, this source is not used without software intervention. Also, this source cannot be used in single path configurations because BATT and BP are shorted on the board in that case. By setting the ICHRGTR[2:0] bits to a non-zero value, the internal current source is activated. The ICHRGTR[2:0] bits set the current for the trickle charger, as shown in Table 8-9.

Table 8-9. Internal Trickle Charge Current Control Settings

Parameter	Value	Trickle Charge Current (in mA)[1]		
		Min	Nom	Max
ICHRGTR[2:0]	000	0	0	0
	001	6	9	12
	010	14	20	26
	011	25	36	47
	100	29	42	55
	101	35	50	65
	110	41	59	77
	111	50	68	86

1 Required minimum headroom BP-BATT = 1.0 V.

8.2.6 Battery Comparators

Several comparators are active at the BATT pin that are used for charging.

Table 8-10. Battery Detectors Main Characteristics

Parameter	Description	Min	Typ	Max	Units
BATTL Threshold	Low to High	-3%	2.7	+3%	Volts
BATTON Threshold	Low to High	-3%	3.43	+3%	Volts
BATTH Threshold	Low to High	-3%	3.7	+3%	Volts
Hysteresis	—	50	—	200	mV

8.3 Charger Operation

8.3.1 CEA-936-A

The CEA-936-A carkit specification allows a USB connection to be used not only as an USB interface but also as a generic supply plus analog audio interface. The purpose is to standardize the carkit interface over a USB connection. The USB VBUS line in this case is used to provide a supply within the USB voltage limits and with at least 500 mA of current drive capability. However, this also opens the possibility to create a range of USB compatible wall chargers, referred to as CEA-936-A charger in the remainder of this

chapter. The CEA-936-A standard also allows providing a supply from the phone to the accessory over the VBUS line, just like in the USB on the go case.

Upon plugging a legacy USB host, the VBUS will be detected, the D+ will be pulled up by the USB transceiver in the MC13783 (in case of full speed mode), while the D- line will be pulled low by the host. On the other hand, upon plugging a CEA-936-A charger, the D+ and D- lines will both be pulled high by the CEA-936-A charger.

The USB ID line can give additional information on the type of device connected. In case of a legacy device the line is not existing, so high impedance. For a CEA-936-A charger the line can be left open, leading to setting up a negotiation protocol or can be terminated with a given impedance to identify the CEA-936-A charger drive capability. The latter is not specified within the CEA-936-A carkit specification but is a freedom to the phone manufacturer.

When trickle charging from the USB cable, it is important not to exceed the 100 mA in case of a legacy USB bus.

For further USB, USB on the go and CEA-936-A detection and negotiation protocols, see Chapter 10, “Connectivity”.

8.3.2 Charger Control Logic

Table 8-11. Dual Path Logic

CHRGRAW	UID	RESETB	UDP	UDM	FET OVRD	FET CTRL	BATT	BP Regulator	BATTFET	Charge Path Regulator	Internal Trickle Charger	Charger Turn On
H	<3V	L	L	L	X	X	<BATT ON	OFF	H	TRICKLEL	OFF	L
			L	H								
			H	L								
			L	L	X	X	>BATT ON	OFF	L	TRICKLEL	OFF	H
			L	H								
			H	L								
			H	H	X	X	X	ON	H	OFF	OFF	H
		H	L	L	0	X	X	OFF	L	ICHRG[3:0]	NA	H
			L	H								
			H	L								
			H	H	0	X	X	ON	H	ICHRG[3:0]	ICHRGTR[2:0]	H
			X	X	1	0	X	ON	H	ICHRG[3:0]	ICHRGTR[2:0]	H
			X	X	1	1	X	OFF	L	ICHRG[3:0]	NA	H
	>3V	X	X	X	X	X	X	ON	H	ICHRG[3:0]	ICHRGTR[2:0]	H
L	X	X	X	X	X	X	X	OFF	L	OFF	OFF	L

Note: For proper operation, when BP regulator is ON and BATT<BATTL, software must use the internal trickle charger to precharge the battery and keep the charge path regulator OFF.

Table 8-12. Serial Path Logic

CHRGRAW	UID	RESETB	UDP	UDM	FETOVRD	FETCTRL	BATT	BATTFET	Charge Path Regulator	Internal Trickle Charger	Charger Turn On
H	<3V	L	L	L	X	X	<BATT ON	L	TRICKLEL	OFF	L
			L	H							
			H	L							
			L	L	X	X	>BATT ON	L	TRICKLEL	OFF	H
			L	H							
			H	L							
			H	H	X	X	X	H	Full Rate	OFF	H
		H	L	L	0	X	X	L	ICHRG[3:0]	NA	H
			L	H							
			H	L							
			H	H	0	X	X	* H	Full Rate	OFF	H
								* L	ICHRG[3:0]	ICHRGTR[2:0]	H
			X	X	1	0	X	H	ICHRG[3:0]	ICHRGTR[2:0]	H
			X	X	1	1	X	L	ICHRG[3:0]	NA	H
	>3V	X	X	X	X	X	X	H	Full Rate	ICHRGTR[2:0]	H
L	X	X	X	X	X	X	X	L	OFF	OFF	L
(*) 'H / Full Rate / OFF / H' if already Full Rate before entering this mode, 'L / ICHRG[3:0] / ICHRGTR[2:0] / H' in the other cases.											

Table 8-13. Single Path Logic

CHRGRAW	UID	RESETB	UDP	UDM	FET OVRD	FET CTRL	BATT	Charge Path Regulator	Charger Turn On
H	<3V	L	L	L	X	X	<BATTON	TRICKLEL	L
			L	H					
			H	L					
			L	L	X	X	>BATTON	TRICKLEL	H
			L	H					
			H	L					
			H	H	X	X	X	**OFF	L
		H	L	L	0	X	X	ICHRG[3:0]	H
			L	H					
			H	L					
			H	H	0	X	X	ICHRG[3:0]	H
			X	X	1	0	X	ICHRG[3:0]	H
			X	X	1	1	X	ICHRG[3:0]	H
	>3V	X	X	X	X	X	<BATTON	** TRICKLEL / TRICKLEM	L
		X	X	X	X	X	>BATTON	** TRICKLEM / TRICKLEH	H
L	X	X	X	X	X	X	X	OFF	L
(**) No TRICKLE charging is available for the RESETb = LOW case and SE1 = HIGH.									

Table 8-14. Separate Input Dual Path Logic

CHRGRAW	RESETB	FET OVRD	FET CTRL	BP Regulator	BATTFET	Charge Path Regulator	Internal Trickle Charger	Charger Turn On
H	L	X	X	ON	H	OFF	OFF	H
H	H	0	X	ON	H	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	0	ON	H	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	1	OFF	L	ICHRG[3:0]	NA	H
L	X	X	X	OFF	L	OFF	OFF	L
Note: For proper operation, when BP regulator is ON and BATT<BATTL, software must use the internal trickle charger to precharge the battery and keep the charge path regulator OFF.								

Table 8-15. Separate Input Serial Path Logic

CHRGRAW	RESETB	FET OVRD	FET CTRL	BATTFET	Charge Path Regulator	Internal Trickle Charger	Charger Turn On
H	L	X	X	H	Full Rate	OFF	H
H	H	0	X	* H	Full Rate	OFF	H
—	—	—	—	* L	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	0	H	ICHRG[3:0]	ICHRGTR[2:0]	H
H	H	1	1	L	ICHRG[3:0]	NA	H
L	X	X	X	L	OFF	OFF	L
(*) ‘H / Full Rate / OFF / H’ if already Full Rate before entering this mode, ‘L / ICHRG[3:0] / ICHRGTR[2:0] / H’ in the other cases							

Table 8-16. Separate Input Single Path Logic

CHRGRAW	RESETB	FETOVRD	FETCTRL	BATT	Charge Path Regulator	Charger Turn On
H	L	X	X	X	**OFF	L
H	H	0	X	X	ICHRG[3:0]	H
H	H	1	0	X	ICHRG[3:0]	H
H	H	1	1	X	ICHRG[3:0]	H
L	X	X	X	X	OFF	L
(**) No TRICKLE charging is available for the RESETb = LOW case and SE1 = HIGH.						

8.3.3 Charger Detection

The application of a charger or USB host will cause the CHGDETI and USBI interrupts to go high. In addition, if a charger is attached, the SE1I will also go high. These interrupts can be used to detect the application of a charger in the system by looking at the CHRGDETS, USB4V4S, and SE1S bits.

In addition, when the Charge Path Regulator is enabled, the charge current is sensed across the R2 resistor to generate the CHGCURRI and CHGCURRS bits. Note that if the charge current falls below the

CHGCURR threshold, the CHGCURRS bit goes low. The CHGCURRS bit is set to 1 whenever the Charge Path regulator is disabled.

If the Charger is removed while the Charge Path regulator is enabled, the software removal detection of the charger can be determined by a combination of CHRGCURRS, CHGDETS, and USB4V4S.

When in separate input charging configuration, the hardware detection of removal of a charger is based on CHRGDETSEP and CHGCURR thresholds. When in common input charging configuration, the hardware detection of removal of a charger is based on CHRGDET and CHGCURR thresholds.

NOTE

The hardware detection of the charger removal with clear the ICHRG[3:0] bits which cause the Charger path Regulator to shut off.

Table 8-17. CHRGRAW Detector

Parameter	Description	Min	Typ	Max	Units
CHGDET Threshold	Low to High	—	—	3.9	Volts
	High to Low	3.5	—	—	Volts
CHGDETSEP Threshold	Low to High	—	—	4.65	Volts
	High to Low	4.4	—	—	Volts
Hysteresis	—	50	—	—	mV
CHGCURR Threshold	—	1	20	30	mA

The switching between CHRGRAW and BATT supplies in the dual path configuration system to provide BP is performed by controlling of the M3 and M4 FETs. The hardware control of the system is designed to protect for fault conditions such as shorting battery to the charger and preventing the radio to shut off. An overlap between the switching is implemented to prevent a under voltage condition while switching. If necessary, the switching can be overridden via software by setting FETOVRD and FETCTRL bits in the charger register. However, the hardware control will take priority over the SPI bits settings based on the conditions causing the switching of the supplies.

When using the CEA-936-A compatible modes of charger operation, the distinction between charger and USB is done based on the SE1 detection, meaning UDP and UDM both high. In some cases this SE1 condition cannot be generated by the charger itself and the SE1 detection will have to be forced by other means. This is achieved by providing a logic input according to Figure 8-7.

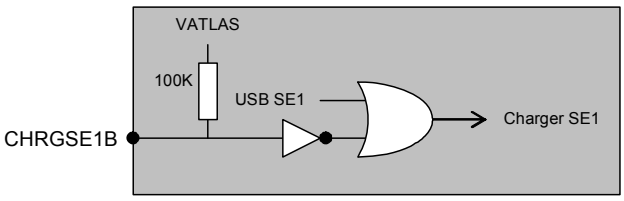


Figure 8-7. Charger SE1 Detection

When either the SE1 signal from the USB SE1 detector is high or the input pin CHRGSE1B is low, then the SE1 signal to the charger block in the MC13783 goes high. Note that this is valid for the CEA-936-A

compatible modes only, not for the other charger modes. The built in pull up will make that if CHRGSE1B is left open it will be pulled high and no SE1 is detected.

8.3.4 Standalone Trickle Charging

The MC13783 has a standalone trickle charge mode of operation in order to ensure that a completely discharged battery can be charged without the Microprocessor's control. This is especially important in single path configurations and when charging from a USB host. USB host implies that SE1 signal is not high. That is UDP and UDM are not tied together pulled high, or that the CHRGSE1B pin is NOT pulled low. The Standalone Trickle Charging feature is NOT available for the case where SE1 signal is HIGH and SINGLE path operation is selected.

Upon plugging a valid supply to the CHRGRAW input and SE1 signal is low as described above, the trickle cycle is started. The trickle charge current level is set to the TRICKLEL. When the battery voltage rises above the BATTON threshold, which is sufficient voltage for phone operation, a power up sequence is automatically initiated. During hardware trickle charging, the MC13783 will not power up based on a BPON turn on event before the BATTON threshold is crossed.

Even after the phone has powered up, the Standalone trickle charge will remain on until software does an initial write to the ICHRG[3:0] to enable charging. When performing an ICHRG[3:0] read before writing a value to it, all zero's are returned, so not the internal trickle charge value. If the battery voltage was already greater than BATTON when the valid supply to the CHRGRAW input is attached, the phone will power up immediately without starting a trickle charge cycle.

The trickle charge is terminated upon input supply or over voltage, trickle charging time out or by software control. The time out occurs upon the expiration of the trickle timer. The charge path regulator will ensure the battery voltage during trickle charging will not exceed the value as set by VCHRG[2:0].

If factory mode (UID > 3V) is detected in the single path charging configuration, and when the battery voltage is above BATTH comparator threshold, the charge current is set to the TRICKLEH. The trickle charge timer will be disabled in factory mode.

When plugging a USB host without a battery placed in the phone, the trickle charge cycle will make BATT to rise, creating a power up. Because the USB host will not provide enough current to supply the application, the charge path is controlled at TRICKLEL, the phone will immediately shut down. A built in mechanism will prevent the phone from powering up again. As a result, when applying a battery to the phone at a later stage, the USB trickle charge is not automatically started and one has to remove and plug back in the USB cable.

Since normal LED control via the SPI bus is not possible in the standalone trickle mode, a current sink will be provided at the CHRGLED pin which is active as long as the standalone trickle charge is active. This means that the trickle LED will remain on in case the phone is powered on until the charger is programmed by SPI. The LED can be connected to either BP or CHRGRAW. By having the LED current sink available at a pin creates the flexibility to connect it to any of the signaling LEDs. The trickle LED is activated at the moment the trickle timer is started. Once the phone has powered on, the trickle LED can be disabled by clearing the CHRGLEDEN SPI bit. The trickle LED is also disabled when an over voltage condition occurs unless the CHRGLEDEN bit was set high by software.

Table 8-18. Trickle Charge Main Characteristics

Trickle current TRICKLEL	ICHRG[3:0]=0001[1]
Trickle current TRICKLEM (available for UID>3V)	ICHRG[3:0]=0011
Trickle current TRICKLEH	ICHRG[3:0]=0110
Trickle timer at TRICKLEL	180 min
Trickle timer at TRICKLEM	90 min
Current sink at CHRGLED in trickle mode	8 mA

[1] For battery voltages under ~2.4 V, the current is slightly lower during trickle charging.

8.4 Coincell

The coin cell charger circuit will function as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coincell charger is enabled via the COINCHEN bit. The output voltage is selectable. The coincell charger voltage is programmable in the ON state where the charge current is fixed at ICOINHI. In the User Off modes, the coincell charger will continue to charge to the predefined voltage setting but at a lower maximum current ICOINLO if COINCHEN = 1. In the Off mode, the coincell is internally connected to VATLAS via a weak pull up when its voltage drops below VATLAS and if the COINCHEN bit was not reset to a 0 by software before shutting down the phone. A large capacitor, electrolytic or supercap, can also be used instead of a lithium based coincell. To avoid discharge by leakage currents from external components or by the MC13783, the COINCHEN bit must always remain set in that case. A small capacitor must be placed from LICELL to ground under all circumstances.

Table 8-19. Coincell Charger Main Characteristics

Coincell Charge Voltage	VCOIN[2:0]	V
	000	2.50
	001	2.70
	010	2.80
	011	2.90
	100	3.00
	101	3.10
	110	3.20
	111	3.30
Voltage Accuracy	100 mV	
Coincell Charge Current in ON mode ICOINHI	60 uA	
Coincell Charge Current in User Off modes ICOINLO	10 uA typ, 5 uA min at 2.5 V	
Current Accuracy	30%	
LICELL Bypass Capacitor	100 nF	
LICELL Bypass Capacitor as coincell replacement	4.7uF min	

8.5 Battery Interface Register Summary

Table 8-20. Charger Register SPI Bit

Bit #	Bit Name	Reset Signal	Reset State	Type	Description
0	VCHRG0	RESETB	0	R/W	Sets the output voltage of Charge Regulator.
1	VCHRG1	RESETB	0	R/W	—
2	VCHRG2	RESETB	0	R/W	—
3	ICHRG0	RESETB	0	R/W	Sets the current of the main charger DAC.
4	ICHRG1	RESETB	0	R/W	—
5	ICHRG2	RESETB	0	R/W	—
6	ICHRG3	RESETB	0	R/W	—
7	ICHRGTR0	RESETB	0	R/W	Sets the current of the trickle charger.
8	ICHRGTR1	RESETB	0	R/W	—
9	ICHRGTR2	RESETB	0	R/W	—
10	FETOVRD	RESETB	0	R/W	0 = BATTFET and BPFET outputs are controlled by hardware 1 = BATTFET and BPFET are controlled by the state of the FETCTRL bit
11	FETCTRL	RESETB	0	R/W	0 = BPFET is driven low, BATTFET is driven high if FETOVRD is set 1 = BPFET is driven high, BATTFET is driven low if FETOVRD is set
12	Reserved	RESETB	0	R/W	For future use
13	RVRSMODE	RESETB	0	R/W	0 = Reverse mode disabled 1 = Reverse mode enabled
14	Reserved	RESETB	0	R/W	For future use
15	OVCTRL0	RESETB	0	R/W	Over voltage threshold select bit.
16	OVCTRL1	RESETB	0	R/W	—
17	UCHEN	RESETB	0	R/W	Unregulated Charge Enable bit
18	CHRGLEDEN	RESETB	0	R/W	0 = CHRGLED disabled 1 = CHRGLED enabled
19	CHRGRAWPDEN	RESETB	0	R/W	Enables a 5 K pull down at CHRGRAW. To be used in the dual path charging configuration
20	Reserved	RESETB	0	R/W	For future use
21	Reserved	RESETB	0	R/W	For future use
22	Unused	—	0	R	Not available
23	Unused	—	0	R	Not available

Table 8-21. Charger Related Interrupts

Interrupt bit	Mask bit	Sense bit	Description
CHGDETI	CHGDETM	CHGDETS	Charger detection interrupt, dual edge, debounce 32 ms
CHGOVI	CHGOVM	CHGOVS	Charger over voltage detection interrupt, dual edge, 7.8 ms rising edge debounce

Table 8-21. Charger Related Interrupts (continued)

Interrupt bit	Mask bit	Sense bit	Description
CHGREVI	CHGREVM	CHGREVS	Charger path reverse current interrupt, rising edge, 2.9 ms debounce
CHGSHORTI	CHGSHORTM	CHGSHORTS	Charger path short circuit in reverse supply mode interrupt, rising edge, 150 us or 2.9 ms debounce depending on threshold
CCCVI	CCCVM	CCCVS	CCCV interrupt Logic high indicates that the charger has switched its mode from CC to CV or from CV to CC. CCVS = 0 for constant current charging, CCCVS = 1 for constant voltage charging. Detection at 98% of VCHRG[2..0]. Write a 1 to this location to clear the interrupt. Dual Edge, 2 s debounce
CHGCURRI	CHGCURRM	CHGCURRS	CHGCURR interrupt Logic high indicates that the charge current has dropped below its threshold. Falling edge, debounce 3.9 ms

Chapter 9
ADC Subsystem

9.1 Converter Core

The ADC core is a 10-bit successive approximation convertor. The ADC core and logic runs at an internally generated frequency of approximately 2 MHz, based on the 2 times the PLL multiplied 32.768 kHz coming from the crystal oscillator or the RC oscillator. The actual ADC clock frequency depends on the PLLX[2:0] setting and, when based on the crystal, will range from 1.835 MHz to 2.294 MHz. This internal clock is active whenever ADEN or one of the switchers or charge pump is active or if PLLEN is set to 1. Any trigger event occurring between the ADC being enabled and the 2 MHz being present is memorized and the ADC will start conversion only after the valid clock is present. Locally an ADC32 kHz clock signal is derived from the 2 MHz which therefore varies with PLLX[2:0]. This clock is used for the ADC timers.

Table 9-1. ADC Specification

Parameter	Condition	Min	Typ	Max	Units
Conversion Current	—	—	0.75	1	mA
A/D Quiescent Current	Normal operation	—	—	750	uA
OFF Supply Current	—	—	—	1	uA
Converter Reference Voltage	—	—	2.3	—	V
Valid Analog Input Range	—	0	—	2.30	V
Maximum Input Voltage	No degradation of A/D readout	—	—	VATLAS	V
Conversion Time per channel	PLLX[2:0] = 000	—	—	12.0	us
	PLLX[2:0] = 100	—	—	10.5	us
	PLLX[2:0] = 111	—	—	9.6	us
Integral Nonlinearity	Rs = 5 kΩ max	—	—	+/-3	LSB
Differential Nonlinearity	Rs = 5 kΩ max	—	—	+/-1	LSB
Zero Scale Error (Offset)	Rs = 5 kΩ max	—	—	10	LSB
Full Scale Error (Gain)	Rs = 5 kΩ max	—	—	+/-25	LSB
Drift over temperature	—	—	—	+/-1	LSB
Turn on/off time	ADEN set to 1, Switchers enabled	—	—	5	us
A/D Clock Startup Delay	ADEN set to 1, Switchers disabled	—	—	1	ms
(1) Rs represents a possible external series resistor between the voltage source and the ADIN input.					

9.2 Input Selector

The ADC has 2 groups of 8 input channels. ADSEL selects between two groups of input signals. If set to zero then group 0 is read and stored, if set to 1 then group 1 is read and stored. This is done to shorten the total read time and to reduce the required storage of converted values. Table 9-2 gives an overview of the attribution of the A to D channels where ADA[2:0] stands for ADA1[2:0] and ADA2[2:0].

Table 9-2. ADC Inputs

	Channel	Signal Read	Expected Input Range	Scaling	Scaled Version
Group 0 – ADSEL=0	0	Battery Voltage (BATT)	2.50 V–4.65 V	-2.40 V	0.10 V–2.25 V
	1	Battery Current (BATT – BATTISNS)	-50 V–+50 mV	x20	-1.00 V–+1.00 V
	2	Application Supply (BP)	2.50 V–4.65 V	-2.40 V	0.10 V–2.25 V
	3	Charger Voltage (CHRGRAW)	0 V–10 V / 0 V–20 V	/5 /10	0 V–2.00 V 0 V–2.00 V
	4	Charger Current (CHRGISNSP-CHRGISNSN)	-250 mV–+250 mV	X4	-1.00 V–1.00 V
	5	General Purpose ADIN5 / Battery Pack Thermistor	0 V–2.30 V	No	0 V–2.30 V
	6	General Purpose ADIN6 / Backup Voltage (LICELL)	0 V–2.30 V / 1.50 V–3.50 V	No / -1.20 V	0 V–2.30 V 0.30 V–2.30 V
	7	General Purpose ADIN7 / UID / Die Temperature	0 V–2.30 V / 0 V–2.55 V / TBD	No / x0.9 / No	0 V–2.30 V
Group 1 – ADSEL=1	8	General Purpose ADIN8	0 V–2.30 V	No	0 V–2.30 V
	9	General Purpose ADIN9	0 V–2.30 V	No	0 V–2.30 V
	10	General Purpose ADIN10	0 V–2.30 V	No	0 V–2.30 V
	11	General Purpose ADIN11	0 V–2.30 V	No	0 V–2.30 V
	12	General Purpose TSX1 / Touchscreen X-plate 1	0 V–2.30 V	No	0 V–2.30 V
	13	General Purpose TSX2 / Touchscreen X-plate 2	0 V–2.30 V	No	0 V–2.30 V
	14	General Purpose TSY1 / Touchscreen Y-plate 1	0 V–2.30 V	No	0 V–2.30 V
	15	General Purpose TSY2 / Touchscreen Y-plate 2	0 V–2.30 V	No	0 V–2.30 V

Some of the internal signals are first scaled to adapt the range to the input range of the ADC. The charge current and the battery current are indirectly read out by the voltage drop over the resistor in the charge path and battery path respectively. See the related sections for more details. Note that the 10-bit ADC core will convert over the entire scaled version of the input channel, so always from 0 V to 2.30 V or from -1.15 V to +1.15 V.

For some applications an external resistor divider network is used to scale down the to be measured voltage to the ADC input range. The source resistance presented by this may be greater than the maximum specified Rs, see ADC specification table. In that case, the readout value will be lower than expected due to the dynamic input impedance of the ADC convertor. This readout error presents itself as a gain error which can be compensated for by factory phasing. An alternative is to place a 100 nF bypass capacitor at the ADIN input concerned.

9.3 Control

The ADC parameters are programmed by the processors via SPI. Locally on the MC13783, the different ADC requests are arbitrated and executed. When a conversion is finished, an interrupt ADCDONEI, with corresponding mask bit ADCDONEM, is generated to the processor which started the conversion. This section describes the control in case of a single SPI request, dual SPI access and multiple requests are described in the ADC arbitration section.

9.3.1 Starting Conversions

The ADC will have the ability to start a series of conversions in two ways

1. Triggered with the Start Convert (ASC) bit.
2. Triggered with the rising edge of the ADTRIG signal.

The conversion will begin after a delay set by the ATO register. This register is 8 bits long and is clocked by the ADC32 kHz clock. The minimum ATO delay is one ADC32 kHz clock cycle.

Once conversion is initiated all 8 channels will be sequentially converted and stored in registers if the RAND bit is set to 0. If RAND is set to a 1, eight conversions on one channel will be performed and stored.

If WCOMP is set high, independent of the state of the RAND bit, eight conversions on one channel will be performed and the conversions will be digitally compared to WHIGH and WLOW. If one of the conversions is greater than WHIGH or smaller than WLOW the interrupt pin will be asserted at the end of the conversions, at the same time as the ADCDONEI interrupt. Note that WHIGH and WLOW are only 6 bits wide. The 6 MSBs of the conversion are used in the comparison. The results of the eight conversions are stored. The exact behavior of the WCOMP function is described in its dedicated section.

The delay between conversions can be made equal to the ATO delay by setting the ATOX bit to a 1. Figure 9-1 depicts this with Tconv as the conversion time and Tato+1 as the ATO delay plus a 32K clock cycle. The ADC32 kHz is automatically synchronized to the trigger event which avoids any synchronization error.

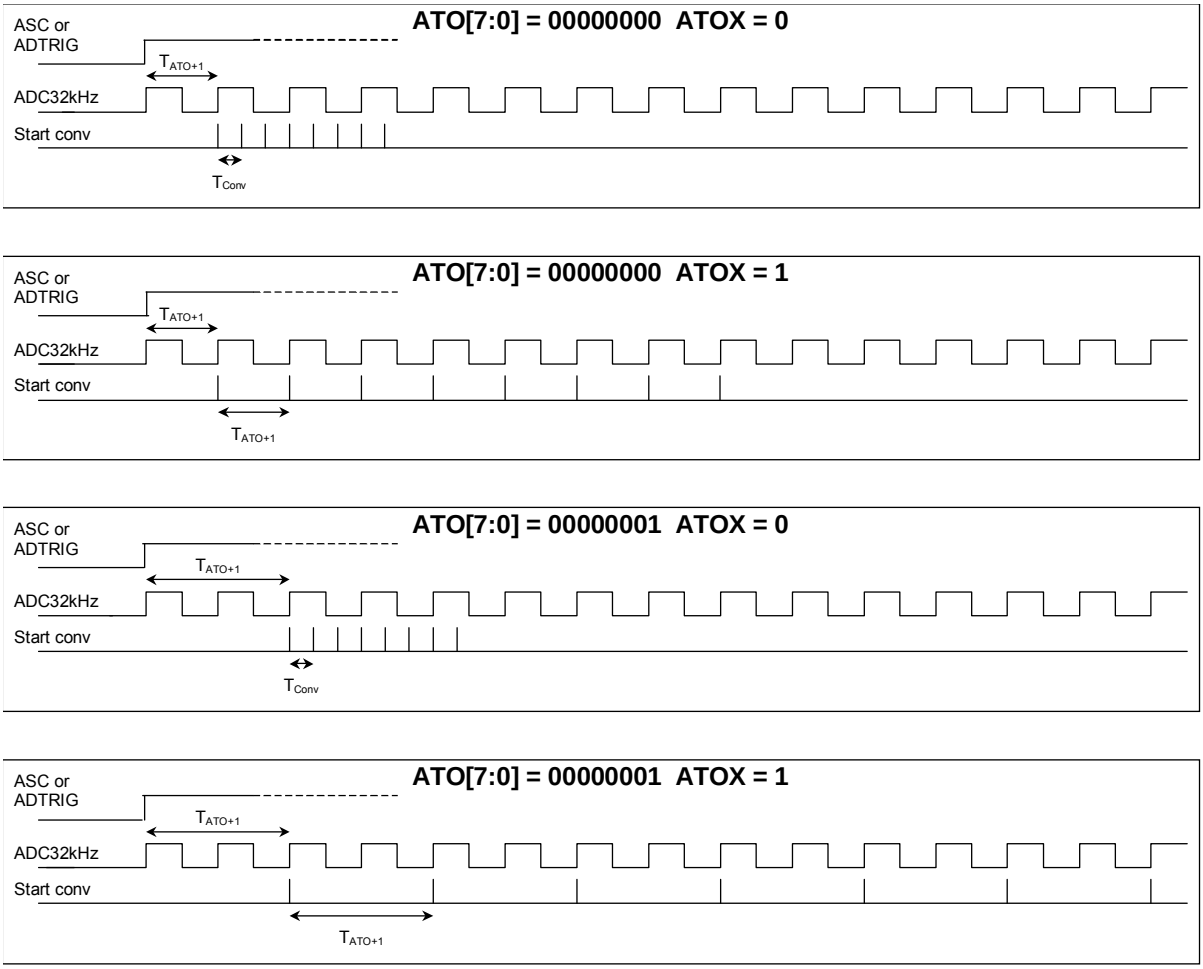


Figure 9-1. ATO and ATOX Delay Examples

To convert multiple channels starting the conversion with the ASC bit, the following steps are executed:

1. Enable A/D (ADEN=1). Set RAND to 0, and select the group of channels via ADSEL.
2. Start conversion at channel 0 by writing a 1 to the start conversion bit (ASC). The conversion will begin once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.)
4. Write the result address (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all channel results.

To convert multiple channels starting the conversion with the rising edge of ADTRIG, the following steps are executed:

1. Enable A/D (ADEN=1). Set RAND to 0, and select the group of channels via ADSEL. Note that ASC will go high with the rising edge of ADTRIG.
2. The conversion will automatically start at channel 0 once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.)

4. Write the result address (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all channel results.

To convert a single channel starting the conversion with the ASC bit, the following steps are executed:

1. Enable A/D (ADEN = 1). Set RAND to 1. Set ADA1[2:0] to the desired channel.
2. Start conversion by writing a 1 to the start conversion bit. (ASC) The conversion will begin once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.) In this mode the A/D will perform 8 conversions of the selected channel and save the results in ADA[2:0]
4. Write the conversion number 0-7 (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all 8 results.

To convert a single channel starting the conversion with the rising edge of ADTRIG, the following steps are executed:

1. Enable A/D (ADEN=1). Set RAND to 1. Set ADA1[2:0] to the desired channel. Note that ASC will go high with the rising edge of ADTRIG.
2. The conversion will automatically start once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.) In this mode the A/D will perform 8 conversions of the selected channel and save the results in ADA[2:0]
4. Write the conversion number 0-7 (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all 8 results.

ADC completely ignores either ADTRIG or ASC pulses while ADEN is low. When reading conversion results it is therefore preferable to make ADEN = 0.

To avoid that the ADTRIG input involuntarily triggers a conversion, the ADTRIGIGN bit can be set which will ignore any transition on the ADTRIG pin.

9.3.2 Reading Conversions

Once a series of (8) A/D conversions is complete, they are stored in one set of 8 internal registers and the values can be read out by software. In order to accomplish this, software must set the ADA1 and ADA2 address bits to indicate which values will be read out. Two sets of addressing bits allows any two readings to be read out which are stored in the 8 internal registers. For example, if it is desired to read the conversion values stored in addresses 2 and 6, the software will need to set ADA1[2:0] to 010 and ADA2[2:0] to 110. Any SPI read of the A/D result register will return the values of the conversions indexed by ADA1[2:0] and ADA2[2:0]. ADD1[9:0] will contain the value indexed by ADA1[2:0], where as ADD2[9:0] will contain the conversion value indexed by ADA2[2:0].

An additional feature allows for automatic incrementing of the ADA addressing bits. This involves bits ADINC1 and ADINC2. When these bits are set, the ADA1 and ADA2 addressing bits will automatically

increment during subsequent readings of the A/D result register. This allows for rapid reading of the A/D results registers with a minimum of SPI transactions. As an example the following sequence of events will convert and read out 8 channels via the SPI bus.

1. Write setting ADEN=1, RAND=0, ADSEL=0, ADA1[2:0]=000 (channel 0), ADA2[2:0]=100 (channel 4). All other bits are zeros.
2. Write setting ASC=1, ADINC1=1, ADINC2=1. All other bits are zero. The conversion will start after the ATO delay since ASC was set to 1.
3. Wait for the interrupt line to go high and read from the interrupt register to verify ADCDONEI is set.
4. Read from the result register. The channel 0 data is in bits ADD1[9:0], and the channel 4 data is in bits ADD2[9:0]. ADINC1 and ADINC2 will still be high. ASC will be zero.
5. Read from the result register. The channel 1 data is in bits ADD1[9:0], and the channel 5 data is in bits ADD2[9:0].
6. Read from the result register. The channel 2 data is in bits ADD1[9:0], and the channel 6 data is in bits ADD2[9:0].
7. Read from the result register. The channel 3 data is in bits ADD1[9:0], and the channel 7 data is in bits ADD2[9:0].

Any intermediate reading from the result register while waiting for the interrupt during step 3 will already increment the ADA addressing bits and therefore be avoided.

9.4 Pulse Generator

A SPI controllable pulse generator is available at ADOUT synchronized with the ADC conversion. This pulse can be used to enable or drive external circuits only during the ADC conversion. By setting ADOUTEN high, a pulse is generated at ADOUT upon every ADC trigger as long as this bit remains set. To generate a single pulse when triggering via ADTRIG, the ADONESHOT function may be used, see also the arbitration section of this chapter. The rising edge of the ADOUT pulse occurs a few microseconds after the start of a series of ADC conversions initiated via the ASC bit or ADTRIG. This allows the circuitry connected to ADOUT to power up and stabilize during the ATO delay. The ADOUT pulse duration is set via the ADOUTPER bit. For ADOUTPER is zero, the pulse will last for 4 conversions, when set high for 8 conversions. The absolute length of the pulse can be set via the ATO and ATOX settings. The ADOUT function can be used in single and multiple channel mode. Figure 9-2 depicts the behavior for ATO[7:0]=00000000, ATOX=1.

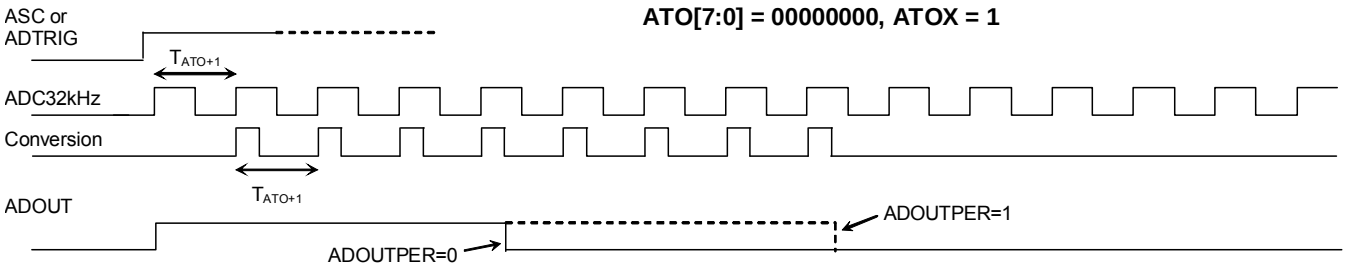


Figure 9-2. ADOUT Pulse Generator Behavior

Table 9-3. ADOUT Output Characteristics

Parameter	Condition	Min	Typ	Max	Units
ADOUT Output Low	Output sink 1 mA	0	—	0.2	V
ADOUT Output High	Output source 1 mA	VIOHI - 0.2	—	VIOHI	V
ADOUT Output Rise Time	Cload = 100 pF	—	1	2	us
ADOUT Output Fall Time	Cload = 100 pF	—	1	2	us

9.5 Dedicated Channels Reading

9.5.1 Battery Current and Voltage

Traditional battery capacity estimation is based on battery terminal voltage reading combined with estimated phone current drain based on emitted PA power. For improved battery capacity estimation, especially in non transmit mode like gaming, this method is too approximative. To improve the estimation, the current out of the battery must be quantified more accurately. For this, on the MC13783, the current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS. This function is enabled by setting the BATTICON bit to one.

The battery current can be read either in multiple channel mode or in single channel mode. In both cases, the battery terminal voltage at BAT and the voltage difference between BAT and BATTISNS are sampled simultaneously but converted one after the other. This is done to effectively perform the voltage and current reading at the same time. In multiple channel mode, the converted values are read at the assigned channel. In single channel mode, with RAND=1, ADSEL=0, ADA1[2:0]=001, the converted result is available in 4 pairs of battery voltage and current reading. Table 9-4 depicts this.

Table 9-4. Battery Current Reading Sequence

ADC Trigger	Signals Sampled	Signal Converted	Readout	Contents
0	BATT, BATT-BATTISNS	BATT	Channel 0	BATT
1	—	BATT-BATTISNS	Channel 1	BATT-BATTISNS
2	BATT, BATT-BATTISNS	BATT	Channel 2	BATT
3	—	BATT-BATTISNS	Channel 3	BATT-BATTISNS
4	BATT, BATT-BATTISNS	BATT	Channel 4	BATT
5	—	BATT-BATTISNS	Channel 5	BATT-BATTISNS
6	BATT, BATT-BATTISNS	BATT	Channel 6	BATT
7	—	BATT-BATTISNS	Channel 7	BATT-BATTISNS

If the BATICON bit is not set, the ADC will convert the voltage at the ADC channel 1 which is a non available input. When RAND=1 and BATICON=0, the specific sequence as indicated in Table 9-4 will not be executed and ADC channel 1 will be converted 8 times.

The voltage difference between BATT and BATTISNS is first amplified and then converted by the ADC. The conversion is read out in a 2's complement format, see Table 9-5. The positive reading corresponds to the current flow out of the battery, the negative reading to the current flowing into the battery. The value of the sense resistor used, determines the accuracy of the result as well as the available conversion range.

NOTE

Very high values will reduce the operating life of the phone due to the voltage drop over the resistor.

Table 9-5. Battery Current Reading Coding

Conversion Code ADDn[9:0]	Voltage at Input ADC in mV	BATT – BATTISNS in mV	Current through 20 mOhm in A	Current Flow
0 111 111 111	1150.00	57.50	2.875	From battery
0 000 000 001	2.25	0.11	0.006	From battery
0 000 000 000	0	0	0	—
1 111 111 111	-2.25	-0.11	0.006	To battery
1 000 000 000	-1150.00	-57.50	2.875	To battery

Table 9-6. Battery Current Reading Specification

Parameter	Condition	Min	Typ	Max	Units
Amplifier Gain	—	—	20	—	Times
Amplifier Offset	—	—		1	mV
Sense Resistor	—	—	20	—	mOhm
Note: Amplifier Bias Current accounted for in overall ADC current drain.					

The battery voltage is read at the BATT pin at channel 0. The battery voltage is first scaled by subtracting 2.40 V in order to fit the input range of the ADC. The same reading conversion is applicable to the BP reading on channel 2.

Table 9-7. Battery Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at Input ADC in V	Voltage at BATT in V[1]
1 111 111 111	2.300	4.700
1 111 101 000	2.250	4.650
0 000 101 100	0.100	2.500
0 000 000 000	0.000	<2.400

[1] The max. rating for BATT is 4.65 V.

9.5.2 Charge Current and Voltage

The charge current is read by monitoring the voltage drop over the charge current sense resistor. This resistor is connected between CHRGISNSP and CHRISNSN. The conversion is read out in a Two's complement format, see Table 9-8. The positive reading corresponds to the current flow from charger to battery, the negative reading to the current flowing into the charger terminal. The value of the sense resistor used, determines the accuracy of the result as well as the available conversion range. The conversion circuit is enabled by setting the CHRGICON bit to a one.

Table 9-8. Charge Current Reading Coding

Conversion Code ADDn[9:0]	Voltage at Input ADC in mV	CHRGISNSP – CHRGISNSN in mV	Current through 100 mOhm in A	Current Flow
0 111 111 111	1150.00	287.5	2.875	To battery
0 000 000 001	2.25	0.6	0.006	To battery
0 000 000 000	0	0	0	—
1 111 111 111	-2.25	-0.6	0.006	To charger
1 000 000 000	-1150.00	-287.5	2.875	To charger

Table 9-9. Charge Current Reading Specification

Parameter	Condition	Min	Typ	Max	Units
Amplifier Gain	—	—	4	—	Times
Amplifier Offset	—	—	—	1	mV
Sense Resistor	—	—	100	—	mOhm
Note: Amplifier Bias Current accounted for in overall ADC current drain.					

The charger voltage is measured at the CHRGRAW pin at channel 3. The charger voltage is first scaled in order to fit the input range of the ADC. If the CHRGRAWDIV bit is set to a 1 (default) then the scaling factor is a divide by 5, when set to a 0 a divide by 10.

Table 9-10. Charger Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at Input ADC in V	Voltage at CHRGRAW[1] in V, CHRGRAWDIV = 0	Voltage at CHRGRAW in V, CHRGRAWDIV = 1
1 111 111 111	2.300	23.000	11.500
1 101 111 001	2.000	20.000	10.000
0 000 000 000	0.000	0.000	0.000

1 The max. rating for CHRGRAW is 20 V.

9.5.3 Backup Voltage

The voltage of the coincell connected to the LICELL pin can be read out via the ADC if the LICON bit is set to a one. This voltage reading does not take any current from the coincell when not converting. Due to the switched capacitor structure of the ADC, even during a readout the current drain from the coincell is negligible. Since the voltage range of the coincell exceeds the input voltage range of the ADC, the coincell voltage is first scaled.

Table 9-11. Coincell Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at input ADC in V	Voltage at LICELL in V
1 111 111 111	2.300	3.500
0 010 000 101	0.300	1.500
0 000 000 000	0.000	<1.200

9.5.4 Battery Thermistor and Battery Detect

If a battery is equipped with a battery thermistor, its value can be read out via the ADC input ADIN5. If the RTHEN bit is set an internal pull up current source is activated. If this bit is not set, the ADIN5 is used as a general purpose ADC voltage reading input and the thermistor will have to be biassed with an external pull up.

The reading of the thermistor value is optimized for a thermistor which changes -4.27% per degree according the formula 31.115 kOhm * 10^(-T/52.777) with T in °C. Typical values for the valid charging range are therefore 38 kOhm at -5 °C, 10 kOhm at +25 °C, and 2.2 kOhm at 60 °C.

Table 9-12. Battery Thermistor Interface Target Specification

Parameter	Target
Thermistor Input range	2 V–100 kOhm
Internal current source	20 uA
Absolute Resistance Measurement Inaccuracy over Temperature	10%
BATTDET threshold	2.4V ± 4%
Bias current BATTDET function with RTHEN=1	30 uA
BATTDETB output voltage high	VIOLO

If the battery thermistor reading as described above does not suit the application needs, the thermistor can also be connected to the ADOUT pin. As a result the thermistor will only be biased during the ADC conversions. The ADIN5 input must be set as a general purpose input in that case. Alternatively the thermistor can also be biased via a GPOx output.

When a phone is on, SIM removal has to be detected to avoid fraudulent use of the phone. A mechanical way of doing so is to provide a slider in which the SIM card has to be inserted. When opening the slider a contact is made/broken which will inform the processor the SIM card slider is opened. The SIM card holder with slider however takes more board space and is more expensive then a SIM card holder without.

An easy way of doing a SIM removal detection for such a card holder is to place it under the battery pack and perform a battery thermistor check. When the thermistor terminal becomes high impedance, the battery is considered being removed.

If the BATTDETEN bit is set to a 1 (default is 0), the SIM removal function is enabled. A battery detect comparator will compare the voltage at ADIN5 with BATTDET. If this threshold is exceeded the BATTDETB pin will be made high after a debounce of 16 ms (dual edge). If the BATTDETEN bit is not set, the output BATTDETB is low.

If the RTHEN bit was set as well, the internal current source used for the thermistor reading is permanently enabled. In case the internal pull up source is not used for this purpose a general purpose output GPOx must be used to supply the thermistor via a resistive network. ADOUT cannot be used for this because ADOUT will only be high during ADC conversions while the battery detect function must operate permanently.

As an example for using a GPOx output to drive the thermistor, suppose a 10kOhm nominal thermistor which however at low temperatures can become as high as 300kOhm worst case. Then, use GPO1 to pull up the thermistor via a resistor of 47kOhm. Additional RC filtering towards the ADC input can be applied.

When not charging, the SIM removal function is not required to operate since a battery removal is already handled by the power cut function. Although the additional current drain due to the battery detect function is small, it is advised to disable the function when not charging to safe this current.

9.5.5 Die Temperature and UID

The die temperature can be read out on the ADIN7 channel if the DTHEN bit is set. The die temperature is read out as a the voltage over a forward biased diode within the thermal protection circuit. The relation between the read out code and temperature is given in Table 9-13.

Table 9-13. Die Temperature Voltage Reading

Parameter	Typical
Die Temperature Read Out Code at 25 °C	282
Temperature change per LSB	-1.14 °C

The UID voltage can be read out on the ADIN7 channel if the UIDEN bit is set. The voltage at UID is scaled by a factor of 0.9 in order to fit the UID input range to the ADC input range. Any UID voltage greater than then the input range will be clamped. This is required since the UID voltage potentially can be as high as 5.25 V during fault conditions.

Table 9-14. UID Voltage Reading Coding

Conversion Code ADDn[9:0]	Voltage at Input ADC in V	Voltage at UID in V
1 111 111 111	2.300	>2.555
0 000 000 000	0.000	0

If both the DTHEN and UIDEN bit are set, then the general purpose input ADIN7 is converted as given in Table 9-15.

Table 9-15. ADIN7 Channel Selection

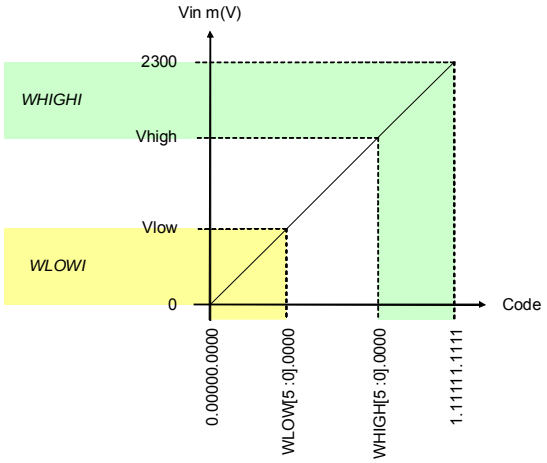
DTHEN	UIDEN	ADC Channel Converted
0	0	General purpose input ADIN7
0	1	UID
1	0	Die temperature
1	1	Die temperature

9.5.6 Readout Comparison

As mentioned in the control section of this chapter, a readout comparison function is available. The two use cases, voltage and current comparison, are further developed as follows.

Table 9-16 regroups the key elements for the voltage comparison. The ADC voltage reading, without scaling, is presented in the table. The diagram shows on the X-axis the ADC reading as a 10 bit Code. The WLOW and WHIGH settings are represented as WLOW[5:0].0000 and WHIGH[5:0].0000 respectively to indicate that the comparison is done for the 6 MSB. The corresponding input voltage thresholds Vhigh and Vlow are derived from the WLOW[5:0] and WHIGH[5:0] setting according the given formulas.

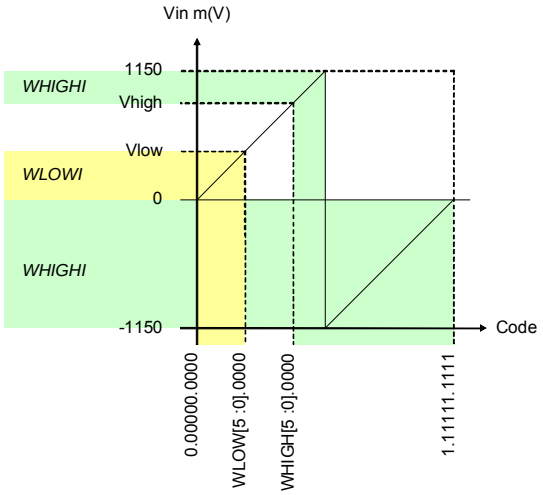
Table 9-16. Voltage Readout Comparison Summary

<table>
<tr><th>Code</th><th>Input ADC (mV)</th><td rowspan="4">$$Vhigh = \frac{2300}{2^{10}-1} \cdot \sum_{n=0}^{5} WHIGH(n) \cdot 2^{n+4} mV$$
$$Vlow = \frac{2300}{2^{10}-1} \cdot \sum_{n=0}^{5} WLOW(n) \cdot 2^{n+4} mV$$</td></tr>
<tr><td>1.11111.1111</td><td>1023*2300/1023=2300</td></tr>
<tr><td>0.00000.0001</td><td>1*2300/1023=2.25</td></tr>
<tr><td>0.00000.0000</td><td>0</td></tr>
<tr><td colspan="2"> 
</td><td>A WHIGHI interrupt is generated for Vin > Vhigh and a WLOWI for Vin < Vlow.
For proper use, WLOW[5:0] < WHIGH[5:0].</td></tr>
</table>

Two current reading channels are available, one for the battery current, and one for the charger current. The comparison function is only available for the charge current reading.

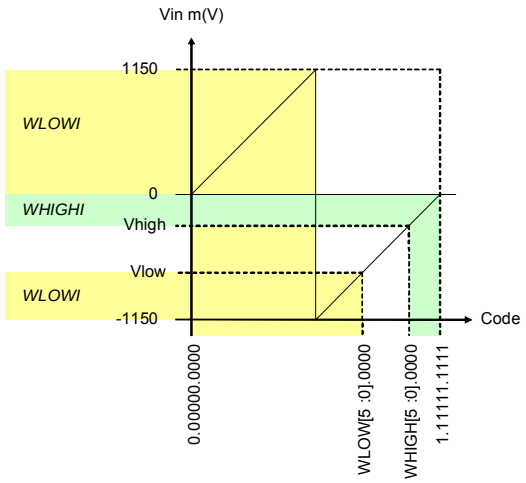
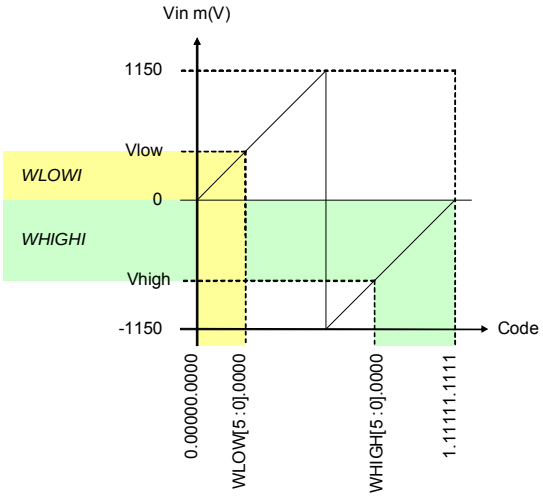
Table 9-17 regroups the key elements for the current comparison. The current is read out as a scaled voltage drop over a sense resistor. The ADC current reading is presented in a two's complement format as given in the table. The diagrams show on the X-axis the ADC reading as a 10 bit Code. The WLOW and WHIGH settings are represented as WLOW[5:0].0000 and WHIGH[5:0].0000 respectively to indicate that the comparison is done for the 6 MSB. The corresponding input voltage range is from 1150 mV to +1150 mV with the thresholds Vhigh and Vlow derived from the WLOW[5:0] and WHIGH[5:0] setting according the given formulas.

Table 9-17. Current Readout Comparison Summary

<table>
<tr><th>Code</th><th>Input ADC (mV)</th><td rowspan="6">$$Vhigh = \frac{2300}{2^{10}-1} \cdot \left[\left(\sum_{n=0}^{4} WHIGH(n) \cdot 2^{n+4} \right) - WHIGH(5) \cdot 2^{9} \right] mV$$
$$Vlow = \frac{2300}{2^{10}-1} \cdot \left[\left(\sum_{n=0}^{4} WLOW(n) \cdot 2^{n+4} \right) - WLOW(5) \cdot 2^{9} \right] mV$$</td></tr>
<tr><td>0.11111.1111</td><td>+511*2300/1023=1149</td></tr>
<tr><td>0.00000.0001</td><td>+1*2300/1023=2.25</td></tr>
<tr><td>0.00000.0000</td><td>0</td></tr>
<tr><td>1.11111.1111</td><td>-1*2300/1023=2.25</td></tr>
<tr><td>1.00000.0000</td><td>-512*2300/1023=1151</td></tr>
<tr><td colspan="2"> 
</td><td>Case 1: Positive Current Flow

When the current flow is expected to be positive, it follows that a WHIGHI interrupt is generated for Vin > Vhigh and a WLOWI for 0 < Vin < Vlow. Upon reversal of current a WHIGHI is generated. This setup can be used to detect a positive current getting out of range.</td></tr>
</table>

Table 9-17. Current Readout Comparison Summary (continued)

	Case 2: Negative Current Flow When the current flow is expected to be negative, it follows that a WHIGHI interrupt is generated for 0 > Vin > Vhigh and a WLOWI for Vin < Vlow. Since both Vhigh and Vlow are negative, the Vlow corresponds to currents with a higher magnitude then Vhigh. Upon reversal of current a WLOWI is generated. This setup can be used to detect a negative current getting out of range.
	Case 3: Alternate Current Flow When the current flow can be either negative or positive, it follows that a WHIGHI interrupt is generated for 0 > Vin > Vhigh and a WLOWI for 0 < Vin < Vlow. This case is shown for illustration purposes only because it is thought this is of little practical use.

9.6 Touch Screen Interface

The touchscreen interface provides all circuitry required for the readout of a 4-wire resistive touchscreen. The touchscreen X plate is connected to TSX1 and TSX2 while the Y plate is connected to TSY1 and TSY2. A local supply ADREF will serve as a reference. Several readout possibilities are offered.

In interrupt mode, a voltage is applied via a high impediment source to only one of the plates, the other is connected to ground. When the two plates make contact both will be at a low potential. This will generate a pen interrupt to the processor. This detection does not make use of the ADC core.

A finger will connect both plates over a wider area then a stylus. To distinguish both sources, in the contact resistance mode the resistance between the plates is measured by applying a voltage difference between the X and the Y plate. The current through the plates is measured.

Since the plate resistance varies from screen to screen, measuring its value will improve the pressure measurement. Also, it can help in determining if more than 1 spot is touched on the screen. In the plate

measurement mode, a potential is applied across one of the plates while the other plate is left floating. The current through the plate is measured.

The contact resistance mode and plate measurement mode are together referred to as resistive mode.

To determine the XY coordinate pair, in position mode a voltage difference over the X plate is read out via the Y plate for the X-coordinate and vice versa for the Y- coordinate readout. A special case of the position mode is the calibration mode in which the user will point with a stylus the opposite corners of the screen. This calibration step will allow to take into account the serial resistance in the display connector and the multiplexer for the later coordinate calculations. In the MC13783, during the position mode the contact resistance is read as well in addition to the XY coordinate pair.

The readout modes are set via the TSMOD[2:0] bits according to Table 9-18.

NOTE

In modes other than Inactive or Interrupt, normal control of group 2 ADC channels is no longer possible. Also, in these modes setting bits like RAND, ADSEL, ADA1[2:0] or WCOMP will have no effect.

Table 9-18. Touchscreen Mode Setting

TSMOD2	TSMOD1	TSMOD0	Touchscreen Mode	
0	0	0	Inactive Mode	TSX1/TSX2/TSY1/TSY2 used as general purpose inputs Input channels ADIN8-ADIN11 can be converted
0	0	1	Interrupt Mode	Generates an interrupt TSI when plates make contact. The ADEN bit does not need to be set to a 1 to enable this mode. TSI is dual edge sensitive and 30ms debounced
0	1	0	Resistive Mode	Sequential reading of X and Y plate and contact resistance. Input channels ADIN8-ADIN11 are not converted
0	1	1	Position Mode	Sequential reading of X and Y coordinate pairs and contact resistance Input channels ADIN8-ADIN11 are not converted
1	0	0	Inactive Mode	Same mode as for TSMOD[2:0]=000
1	0	1	Inactive Mode	Same mode as for TSMOD[2:0]=000
1	1	0	Inactive Mode	Same mode as for TSMOD[2:0]=000
1	1	1	Inactive Mode	Same mode as for TSMOD[2:0]=000

To perform touchscreen readings, the processor will have to set one of the touchscreen interface readout modes, program the delay between the conversions via the ATO and ATOX settings, trigger the ADC via one of the trigger sources, wait for an interrupt indicating the conversion is done, and then read out the data. In order to reduce the interrupt rate and to allow for easier noise rejection, the touchscreen readings are repeated in the readout sequence. In this way in total 8 results are available per readout.

Table 9-19. Touchscreen Reading Sequence

ADC Conversion	Signals Sampled in Resistive Mode	Signals Sampled in Position Mode	Readout Address[1]
0	X plate resistance	X position	000
1	X plate resistance	X position	001
2	X plate resistance	X position	010
3	Y plate resistance	Y position	011
4	Y plate resistance	Y position	100
5	Y plate resistance	Y position	101
6	Contact resistance	Contact resistance	110
7	Contact resistance	Contact resistance	111

1 Address as indicated by ADA1[2:0] and ADA2[2:0].

Figure 9-3 shows how the ATO and ATOX settings determine the readout sequence. The ATO must be set long enough so that the touchscreen can be biased properly before conversions start.

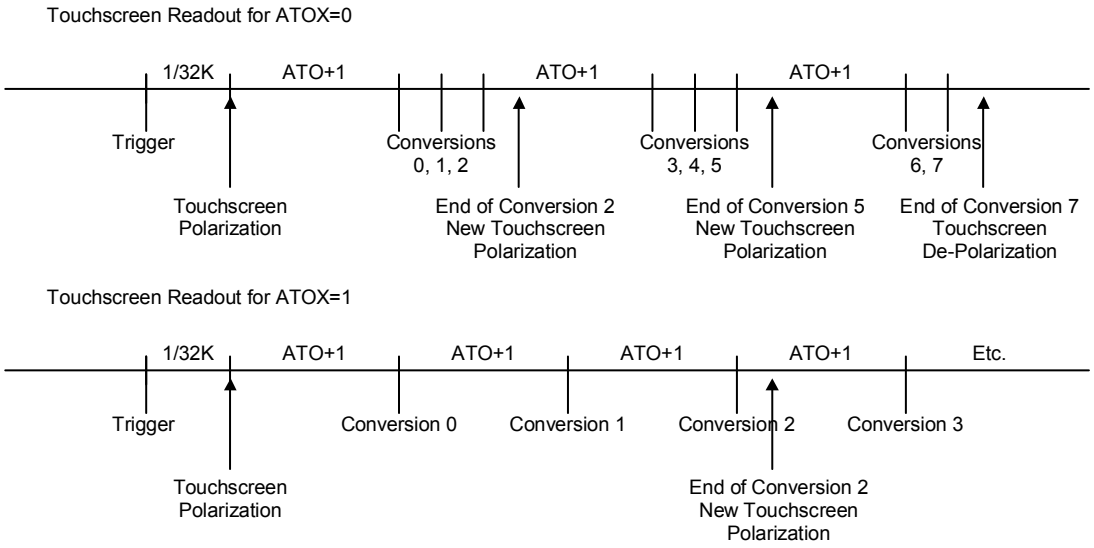


Figure 9-3. Touchscreen Reading Timing

The main resistive touchscreen panel characteristics are listed in Table 9-20. The switch matrix on the MC13783 is designed such that the switch resistances are of no influence on the overall readout.

Table 9-20. Touchscreen Interface Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Absolute Resistive Measurement Inaccuracy	Over temperature	—	—	20	%
Plate Resistance X, Y	—	100	—	1000	Ohm

Table 9-20. Touchscreen Interface Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Unit
Resistance Between Plates	Contact	180	400	—	Ohm
	Pressure	180	—	1000	Ohm
Settling Time	Position measurement	3	—	5.5	us
Capacitance Between Plates	—	0.5	2	—	nf

The reference for the touchscreen is ADREF. It is a dedicated regulator, that is to say, no other loads than the touchscreen must be connected here. For non touchscreen operation the ADC does not rely on ADREF and the reference can be disabled. In non touchscreen applications ADREF will never get enabled and the bypass capacitor of ADREF can be omitted. The operating mode of ADREF can be controlled with the ADREFEN and ADREFMODE bits in the same way as the other general purpose regulators are controlled, see also Chapter 5, “Power Control System”. While the rest of the ADC is powered from VATLAS, the ADREF regulator is internally powered from BP.

Table 9-21. ADC Reference Characteristics

Parameter	Condition	Min	Typ	Max	Units
Quiescent Current	Active Mode	—	20	—	uA
	Low-Power Mode	—	5	—	uA
Off Current	—	—	1	—	uA
Max Load Current	Active Mode	—	—	25	mA
	Low-Power Mode	—	—	1	mA
Output Voltage	1<IL<25 mA	-3%	2.30	+3%	V
Load Regulation	1<IL<25 mA	—	—	0.5	mV/mA
Line Regulation	1<IL<25 mA	—	—	20	mV
PSRR	IL = 5 mA	40	—	—	dB
Turn-on Time	90% of output	—	—	500	us
Bypass Capacitor ESR	—	0	—	0.5	Ohm
Bypass Capacitance	—	—	2.2	—	uF
Discharge Resistor	Regulator disable	—	100	—	Ohm

9.7 ADC Arbitration

The ADC convertor and its control is based on a single ADC convertor core with the possibility to store two requests and their results. There are 3 main operating modes for the arbitration control which are set via the ADCSEL[1:0] bits, see Table 9-22. These bits are located in the “Arbitration Peripheral Audio” register which is only accessible via the primary SPI. These bits are set at startup and are not to be reconfigured dynamically during phone operation.

Table 9-22. ADC Arbitration Control

ADCSEL1	ADCSEL0	Arbitration Control
0	0	Primary SPI can queue a single ADC conversion request Secondary SPI can queue a single ADC conversion request
0	1	Primary SPI can queue two ADC conversion requests Secondary SPI has no ADC access.
1	0	Primary SPI has no ADC access (except for the arbitration control itself). Secondary SPI can queue two ADC conversion requests
1	1	Will give same operating mode as for ADSEL[1:0]=00
Note: ADCSEL[1:0] are not the same bits as ADSEL which selects the group to be converted.		

Figure 9-4 depicts the ADC configuration as a function of the arbitration setting ADSEL[1:0].

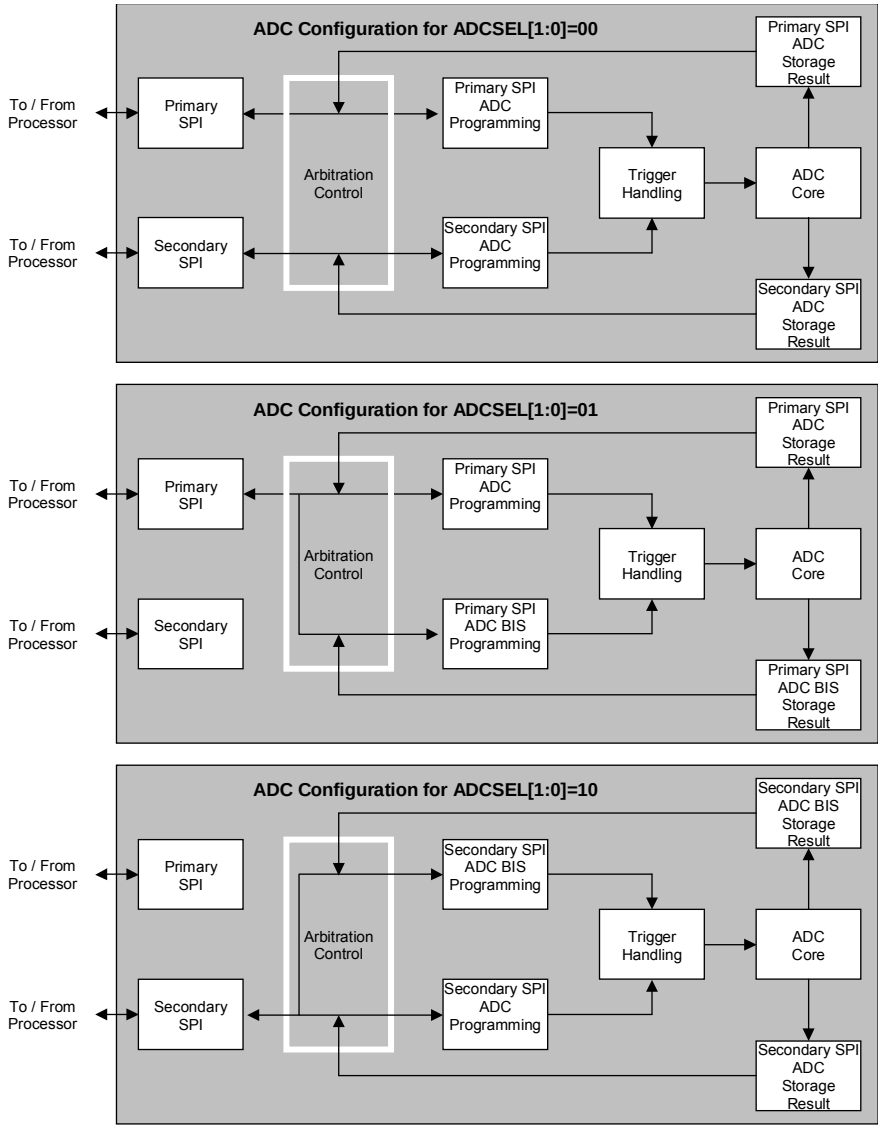


Figure 9-4. ADC Configurations

NOTE

Each of the ADC requests can be programmed for conversions of group 0 (channels 0-7, battery management related channels) or group 1 (channels 8-15, touchscreen and ambient light related channels).

In case of dual SPI access, the primary SPI set will address the primary SPI ADC and the secondary SPI set the secondary SPI ADC. In case of single SPI access, the single SPI must have the ability to write to the two sets of ADC control, namely 'its own' ADC and 'the other' ADC or ADC BIS. The write access to the control of ADC BIS is handled via the ADCBISn bits located at bit position 23 of the ADC control registers. By setting this bit to a 1, the control bits which follow are destined for the ADC BIS. ADCBISn will always read back 0 and there is no read access to the ADCBIS control bits.

The read results from the ADC and ADC BIS conversions are available in two separate registers. This means that ADC software can be strictly identical independent if it runs via the primary or secondary SPI. It also means that in case of dual SPI control, the same result register address is used by both SPIs. In case of dual SPI control, so ADCSEL[1:0]=00, the ADCBISn bit will have no function and are a don't care.

Figure 9-5 schematically shows how the ADC control and result registers are set up.

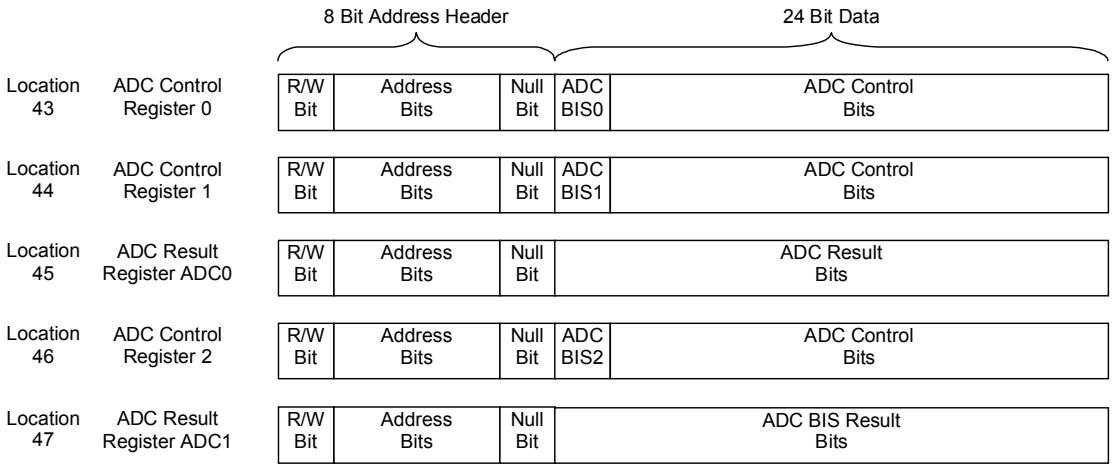


Figure 9-5. ADC Register Set for ADC BIS Access

There are two interrupts available to inform the processor when the ADC has finished its conversions. The ADCDONEI interrupt will go high after the conversion for ADC has finished, and ADCBISDONEI will go high after the conversion for ADC BIS has finished. Although both interrupts are available for both SPIs, only the interrupts to the SPI requesting the conversions are generated. This is depicted in Table 9-23. The interrupts can be masked.

Table 9-23. ADCDONE Interrupt Logic

	Pri SPI		Sec SPI	
	ADCDONEI	**ADCBISDONEI**	**ADCDONEI**	**ADCBISDONEI**
ADCSEL0: ADCSEL1 = 0: 0 or 1: 1				
Pri SPI ADC Conversion Request finished	1	0	0	0
Sec SPI ADC Conversion Request finished	0	0	1	0

Table 9-23. ADCDONE Interrupt Logic (continued)

	Pri SPI		Sec SPI	
	ADCDONEI	**ADCBISDONEI**	**ADCDONEI**	**ADCBISDONEI**
ADCSEL0: ADCSEL1 = 0: 1				
Pri SPI ADC Conversion Request finished	1	0	0	0
Pri SPI ADCBIS Conversion Request finished	0	1	0	0
ADCSEL0: ADCSEL1 = 1: 0				
Sec SPI ADC Conversion Request finished	0	0	1	0
Sec SPI ADCBIS Conversion Request finished	0	0	0	1

There is only a single set of WHIGHI and WLOWI interrupt bits provided per SPI bus. This means that when queueing two ADC conversion requests on a single SPI, the WCOMP must only be used on the non BIS conversion requests.

When two requests are queued, the request for which the trigger event occurs the first will be converted the first. During the conversion of the first request, an ADTRIG trigger event of the other request is ignored if for the other request the TRIGMASK bit was set to 1. When this bit is set to 0, the other request ADTRIG trigger event is memorized, and the conversion will take place directly after the conversions of the first request are finished. It is not advised to use ADTRIG as a trigger event for two queued requests, this will lead to read out conflicts.

Figure 9-6 shows the influence of the TRIGMASK bit. The TRIGMASK bit is particularly of use when an ADC conversion has to be lined up to a periodically ADTRIG initiated conversion. In case of ASC initiated conversions, the TRIGMASK bit is of no influence.

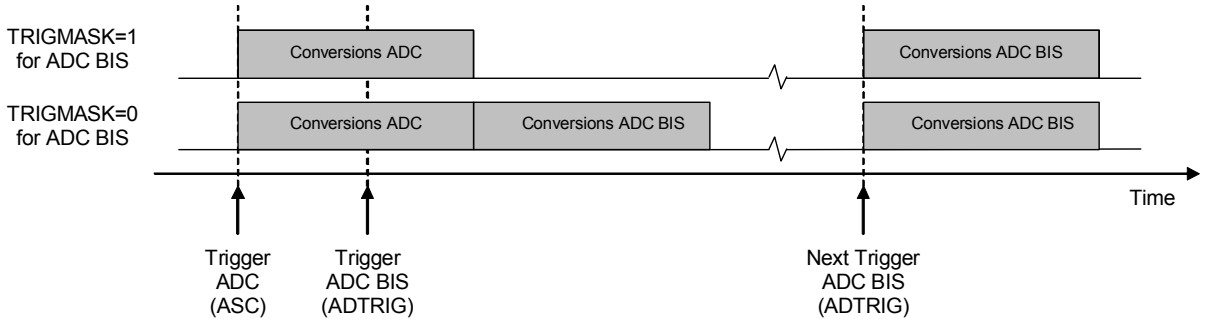


Figure 9-6. TRIGMASK Functional Diagram

To avoid that results of previous conversions get overwritten by a periodical ADTRIG signal, a single shot function is available which will make only a single set of conversions will be executed. The single shot function is enabled by setting the ADONESHOT bit to a one and in that case one and only one ADTRIG trigger event is accepted. In order to perform a new single shot conversion, the ADONESHOT bit needs to be cleared followed by a dummy conversion. After the dummy conversion has finished, the ADC can again be reprogrammed for a single shot conversion via ADONESHOT.

NOTE

This bit is available for each of the conversion requests ADC or ADC BIS, so can be set independently.

When the ADC is not active, a specific arbitration is implemented for the touchscreen interface. The TSMOD[2:0] bits from both SPIs are first bitwise OR-ed and the result is used to set the touchscreen mode. This means in practice that the touchscreen interface is to be controlled via only one of the SPIs. The other SPI will have to set its TSMOD[2:0] bits to all zero. If the ADC is performing a conversion then the TSMOD[2:0] from the SPI port that initiated the conversion will determine the mode of touchscreen interface and the TSMOD[2:0] bits of the other SPI are of no interest.

One can distinguish 3 types of potential conflicting requests coming from the software when overwriting the current ADC control settings, so overwriting the same control bit locations. Conflicts can be avoided by a proper use of the interrupt mechanism. In the following examples the programming occurs via the same SPI and for the same control bit locations with for example ADCBISn=0.

- Sequential Requests: The SPI has requested a conversion, the ADC starts the conversion, the ADC finishes, the SPI does a new request for a conversion. In this case the second request is executed and the results of the first request are overwritten. An ADCDONEI however was generated when the ADC finished the conversions of the first request.
- Overlapping Requests: The SPI has requested a conversion, the ADC starts the conversion, the ADC is converting, the SPI does a new request for a conversion. In this case, writing to the SPI while the first ADC request is executed must be considered as a programming error since an ADCDONEI was yet not generated. Effectively, the contents of the SPI register get changed and therefore the behavior of the conversion which is ongoing.
- Overruling Requests: The primary SPI has requested a conversion, the ADC did not start the conversion, the primary SPI does a new request for a conversion. In this case the first request does not get executed and only the second one. This can be the case for an ADTRIG based first request while the ADTRIG does not show up. Also in this case an ADCDONEI was not generated and an overruling request can therefore in practice become an overlapping request.

9.8 ADC Control Register Summary

Table 9-24. Register 43, ADC 0

Name	Bit #	R/W	Reset	Default	Description
LICELLCON	0	R/W	RESETB	0	Enables lithium cell reading
CHRGICON	1	R/W	RESETB	0	Enables charge current reading
BATICON	2	R/W	RESETB	0	Enables battery current reading
RTHEN	3	R/W	RESETB	0	Enables thermistor reading
DTHEN	4	R/W	RESETB	0	Enables die temperature reading
UIDEN	5	R/W	RESETB	0	Enables UID reading
ADOUTEN	6	R/W	RESETB	0	Enables the pulse at the ADOUT pin
ADOUTPER	7	R/W	RESETB	0	Sets the ADOUT period

Table 9-24. Register 43, ADC 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
Reserved	8	R/W	RESETB	0	For future use
Reserved	9	R/W	RESETB	0	For future use
ADREFEN	10	R/W	RESETB	0	Enables the touchscreen reference
ADREFMODE	11	R/W	RESETB	0	Sets the touchscreen reference mode
TSMOD0	12	R/W	RESETB	0	Sets the touchscreen mode
TSMOD1	13	R/W	RESETB	0	—
TSMOD2	14	R/W	RESETB	0	—
CHRGRAWDIV	15	R/W	RESETB	1	Sets CHRGRAW scaling to divide by 5
ADINC1	16	R/W	RESETB	0	Auto increment for ADA1
ADINC2	17	R/W	RESETB	0	Auto increment for ADA2
WCOMP	18	R/W	RESETB	0	Normal conversion mode with limit comparison
Reserved	19	R/W	RESETB	0	For future use
Reserved	20	R/W	RESETB	0	For future use
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
ADCBIS0	23	W	—	0	Access to the ADCBIS control

Table 9-25. Register 44, ADC 1

Name	Bit #	R/W	Reset	Default	Description
ADEN	0	R/W	RESETB	0	Enables the ADC
RAND	1	R/W	RESETB	0	Sets the single channel mode
Reserved	2	R/W	RESETB	0	For future use
ADSEL	3	R/W	RESETB	0	Selects the set of inputs
TRIGMASK	4	R/W	RESETB	0	Trigger event masking
ADA10	5	R/W	RESETB	0	Channel selection 1
ADA11	6	R/W	RESETB	0	—
ADA12	7	R/W	RESETB	0	—
ADA20	8	R/W	RESETB	0	Channel selection 2
ADA21	9	R/W	RESETB	0	—
ADA22	10	R/W	RESETB	0	—
ATO0	11	R/W	RESETB	0	Delay before first conversion
ATO1	12	R/W	RESETB	0	—
ATO2	13	R/W	RESETB	0	—

Table 9-25. Register 44, ADC 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
ATO3	14	R/W	RESETB	0	—
ATO4	15	R/W	RESETB	0	—
ATO5	16	R/W	RESETB	0	—
ATO6	17	R/W	RESETB	0	—
ATO7	18	R/W	RESETB	0	—
ATOX	19	R/W	RESETB	0	Sets ATO delay for any conversion
ASC	20	R/W	RESETB	0	Starts conversion
ADTRIGIGN	21	R/W	RESETB	0	Ignores the ADTRIG input
ADONESHOT	22	R/W	RESETB	0	Single trigger event only
ADCBIS1	23	W	RESETB	0	Access to the ADCBIS control

Table 9-26. Register 45, ADC 2

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R	NONE	0	For future 12 bit use
Reserved	1	R	NONE	0	—
ADD10	2	R	NONE	0	Results for channel selection 1
ADD11	3	R	NONE	0	—
ADD12	4	R	NONE	0	—
ADD13	5	R	NONE	0	—
ADD14	6	R	NONE	0	—
ADD15	7	R	NONE	0	—
ADD16	8	R	NONE	0	—
ADD17	9	R	NONE	0	—
ADD18	10	R	NONE	0	—
ADD19	11	R	NONE	0	—
Reserved	12	R	NONE	0	For future 12 bit use
Reserved	13	R	NONE	0	—
ADD20	14	R	NONE	0	Results for channel selection 2
ADD21	15	R	NONE	0	—
ADD22	16	R	NONE	0	—
ADD23	17	R	NONE	0	—
ADD24	18	R	NONE	0	—
ADD25	19	R	NONE	0	—

Table 9-26. Register 45, ADC 2 (continued)

Name	Bit #	R/W	Reset	Default	Description
ADD26	20	R	NONE	0	—
ADD27	21	R	NONE	0	—
ADD28	22	R	NONE	0	—
ADD29	23	R	NONE	0	—

Table 9-27. Register 46, ADC 3

Name	Bit #	R/W	Reset	Default	Description
WHIGH0	0	R/W	RESETB	0	Comparator high level in WCOMP mode
WHIGH1	1	R/W	RESETB	0	—
WHIGH2	2	R/W	RESETB	0	—
WHIGH3	3	R/W	RESETB	0	—
WHIGH4	4	R/W	RESETB	0	—
WHIGH5	5	R/W	RESETB	0	—
ICID0	6	R/W	NONE	0	MC13783 derivative
ICID1	7	R/W	NONE	1	—
ICID2	8	R/W	NONE	0	—
WLOW0	9	R/W	RESETB	0	Comparator low level in WCOMP mode
WLOW1	10	R/W	RESETB	0	—
WLOW2	11	R/W	RESETB	0	—
WLOW3	12	R/W	RESETB	0	—
WLOW4	13	R/W	RESETB	0	—
WLOW5	14	R/W	RESETB	0	—
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
ADCBIS2	23	W	RESETB	0	Access to the ADCBIS control

Table 9-28. Register 47, ADC 4

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R	NONE	0	For future 12 bit use
Reserved	1	R	NONE	0	—
ADDBIS10	2	R	NONE	0	Result for channel selection 1 of ADCBIS
ADDBIS11	3	R	NONE	0	—
ADDBIS12	4	R	NONE	0	—
ADDBIS13	5	R	NONE	0	—
ADDBIS14	6	R	NONE	0	—
ADDBIS15	7	R	NONE	0	—
ADDBIS16	8	R	NONE	0	—
ADDBIS17	9	R	NONE	0	—
ADDBIS18	10	R	NONE	0	—
ADDBIS19	11	R	NONE	0	—
Reserved	12	R	NONE	0	For future 12 bit use
Reserved	13	R	NONE	0	—
ADDBIS20	14	R	NONE	0	Result for channel selection 2 of ADCBIS
ADDBIS21	15	R	NONE	0	—
ADDBIS22	16	R	NONE	0	—
ADDBIS23	17	R	NONE	0	—
ADDBIS24	18	R	NONE	0	—
ADDBIS25	19	R	NONE	0	—
ADDBIS26	20	R	NONE	0	—
ADDBIS27	21	R	NONE	0	—
ADDBIS28	22	R	NONE	0	—
ADDBIS29	23	R	NONE	0	—

Chapter 10
Connectivity

The connectivity interface includes USB, RS232 and CEA-936-A capability. The connectivity interface is programmed into one of these modes by the CONMODE[2:0] provided in Table 10-1. For details on each of these settings, please refer to the related sections.

Table 10-1. Connectivity Interface

CONMODE[2:0]	Connectivity Interface Mode
000	USB
001	RS232
010	
011	Reserved
100	CEA-936-A
101	
110	
111	

10.1 USB Interface

10.1.1 Supplies

The USB interface is supplied by the VUSB and the VBUS regulators. The VBUS regulator takes the boost supply and regulates it down to the required USB-OTG level which is provided to VBUS in the case of a USB-OTG connection. The transceiver itself is supplied from VUSB. The VUSB regulator by default is supplied by BP via the VINIOHI pin and by SPI programming can be boost or VBUS supplied as well.

Since in the common input modes (CHRGMOD1=HiZ) the VBUS can be joined with the charger input, see Chapter 8, “Battery Interface and Control”, the VBUS node must be able to withstand in this configuration the same high voltages as the charger. To obtain this, for input voltages higher than the USB specification, the USB interface is internally disconnected from VBUS. Also, outside the specified range the VUSB regulator will not be operational if supplied from VBUS. In the separate input modes (CHRGMOD1=VATLAS) this mechanism is not operational and VBUS can only withstand the standard USB fault mode voltages.

Table 10-2. VUSB Control Register Bit Assignments

Parameter	Value	Function
VUSB	0	output = 3.2 V
	1	output = 3.3 V[1]
VUSBIN[1:0]	00	input = Boost via VINBUS, default in boot mode
	01	input = VBUS
	10	input = BP (VINVIB), default in non boot modes
	11	input = VBUS

1 Required for CONMODE[2:0]=000 and UID current pull up.

Table 10-3. VUSB Regulator Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax		4.2	5.0	6.0	V
Operating Current Load Range ILmin to ILmax	USB transceiver disabled[1]	0	—	50	mA
Extended Input Voltage Range	Performance may be out of specification	2.7	—	6.0	V
Bypass Capacitor Value Range		0.65	1.0	6.58	uF
Bypass Capacitor ESR	10 kHz–1 MHz	0	—	0.1	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom - 3%	Vnom	Vnom + 3%	V
Load Regulation	0 < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.40	mV/mA
Line Regulation	Vinmin < Vin < Vinmax For any ILmin < IL < ILmax	—	—	20	mV
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	80	—	350	mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	uA
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vinmin + 100 mV	35	40	—	dB
	Vin = Vnom + 1 V	50	60	—	dB

Table 10-3. VUSB Regulator Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Output Noise	Vin = Vinmin IL = 75% of ILmax	—	—	—	—
	100 Hz – 50 kHz	—	—	1	uV/√Hz
	50 kHz – 1 MHz	—	—	0.2	uV/√Hz
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	1	ms
Turn-Off Time	Disable to 10% of initial value Vin = Vinmin, Vinmax IL = 0	0.1	—	10	ms
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	1	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV

[1] When the USB transceiver is enabled and transmitting, its current drain has to be taken into account.

Table 10-4. VBUS Regulator Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
General					
Operating Input Voltage Range Vinmin to Vinmax	Supplied by boost convertor	5.2	5.5	6.0	V
Operating Current Load Range ILmin to ILmax		0	—	100	mA
Extended Input Voltage Range	Performance may be out of specification	4.75	—	6.0	V
Bypass Capacitor Value Range		1.3	2.2	6.5	uF
Bypass Capacitor ESR	10 kHz - 1 MHz	0.47	—	1.0	Ω
Active Mode - DC					
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	4.5	5.0	5.15	V
Current Limit	Vinmin < Vin < Vinmax Short circuit Vout to ground	—	—	—	—
	High Limit Ilimhi	100	—	300	mA
	Low Limit Ilimlo	600	—	1550	uA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0 Measured from VINBUS and BP	—	200	—	uA

Table 10-4. VBUS Regulator Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Active Mode - AC					
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz	—	—	—	—
	Vin = Vnom + 1 V	35	40	—	dB
Turn-On Time	Enable to 90% of end value Vin = Vinmin, Vinmax IL = 0	—	—	2	ms
Turn-Off Time	Disable to 0.8 V, per USB-OTG specification parameter VA_SESS_VLD Vin = Vinmin, Vinmax IL = 0	—	—	1.3	s
Start-Up Overshoot	Vin = Vinmin, Vinmax IL = 0	—	1	2	%
Transient Load Response	See waveform Vin = Vinmin, Vinmax	—	—	2	%
Transient Line Response	See waveform IL = 75% of ILmax	—	5	8	mV
Internal Discharge Resistor on Regulator Output	Per USB-OTG specification parameter RA_BUS_IN	40	70	100	KΩ

10.1.2 Detect

Three comparators are used to detect the voltage level on VBUS. These are USBDET4V4 to detect a valid VBUS, and USBDET2V0 and USBDET0V8 to support the USB OTG session request protocol. The comparators have each their own sense bit located in the interrupt sense register. These are USB4V4S, USB2V0S and USB0V8S respectively. The sense bits are a logic 1 when the VBUS level is above the detected threshold. On any rising and falling edge of the comparator outputs, and thus whenever one of the sense bits changes state, a USBI interrupt is generated. Only in case of USBDET4V4 the interrupt is debounced, there is no debounce for the USBDET2V0 and USBDET0V8 detection. The interrupt can be masked via the USBM bit. VBUS can be connected to the charger input pin in case of a joined charger and USB connector, see Chapter 8, “Battery Interface and Control”.

Table 10-5. USB Detect Main Characteristics

Parameter	Condition	Min	Typ	Max	Units
USBDET4V4 Comparator turn on threshold	—	4.4	—	4.65	V
USBDET4V4 Comparator turnoff threshold	—	4.4	—	4.65	V
USBDET4V4 Comparator hysteresis	—	0	—	150	mV

Table 10-5. USB Detect Main Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
USBDET4V4 turn-on delay	Including the USBI debounce	—	—	—	—
	Rising edge	15	—	20	ms
	Falling edge	0.5	—	1.5	ms
USBDET2V0 Comparator turn on threshold	—	1.6	—	2.0	V
USBDET2V0 Comparator turnoff threshold	—	1.6	—	2.0	V
USBDET2V0 Comparator hysteresis	—	0	—	150	mV
USBDET2V0 turn-on delay	—	—	—	100	µs
USBDET0V8 Comparator turnoff threshold	—	0.6	—	0.8	V
USBDET0V8 turn-on delay	—	—	—	100	µs
Over Voltage Protection Level	Limits include rising and falling edge	5.6	—	5.9	V
Over Voltage Protection Disconnect Time	—	—	—	1	us

10.1.3 Transceiver

The USB transceiver data flow is depicted in Figure 10-1.

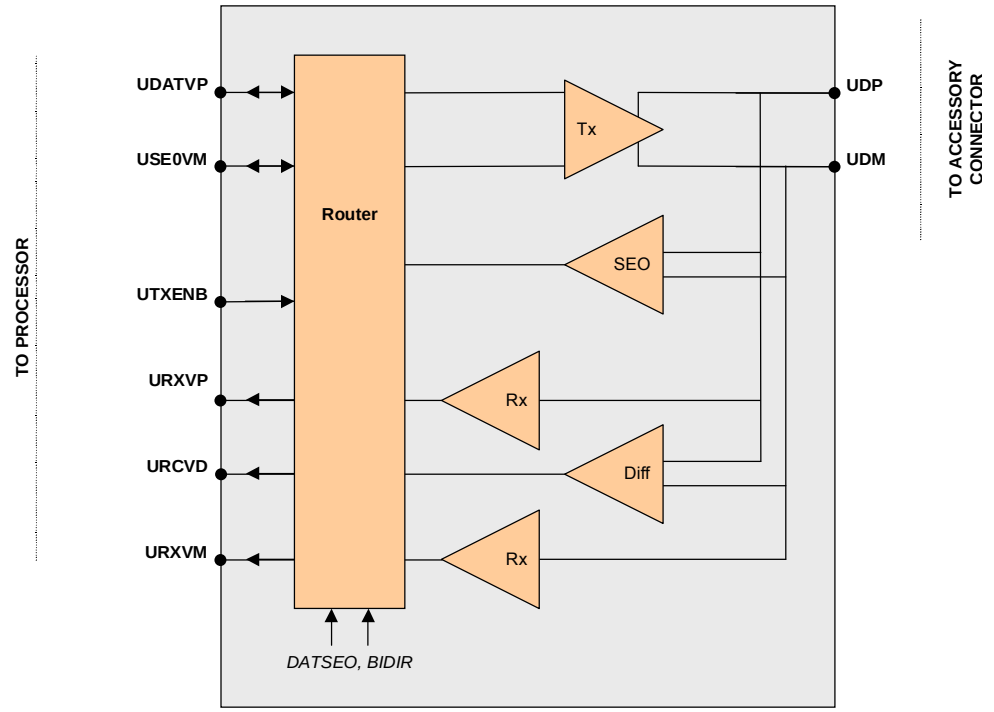


Figure 10-1. USB/RS232 Transceiver Data Flow

In the USB mode of operation, circuitry is provided to prevent sneak path conduction of parasitic pn junctions in the tri-stated RS232 buffers. Additionally, VBUS may be applied when no other external voltage to the IC is present. In this non-operational condition, circuitry is provided to prevent sneak path

conduction of parasitic pn junctions in the tri-stated USB and RS232 buffers. In addition, during a fault condition in the USB cable, it is possible to short VBUS to either UDP, UDM or UID for an indefinite period. Circuitry is provided to prevent conduction into UDP, UDM or UID during this fault condition, and the IC will be capable of withstanding the USB specified VBUS maximum voltage on UDP, UDM and UID under these conditions.

During phone ON, the USB transceiver is enabled when the SPI bit USBXCVREN is set high. Upon a USB legacy host detection, see detection section, an interrupt USBI is generated but neither the transceiver nor the VUSB regulator are automatically enabled. This must be done by software before data transmission. The transceiver is also enabled during boot mode as described in the boot support section of this chapter.

The USB transceiver data formatting operates in four modes, defined by the DATSE0 and BIDIR SPI bits:

DATSE0=1, BIDIR=0: In *single ended unidirectional* mode, only if UTXENB is low then data present on UDATVP is output differentially on UDM and UDP. If USE0VM is high then both UDM and UDP are low regardless of the state of UDATVP. This corresponds to a single ended low (SE0). Independent of the state of TXENB, the data received differentially on UDP and UDM is output on URCVD, while URXVP will follow UDP and URXVM will follow UDM. A total of 6 wires for the processor interface is used.

DATSE0=1, BIDIR=1: In *single ended bidirectional* mode, only if UTXENB is low then data present on UDATVP is output differentially on UDM and UDP. If USE0VM is high then both UDM and UDP are low regardless of the state of UDATVP. This corresponds to a single ended low. If UTXENB is high, the data received differentially on UDP and UDM is output on UDATVP, while USE0VM will be high when a SE0 is detected. During suspend, UDATVP will follow UDP. The buffers on URXVP, URXVM, and URCVD are not tri-stated in this mode and follow the (differential) data on UDP and UDM. A total of 3 wires for the processor interface is used.

DATSE0=0, BIDIR=0: In *differential unidirectional* mode, only if UTXENB is low then data present on UDATVP and USE0VM is output on UDP and UDM respectively. In fact, the UDP signal will follow the UDATVP input signal, with the UDM signal being the complement of UDP as long as no single-ended zero state is received. At the inputs UDATVP and USE0VM a SE0 state shall not occur between bits of normal data transmission, while single-ended one states are acceptable. The SE0 is transmitted by setting both UDATVP and USE0VM low simultaneously. Independent of the state of TXENB, the data received differentially on UDP and UDM is output on URCVD, while URXVP will follow UDP and URXVM will follow UDM. A total of 6 wires for the processor interface is used.

DATSE0=0, BIDIR=1: In *differential bidirectional* mode, if UTXENB is low then data present on UDATVP and USE0VM is output on UDP and UDM respectively. In fact, the UDP signal will follow the UDATVP input signal, with the UDM signal being the complement of UDP as long as no single-ended zero state is received. At the inputs UDATVP and USE0VM a SE0 state shall not occur between bits of normal data transmission, while single-ended one states are acceptable. The SE0 is transmitted by setting both UDATVP and USE0VM low simultaneously. If UTXENB is high, the data received differentially on UDP and UDM is output on URCVD, while UDATVP will follow UDP and USE0VM will follow UDM. The buffers on URXVP and URXVM are not tri-stated in this mode and follow the data on UDP and UDM. A total of 4 wires for the processor interface is used.

In all data modes the receiver is disabled and the outputs tri-stated when the USB transceiver is not enabled. This is the case when the USBEN pin is low while bit USBCNTRL=1, or when bit USBCNTRL=0 with bit USBXCVREN=0.

Table 10-6 summarizes the four operating modes.

Table 10-6. USB Mode Selection

USB Mode		Mode Selection		Mode Description		Corresponding UMOD0/UMOD1 Setting
		DATSE0	BIDIR	UTXENB = Low	UTXENB = High	
Differential	unidirectional (6-wire)	0	0	UDATVP → UDP USE0VM → UDM	UDP → URXVP UDM → URXVM UDP/UDM → URCVD	Don't Care / To VATLAS
	bidirectional (4-wire)		1	UDATVP → UDP USE0VM → UDM	UDP → UDATVP UDM → USE0VM UDP/UDM → URCVD	To VATLAS / To Ground
Single Ended	unidirectional (6-wire)	1	0	UDATVP→ UDP/UDM USE0VM → FSE0	UDP → URXVP UDM → URXVM UDP/UDM → URCVD	To Ground / To Ground
	bidirectional (3-wire)		1	UDATVP → UDP/UDM USE0VM → FSE0	UDP/UDM → UDATVP (active) UDP → UDATVP (suspend) RSE0 → USE0VM	Open / To Ground
Note: FSE0 stands for forced SE0, RSE0 stands for received SE0.						

Via SPI bits DATSE0 and BIDIR, one of the four operating modes can be selected. However, when starting up in a boot mode, there is no up front SPI programming possible. The default operating mode is then determined by the setting of the UMOD0 and UMOD1 pin as indicated in Table 10-6.

NOTE

The UMOD0 is a ternary pin and UMOD1 a binary pin. When UMOD1 is left open, the pin will be pulled to ground by the internal weak pull down.

The processor interface I/O level is set to USBVCC.

10.1.4 Full Speed/ Low Speed Configuration

The USB transceiver supports the low speed mode of 1.5 Mbits/second and the full speed mode of 12 Mbits/second. To indicate the speed to the host an internal 1.5 kOhm pull up to VUSB is used. Via SPI bit FSENB this resistor can be connected to UDP to indicate full speed, or to UDM to indicate low speed. The USBPU bit has to be set to a 1 to physically connect the resistor to VUSB. Since a 5% resistor cannot be implemented as such on silicon, the actual implementation is based on the USB engineering change notice 'pull-up/pull-down resistors' which selects different wider spread resistors depending on the USB operating mode detected. The USB High Speed mode of 480 Mbit/second is not supported.

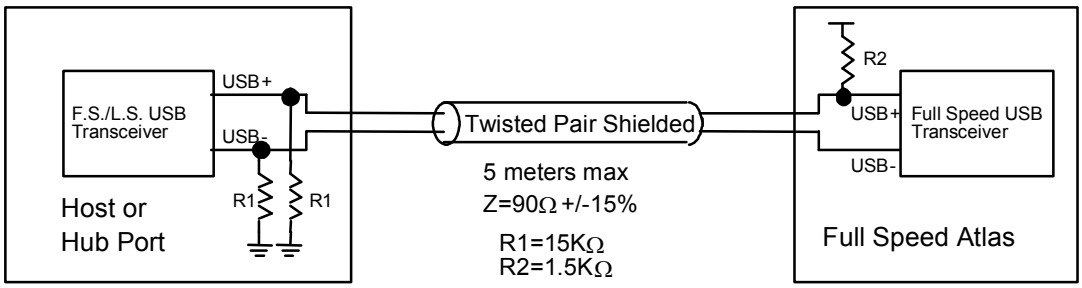


Figure 10-2. Full Speed USB Termination

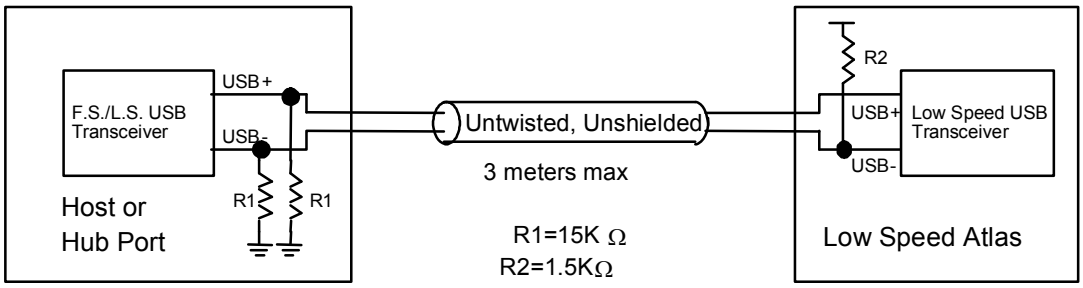


Figure 10-3. Low Speed USB Termination

10.1.5 USB Suspend

USB suspend mode is enabled through the SPI bit USBSUSPEND. When set, the USB transceiver enters a low-power mode which reduces the transceiver current drain to below 500 µA. In USB suspend mode, the VUSB regulator remains enabled and the VBUS detect comparators remain enabled, while the single ended receivers are switched from a comparator to a Schmitt-trigger buffer. In USB suspend mode, the 1.5 K internal resistor is pulled up to VUSB. In USB suspend mode, the USB differential transmit driver and differential receive comparator are disabled and put into a low-power mode. Note the specific case of bidirectional single ended mode where the UDP Schmitt-trigger buffer output is multiplexed onto the UDATVP pin, while a received SE0 is flagged via USE0VM.

10.1.6 USB On-The-Go

USB On-the-Go (OTG) is defined in a supplement to the USB 2.0 specification and covers several modifications. First, the USB-OTG supplement defines a set of connectors and receptacles for use with USB-OTG devices. Second, the USB-OTG specification allows for *dual-role* devices, which can act as either a host or a peripheral device depending on the situation. Finally, the power required to be provided to the bus as a host device was greatly reduced (from 100 mA to 8 mA). See the USB On-The-Go supplement to USB 2.0 for full details on USB On-The-Go.

USB-OTG support circuitry is added in order to allow a phone to act as a dual-role USB-OTG device. In accordance with USB-OTG requirements, the pull down resistors on UDP and UDM can be switched in or out individually via the SPI bits UDPPD and UDMPD (if UDPPD = 1 or UDMPD = 1, the pull downs are switched in). Furthermore, the pulls down resistors are integrated on-chip. This is acceptable for USB-OTG, since all USB timing and voltage level requirements can still be met, even though the USB 2.0

specification suggests the use of 15 k. 5% pull down resistors. The 1.5 k internal pull-up resistor is switched in and out via the SPI bit USBPU (if USBPU =1, the pull up is switched in).

The USB-OTG specification requires that during the session request protocol, the D+ (full speed) line is pulled up for a duration of 5 ms to 10 ms. To reduce the SPI traffic, the SPI bit DLPSRP will be used to time this task. When the DLPSRP = 1 and USBPU = 0 a timer will run for 7.5 ms, and then the pull-up will be disconnected and the DLPSRP bit will revert back to zero. When the bit USBPU = 1, the pull-up will remain connected independent of the setting of DLPSRP.

The 1.5 k and the two pull downs are disconnected from the UDP and UDM lines during transmit. This is controlled via the UTXENB input, such that when the transceiver is in transmit mode, the internal control signals are overridden and the pull-ups/downs are disconnected. This is done to save battery power. The SPI bit PULLOVR disables this function and allows the internal registers to connect/disconnect the pull-ups.

To support VBUS pulsing, there is a programmable current limit and timer on the VBUS regulator. This is controlled via the VBUSPULSETMR[2:0] bits as given in Table 10-7. When the low current limit is set, the VBUS regulator is used as a current source, which is necessary in order to implement the VBUS pulsing method of session request protocol (SRP) as defined in the USB-OTG supplement. When the pulse timer expires, the VBUSPULSETMR[2:0] bits are reset to 0 and the current limit reverts back to its high level.

Table 10-7. VBUS Current Limit Setting

Parameter	Value	Current Limit	Pulse Duration
VBUSPULSETMR[2:0]	000	Ilimhi	Not applicable
	001	Ilimlo	10 ms
	010	Ilimlo	20 ms
	011	Ilimlo	30 ms
	100	Ilimlo	40 ms
	101	Ilimlo	50 ms
	110	Ilimlo	60 ms
	111	Ilimlo	Infinite
Note: See VBUS regulator characteristics for Ilimhi and Ilimlo values. VBUS is automatically enabled if VBUSPULSETMR[2:0] is not 000 or 111.			

During VBUS pulsing, the lower current limit allows for easier detection of a legacy host device on the far end of the USB cable (the timing requirements are less restrictive than if the higher current limit is utilized). The detection method is based upon the legacy host requirement to have a minimum of 96uF of capacitance on VBUS, whereas the maximum capacitance that a dual-role device can have on VBUS is 6.5 uF. Using this order of magnitude difference, an OTG dual-role device can limit the amount of charge that is placed on the bus by limiting the time that the VBUS regulator is turned on. This ensures that an OTG device will not source a significant amount of current into a legacy host device, which can have detrimental effects. Refer to the USB-OTG specification for more details on legacy host detection.

An additional control allows for switching on an additional internal pull down resistor from the VBUS pin to ground to speed up the falling time of VBUS. The pull-down resistor switch is turned on when the VBUS70KPDENB=0 and VBUSEN=0.

The SE0CONN SPI bit allows software to set up the USB transceiver to automatically connect the data pull-up to VUSB any time a SE0 is detected. If a SE0 is detected and SE0CONN=1, then the pull-up is connected (same result as setting USBPU=1) and latched into that state until the SE0CONN bit is cleared (via a SPI write). The reason for this mechanism is to enable the phone to meet the USB-OTG timing requirements without unduly taxing the software. (In one particular USB OTG scenario, a dual-role device is required to connect its pull-up within 1 ms of detecting a SE0.)

A 150 K pull-up resistor to VBUS is provided on the UDP line. This resistor can be used for the accessory type identification when the phone is on. This function is controlled by the DP150KPU bit; when DP150KPU=1, the pull-up resistor is connected to the UDP line. The internal switch for this resistor defaults to a closed state. For proper use the USBPU has to be set to 0.

The ID detector is primarily used to determine if a mini-A or mini-B style plug has been inserted into a mini-AB style receptacle on the phone. However, it is also supports two additional modes which are outside of the USB standards: a so called factory mode and a non USB accessory mode. The state of the ID detection can be read by SPI via the IDFLOATS and IDGNDS sense bits. When one of these bits change state, and IDI interrupt is generated. The interrupt can be masked with the IDM bit. The ID detector is based on an on-chip pull-up controlled by the IDPUCNTRL bit. If set high the pull up is a current source, if set low a resistor. The ID voltage can be read out via the ADC channel ADIN7, see Chapter 9, “ADC Subsystem”. The ID detector thresholds are listed in Table 10-8.

Table 10-8. ID Detection Thresholds

ID Pin External Connection	ID Pin Voltage	IDFLOATS	IDGNDS	Accessory
Resistor to Ground	0.15 * Vatlas < UID < 0.85 * Vatlas	0	0	Non-USB accessory is attached
Grounded	0 < UID < 0.15 * Vatlas	0	1	A type plug is attached indicating a USB-OTG default slave.
Floating	0.85 * Vatlas < UID < 3.0 V	1	0	B type plug is attached indicating a USB Host, a USB-OTG default master, or no device.
Voltage Applied	3.0 V < UID < 3.6 V	1	1	Factory mode

To distinguish different phone accessories, one may opt for a single ended one detection mechanism which is a condition which will not occur within the USB standard devices. The interface on the MC13783 includes a SE1 detector which will set the SE1S bit if a SE1 condition is detected. Any change in SE1S will generate a debounced interrupt SE1I. The interrupt can be masked with the SE1M bit.

Other accessories may be distinguished by the impedance at the ID line. A pull up resistor from the UID pin to VATLAS in parallel to the pull up controlled by IDPUCNTRL can be switched in for this purpose via the ID100KPU bit.

Table 10-9. USB-OTG Specifications

Parameter	Condition	Min	Typ	Max	Units
UDP/UDM pull up resistance	Bus active, RX	1425	—	3090	Ω
UDM/UDP pull up resistance	Bus idle	900	—	1575	Ω
UDP/UDM pull down resistor	—	14.25	19	24.8	kΩ
OTG peripheral input current drain	VBUS and CHRGRAW	—	—	150	uA
Boost to VUSB input switch impedance	—	—	—	25	Ω
VBUS to VUSB-input switch impedance	—	—	—	11	Ω
BP to VUSB-input switch resistance	—	—	—	11	Ω
VBUS to GND pull-down resistance	VBUS70KPDENB = 1 (default)	40	70	100	kΩ
	VBUS70KPDENB = 0, VBUSEN = 0	24	44	64	kΩ
UDP to VATLAS pull up resistance	DP150KPU = 1, USBPU = 0	—	150	—	kΩ
UID pull up	IDPUCNTRL = 0 Resistor to VATLAS	154	220	286	kΩ
	IDPUCNTRL = 1 Current source from VUSB = 3.3 V	4.75	5	5.25	uA
UID parallel pull up	ID100KPU = 1 Resistor to VATLAS	70	100	130	kΩ
SE1 detector input high voltage	UDP = UDM, rising edge	1.8	—	—	V
SE1 detector debounce time	Rising and falling edge	—	1	—	ms

10.1.7 Transceiver Electrical Specification

Table 10-10. General USB Specifications

Parameter	Condition	Min	Typ	Max	Units
Operating Current	FSENB=0	—	13	—	mA
Quiescent Current	—	—	4	—	mA
Suspend Current	Within 1ms of SPI bit write	—	—	500	uA
VBUS Standby Current	VBUS is not driven	—	—	10	uA
Input Low Voltage	UDATVP, USE0VM, UTXENB	—	—	0.8	V
Input High Voltage	UDATVP, USE0VM, UTXENB	USBVCC* 0.7	—	—	V
Input Voltage Range	UDATVP, USE0VM, UTXENB	0	—	USBVCC	V
Output Low Voltage	UDATVP, USE0VM, URCVD (400 uA)	—	—	0.4	V
Output High Voltage	UDATVP, USE0VM, URCVD (400 uA)	USBVCC * 0.9	—	—	V
USBVCC Operating Range	—	1.74	—	3.10	V
Output Low Voltage	UDP, UDM 1.5 KOhm to 3.6 V	—	—	0.3	V

Table 10-10. General USB Specifications (continued)

Parameter	Condition	Min	Typ	Max	Units
Output High Voltage	UDP, UDM 15 KOhm to GND	VUSB*0.9	—	VUSB	V
Output Cross Over Voltage	UDP, UDM	1.3	—	2.0	V
Differential Input Voltage	|(UDP)-(UDM)|	0.2	—	—	V
Common Mode Voltage	UDP, UDM	0.8	—	2.5	V
Single Ended Receive Threshold	UDP, UDM USB Active mode	0.8	—	2.0	V
	UDP, UDM USB Suspend mode	0.5	—	1.2	V
Driver Output Impedance	UDP, UDM, Il=20mA	8.4	14	19.6	Ω

Table 10-11. USB Full Speed Specifications

Parameter	Condition	Min	Typ	Max	Units
Rise and Fall Time	UDP, UDM (CL = 50 pf)	4	—	20	ns
Rise/Fall Time Matching	UDP, UDM	90	—	110	%
Propagation Delay	UDATVP, USE0VM to UDP, UDM	—	—	20	ns
Enable Delay	UTXENB to UDP, UDM	—	—	20	ns
Disable Delay	UTXENB to UDP, UDM	—	—	20	ns
Propagation Delay	UDP, UDM to UDATVP, USE0VM, RCV	—	—	20	ns
Skew between URXVP and URCVD	URXVP rising, URCVD rising URXVP falling, URCVD falling	-4	—	4	ns
Skew between URXVM and URCVD	URXVM falling, URCVD rising URXVM rising, URCVD falling	-4	—	4	ns

Table 10-12. USB Low Speed Specifications

Parameter	Condition	Min	Typ	Max	Units
Rise and Fall Time	UDP, UDM (CL = 350 pf)	75	—	300	ns
Rise/Fall Time Matching	UDP, UDM	80	—	120	%
Propagation Delay	UDATVP, USE0VM to UDP, UDM	—	—	300	ns
Enable Delay	UTXENB to UDP, UDM	—	—	200	ns
Disable Delay	UTXENB to UDP, UDM	—	—	20	ns
Propagation Delay	UDP, UDM to UDATVP, USE0VM, RCV	—	—	30	ns

10.2 RS-232 Interface

In RS232 mode, USBVCC is used for the supply of the interface with the microprocessor. VUSB is used as the supply for the RS232 transceiver and the drivers at the cable side. In this mode, the USB transceiver is tri-stated and the USB module IC pins are re-used to pass the RS232 signals from the radio connector to the digital sections of the radio via the CONMOD[2:0] setting, while the Tx and Rx signals at the cable side can be swapped by setting the RSPOL bit, see Table 10-13.

Table 10-13. RS232 Routing Selection

CONMODE[2:0]	RS232 Routing	
	RSPOL=0 (default)	RSPOL=1
001	Tx signal USE0VM → UDM Rx signal UDP → UDATVP	Tx signal USE0VM →UDP Rx signal UDM → UDATVP
010	Tx signal UDATVP → UDM Rx signal UDP → URXVM	Tx signal UDATVP → UDP Rx signal UDM → URXVM

The Tx line at the cable side is normally active in RS232 mode. By setting the RSTRI bit to a 1 (default is 0) the Tx line will be tristated. Depending on the setting of RSPOL this will occur on UDM or UDP. The receive outputs URXVP and URCVD are tristated in CONMODE[2:0]=001 and 010, while URXVM is only tristated in CONMODE[2:0]=001.

In RS232 mode of operation, circuitry is provided to prevent sneak path conduction of parasitic pn junctions in the tri-stated USB buffers. In RS232 mode the 1.5 K internal USB pull up resistor is automatically disconnected to avoid additional loading on the RS232 drivers.

Table 10-14. RS232 Specifications

Parameter	Condition	Min	Typ	Max	Units
Operating Current	100 kHz, no external loads	—	120	300	uA
Disable current	—	—	—	5	uA
Input Low Voltage	RX input	0	—	0.5	V
Input Low Voltage	TX input	0	—	0.2* USBVCC	V
Input High Voltage	RX input	1.2	—	VBUS	V
Input High Voltage	TX input	0.7* USBVCC	—	USBVCC + 0.3	V
Output Low Voltage	TX output, RX output, 4 mA sink	0	—	0.4	V
Output High Voltage	RX output	0.7* USBVCC	—	USBVCC	V
Output High Voltage	TX output	0.7* VUSB	—	VUSB	V
Rise / Fall Time	RX output, Cload = 30 pf, USBVCC = 2.775 V	—	—	100	ns
Rise / Fall Time	TX output Cload = 100 pf	—	—	100	ns
Rise / Fall Time	TX output Cload = 55 pf	—	—	100	ns
Propagation Delay	All inputs to outputs, Cload = 0 pf	—	—	100	ns

Table 10-14. RS232 Specifications (continued)

Parameter	Condition	Min	Typ	Max	Units
Enable Delay		—	50	100	us
Disable Delay		—	50	100	us
Note: Assume 50 pf loading unless otherwise noted.					

10.3 CEA-936-A Accessory Support

Support for CEA-936-A is provided, including provision for audio muxing to UDP and UDM and ID interrupt generation. Please refer to CEA-936-A specification for details.

Support is provided for mono and stereo audio modes in which audio signals are multiplexed on the USB D+ and D- data lines following the CONMODE[2:0] bit setting. All switches are residing in the USB block and are powered from the VUSB regulator. Figure 10-4 depicts the audio routing.

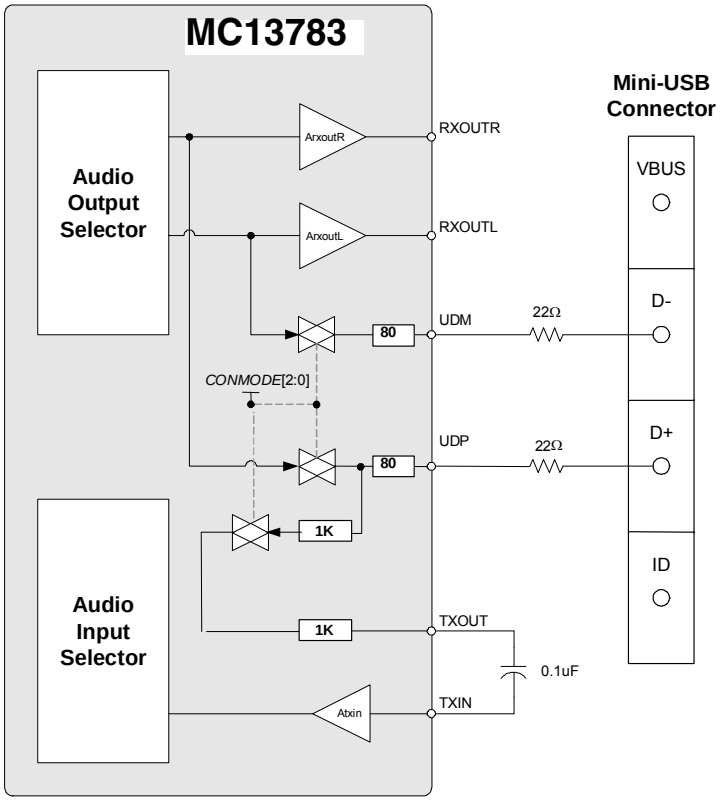


Figure 10-4. CEA-936-A Audio Routing

The audio signals are routed based on the CONMODE[2:0] setting as given in the Table 10-15. The switches driven by CONMODE[2:0] are provided with serial resistors in the audio path to improve EMI robustness. The DC voltage at TXOUT will be equal to the DC voltage at UDP in case of Mono Audio, the coupling cap to TXIN will provide the necessary DC decoupling. The audio circuitry on the MC13783 is capable of supporting the voltage levels which occur during a USB fault condition.

Table 10-15. CEA-936-A Mode Selection

CONMODE[2:0]	CEA-936-A Mode	Routing
100	Mono Audio	MC13783 Receive Audio Left to UDM[1] UDP to TXOUT
101	Stereo Audio	MC13783 Receive Audio Left to UDM[1] MC13783 Receive Audio Right to UDP[1]
110	Test Mode	MC13783 Receive Audio Right to TXOUT USB transceiver enabled
111	Test Mode	MC13783 Receive Audio Left to TXOUT USB transceiver enabled

[1] ARXOUTSEL is used to select the receive source.

The receive outputs URXVP, URXVM and URCVD are tristated in CONMODE[2:0]=100 and 101, while remaining active in CONMODE[2:0]=110 and 111 under the condition that the USB transceiver is not enabled.

Table 10-16. Audio Switches Characteristics

Parameter	Condition	Min	Typ	Max	Units
Impedance	On state, 1 kHz	50	—	150	Ω
	Off state	2	—	—	MΩ
Power Supply Rejection Ratio	Mono Audio, TXOUT and UDM wrt. BP Stereo Audio, UDP and UDM wrt. BP See Linear Regulators chapter for waveforms	80	—	—	dB
Audio Crosstalk	Mono Audio, UDP to UDM and UDM to UDP, 1 kHz Stereo Audio, UDP to UDM, 1kHz	—	—	-66	dB
Audio distortion	1 kHz, 1.4 Vpp at UDP/UDM	—	—	0.1	%
Data to Audio Isolation	USB in Data Mode, Full Speed, Active Receive audio RXOUTR/RXOUTL enabled	—	—	-80	dBV(A)
Audio Input Voltage	Mono Audio, UDP, Input Range	1.0	—	2.9	V
Audio Output Voltage	Mono/Stereo Audio, UDP/UDM, Bias Voltage	—	1.375	—	V
	Mono/Stereo Audio, UDP/UDM, Output Range	0.6	—	2.2	V

The ID Pull-Down resistor and the Carkit Interrupt Detector are provided to allow transitioning between the different signaling modes. While in audio mode, the phone can generate or receive an interrupt requesting a mode change. At the cable side, 5-wire and 4-wire Signaling Negotiation Protocols are supported.

In the 5-wire cable interface protocol, the phone can signal the accessory to exit audio mode by pulling the UID pin to ground momentarily. This is controlled via the IDPD and IDPULSE bits according to Table 10-17.

Table 10-17. CEA-936-A UID Pull Down

IDPD	IDPULSE	UID Pull Down State
0	0	Not pulled down
0	1	Pulled down for 6 ms ± 2 ms IDPULSE bit gets cleared after the pulse has ended
1	X	Pulled down

In the 4-wire cable interface protocol, the phone can signal the accessory to exit audio mode by injecting a positive pulse on the UDM line. This is done by setting the DMPULSE bit to a one. At the end of the pulse this bit is automatically cleared.

The 4-wire cable interface protocol also specifies that when a carkit is in audio signaling mode, it can interrupt the phone by making the UDP line low. This is detected by the Carkit Interrupt Detector implemented on the MC13783. If the output of the Carkit Interrupt Detector goes high, a CKDETI interrupt is generated. The Carkit Interrupt Detector is enabled only in audio signaling mode.

Table 10-18. CEA-936-A Bus Signalling

Parameter	Condition	Min	Typ	Max	Units
UDM Interrupt Pulse Voltage	Generated by MC13783	2.9	—	—	V
UDM Interrupt Pulse Width	Generated by MC13783	200	—	500	ns
UDP Interrupt Pulse Voltage	Received by MC13783	—	—	0.3	V
UDP Interrupt Pulse Width	Received by MC13783	200	—	500	ns

To further facilitate the detection of accessories, the UDP and UDM lines are permanently monitored with a set of comparators. The state of the comparators can be read out via the UDPS and UDMS sense bits. Related mask and interrupt bits are also available. These bits are not valid for USB receive signalling purposes and only intended for static detection. The comparators are active independent of the USB bus activity and CONMODE setting. Only in the test modes these comparators are not active.

10.4 Booting Support

The MC13783 supports booting on USB. The boot mode is entered by the USBEN pin being forced high which enables the USB transceiver and the VUSB regulator supplied from VINBUS. The 1.5 K pull up is connected to UDP and the USB transceiver will operate in the mode as determined by the UMOD0 and UMOD1 pins. To exit the boot mode the USBEN pin can be made low again, or the USBCNTRL bit which at default is at 1 can be set to zero via SPI. Note that in case PUMS2:1=Open:Open, the boost switcher SW3 is off by default, so VINBUS will in that case be equal to BP minus a Schottky diode drop.

10.5 SPI Register Summary

Table 10-19. USB Control Register 0

Name	Bit #	R/W	Default	Description
FSENB	0	R/W	0	0 = USB full speed mode selected 1 = USB low speed mode selected
USBSUSPEND	1	R/W	0	0 = USB Suspend mode disabled 1 = USB Suspend mode enabled
USBPU	2	R/W	0	1 = variable 1.5 K pull-up switched in 0 = variable 1.5 K pull-up switched out
UDPPD	3	R/W	0	0 = 15 K UDP pull-down switched out 1 = 15 K UDP pull-down switched in
UDMPD	4	R/W	0	0 = 15 K UDM pull-down switched out 1 = 15 K UDM pull-down switched in
DP150KPU	5	R/W	1	0 = 150 K UDP pull-up switched out 1 = 150 K UDP pull-up switched in
VBUS70KPDENB	6	R/W	1	0 = VBUS pull-down NMOS switch is ON if VBUSEN = 0, OFF otherwise 1 = VBUS pull-down NMOS switch is OFF
VBUSPULSETMR0	7	R/W	0	VBUS regulator current limit control 000 = current limit set to 200 mA 001 = current limit set to 910 uA for 10 ms 010 = current limit set to 910 uA for 20 ms 011 = current limit set to 910 uA for 30 ms 100 = current limit set to 910 uA for 40 ms 101 = current limit set to 910 uA for 50 ms 110 = current limit set to 910 uA for 60 ms 111 = current limit set to 910 uA The 010 to 110 settings are self clearing at end of timer
VBUSPULSETMR1	8	R/W	0	
VBUSPULSETMR2	9	R/W	0	
DLPSRP	10	R/W	0	0 = DLP Timer disabled 1 = DLP Timer enabled, self clearing at end of pulse
SE0CONN	11	R/W	0	0 = variable UDP pull-up is not automatically connected when SE0 is detected 1 = variable UDP pull-up is automatically connected when SE0 is detected
USBXCVREN	12	R/W	0	0 = USB transceiver disabled if USBEN is low or if USBCNTRL = 0 1 = USB transceiver enabled if CONMODE[2:0] = 000 and RESETB is high
PULLOVR	13	R/W	0	0 = variable 1k5 pull-up and UDP/UDM pull-downs are connected when UTXENB is active low 1 = variable 1k5 pull-up and UDP/UDM pull-downs are disconnected when UTXENB is active low
CONMODE0	14	R/W	0	Connectivity Interface mode select : 000 = USB mode 001 = RS232 mode 1 010 = RS232 mode 2 011 = reserved 100 = mono audio mode 101 = stereo audio mode 110 = Test mode Right mode 111 = Test mode Left mode
CONMODE1	15	R/W	0	
CONMODE2	16	R/W	0	

Table 10-19. USB Control Register 0 (continued)

Name	Bit #	R/W	Default	Description
DATSE0	17	R/W	*	0 = Differential USB mode 1 = Single ended USB mode
BIDIR	18	R/W	*	0 = unidirectional USB transmission 1 = bidirectional USB transmission
USBCNTRL	19	R/W	1	0 = USB mode of operation controlled by SPI 1 = USB mode of operation controlled by USBEN pin
IDPD	20	R/W	0	0 = UID pull-down switched out 1 = UID pull-down switched in
IDPULSE	21	R/W	0	0 = UID line not pulsed 1 = pulse to gnd on the UID line generated This bit is a self clearing bit and will always read back 0
IDPUCNTRL	22	R/W	0	0 = UID pin pulled high through 220 K resistor 1 = UID pin pulled high by 5 uA current source
DMPULSE	23	R/W	0	0 = UDM line not pulsed 1 = A positive pulse on the UDM line is generated. This bit is a self clearing bit and will always read back 0

Table 10-20. USB Control Register 1

Name	Bit #	R/W	Default	Description
VUSBIN0	0	R/W	0	Controls the input source for the VUSB regulator. The default input is BP.
VUSBIN1	1	R/W	1	
VUSB	2	R/W	1	0 = VUSB output voltage set to 3.2 V 1 = VUSB output voltage set to 3.3 V
VUSBEN	3	R/W	0	0 = VUSB output is disabled (unless USBEN pin is asserted high) 1 = VUSB output is enabled (regardless of USBEN pin)
Reserved	4	R/W	0	For future use
VBUSEN	5	R/W	0	0 = VBUS output is disabled (unless VBUSPULSETMR[2:0] <> 0) 1 = VBUS output is enabled (regardless of VBUSPULSETMR[2:0])
RSPOL	6	R/W	0	0 = RS232 TX on UDM, RX on UDP 1 = RS232 TX on UDP, RX on UDM
RSTRI	7	R/W	0	0 = No effect 1 = TX forced to Tristate in RS232 mode only
ID100KPU	8	R/W	0	0 = 100K UID pull up resistor not switched in 1 = 100K UID pull up resistor switched in

Chapter 11
Lighting System

The lighting system of the MC13783 is comprised of independent controlled circuitry for Backlight drivers and Tri-Color LED drivers. This integration provides flexible Backlighting and Fun Lighting for products requiring multi-zone and multi-color product implementations. The core circuitry for Backlights and Fun Lights is enabled with LEDEN=1; disabling through LEDEN=0 will shut down the analog drivers as well as reset all the associated LED timers.

11.1 Backlight Drivers

The Backlight Drivers are generally intended for White LED (WLED) backlighting of color LCD displays or White/Blue LED backlighting for key pads. The drivers consists of independently programmable current sinking channels. SPI registers control programmable features such as DC current level, auto ramping / dimming and PWM settings. Three zones are provided for typical applications which can include backlighting a Main Display, Auxiliary Display, and Key Pad. However, the drivers can be utilized for other lighting schemes such as an integrated WLED flashlight or even non-LED system applications requiring programmable current sinks.

An integrated Boost switcher is provided on the MC13783 (described in the Supplies chapter) for convenient biasing of higher headroom White and/or Blue LEDs. Alternatively, any other available source with sufficient current drive and output voltage for necessary diode headroom may be used (5.5 V must not be exceeded). Figure 11-1, Figure 11-2, and Figure 11-3 illustrate the Backlight Driver zones.

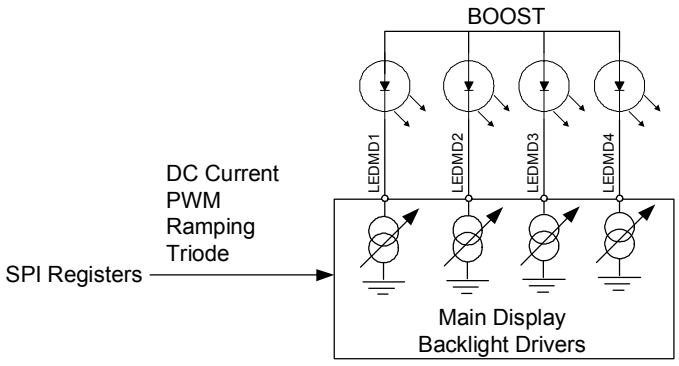


Figure 11-1. Main Display Backlight Driving

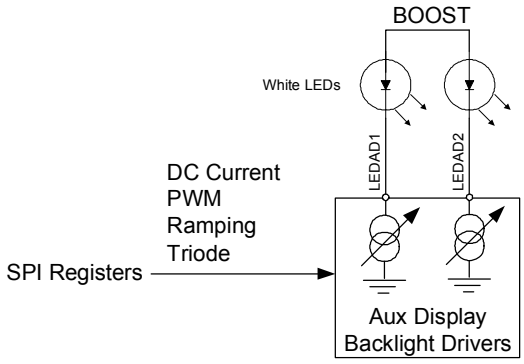


Figure 11-2. Auxiliary Display Backlight Driving

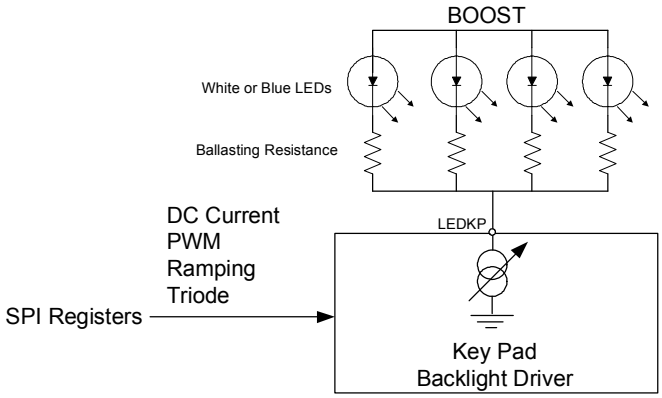


Figure 11-3. Key Pad Backlight Driving

As shown in the preceding figures, the Main and Auxiliary display backlighting allow for individual drivers per WLED to ensure uniformity across a backlighting diffuser screen. Four ganged (master-controlled) driver channels are provided for the Main display (21mA full scale per channel), and 2 ganged channel drivers (21mA full scale per channel) are provided for the Auxiliary display. For the Key Pad driver, current sink capable of driving up to 4 parallel WLEDs is consolidated into a single driver (84mA full scale), since Key Pad uniformity requirements are less stringent than for display backlighting.

The channel currents LEDMDx for the Main Display backlighting are matched current sinks programmed with a master control 3-bit word to allow DC scaling of current from 3 to 21 mA. Four master bits of Duty Cycle settings are used to control perceived brightness or blinking patterns as described below. The duty cycle Period is also programmable for 100 Hz (to avoid visual flickering) and several longer time windows for blinking pattern capability. POR states default to all drivers disabled. Because the drivers are programmable current sinks, LEDs are driven directly without ballasting or current setting resistance.

The two channel Auxiliary Display driver (LEDADx) have the same programmability as the Main Display drivers.

The Key Pad backlighting channel LEDKP is programmable for DC current levels through the SPI by a 3-bit word to allow DC scaling of current for up to 4 WLEDs (84 mA full scale). More LEDs can be used for covering a larger area or improving uniformity as long as the application is within the maximum current capability of the KP driver. Four bits of Duty cycle settings are used to control perceived brightness or blinking patterns as described below. POR states default to the driver disabled. When parallel LEDs are

biased by the LEDKP driver, ballasting resistance may be desirable to improve the uniformity of lighting distribution.

Table 11-1. Backlight Driver Current Sinks

Specification	Conditions	Min	Typ	Max	Units
LED Absolute Current Tolerance	Step 000 through 111, Vdriver = 300 mV	—	0	20	%
LED Current Matching within zones	With respect to the average current in the zone Vdriver = 300 mV	—	—	3	%
LED Channel Off Current	LED Disabled	—	0	1u	uA
Quiescent Consumption	Drivers enabled, PWMs set to 0000, Current levels set to 000	—	100	200	uA
Driver Pin Voltage Range	Drivers enabled or disabled	0	—	5.5	V

11.1.1 Current Level Control

Default behavior for the Backlight Drivers is in Controlled Current Mode, where the drivers are used as programmed current sinks. The maximum programmable channel currents are set to facilitate full scale biasing of single WLEDs on the Main and Auxiliary Display drivers and up to four parallel WLEDs on the Key Pad lighting driver. These bits set the full scale magnitudes for each channel as shown in Table 11-2.

Table 11-2. Backlight Driver Current Control Programming

LEDx2	LEDx1	LEDx0	LEDMDx Level	LEDADx Level	LEDKP Level
0	0	0	0 mA	0 mA	0 mA
0	0	1	3 mA	3 mA	12 mA
0	1	0	6 mA	6 mA	24 mA
0	1	1	9 mA	9 mA	36 mA
1	0	0	12 mA	12 mA	48 mA
1	0	1	15 mA	15 mA	60 mA
1	1	0	18 mA	18 mA	72 mA
1	1	1	21 mA	21 mA	84 mA

11.1.2 Triode Mode

For applications where additional current drive is needed beyond the maximum programmed levels available or the on-chip power dissipation is desired to be reduced, the drivers can be programmed to Triode Mode. The integrated channel drivers behave as a power switch to ground rather than a precision current sink. The resultant current is determined by the rail voltage supplied to the LED divided by intrinsic resistance of the internal switch plus any external ballasting or current setting resistance (if present).

Note that Triode Mode current is a function of the supply voltage applied to LEDs, and so if a controlled current is required, the supply must be kept constant. A current setting resistor can then be used to control the current for a given channel. Alternatively, a driver used in the default Controlled Current Mode (where

the drivers behave as programmed current sinks) can be pushed into Triode Mode for a momentary spike in current. One application example may be to briefly flash the display backlights at maximum power to provide a camera fill-in flash.

PWM control is retained in Triode Mode, so the average current (and therefore the brightness) of the Backlight LEDs can be pulse width controlled for both the Controlled Current Mode and Triode Mode. Reference Figure 11-4 for an application example in Triode Drive Mode.

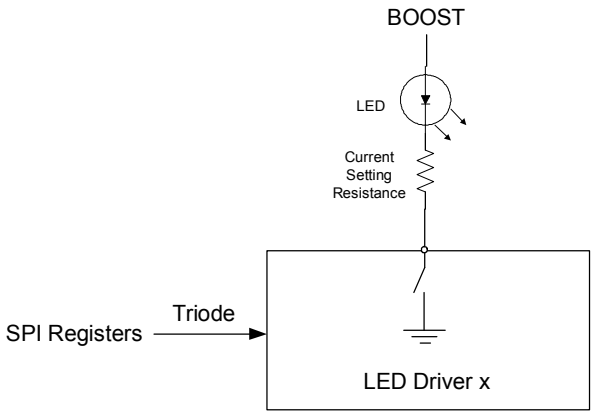


Figure 11-4. Triode Mode Biasing

The Triode Mode of operation overrides the Current Control bits when enabled for a given channel. The default POR state is that Triode Mode is disabled. Caution must be taken to ensure that the DC or pulsed current levels are kept within the safe operating area for LEDs since current is not internally controlled in this mode.

If a product is configured for standard linear control, Triode Mode will draw substantially higher peak current, which will be constrained by the integrated switch and any ballasting resistance that may be used. By keeping the on times and duty cycles fairly low, peak currents may be held within LED reliability guidelines, however, these must be verified by the LED data sheet or with the LED vendor.

This function may be used to drive a visual (non-audible) Alert indication in the product, or for other applications where a brief but very bright strobe display/backlight may be desirable. One application example may be to briefly flash the display backlights at maximum power to provide a camera fill-in flash.

Table 11-3. Triode Mode Characteristics

Specification	Conditions	Min	Typ	Max	Units
Triode Mode On Resistance	LEDMDx	—	10	—	Ohm
	LEDADx	—	10	—	Ohm
	LEDKP	—	2.5	—	Ohm

11.1.3 PWM Control

LED perceived brightness for each zone may be individually set by Duty Cycle control. The default setting for all zones is for 0% duty cycle; this keeps drivers turned off even if they have been programmed on with a non-zero current setting. When the LED drivers are enabled, a 0% duty cycle setting can be used to hold

off any undesired drivers. With the default Period setting over which the Duty Cycle On-Time is applied set to 10 ms, each Backlight zone can be adjusted for non-flickering brightness with an independent 4 bit word for duty cycle. Note that the period over which the duty cycle is applied is also programmable as described in the next section. The on-time pulses for PWM control can be programmed from 0% to 100% in 1 / 15 (approximately 6.7%) steps as shown in Table 11-4.

Table 11-4. Duty Cycle Control

LEDxDC3	LEDxDC2	LEDxDC1	LEDxDC0	Duty Cycle (On-time ratio)
0	0	0	0	0 / 15
0	0	0	1	1 / 15
0	0	1	0	2 / 15
0	0	1	1	3 / 15
0	1	0	0	4 / 15
0	1	0	1	5 / 15
0	1	1	0	6 / 15
0	1	1	1	7 / 15
1	0	0	0	8 / 15
1	0	0	1	9 / 15
1	0	1	0	10 / 15
1	0	1	1	11 / 15
1	1	0	0	12 / 15
1	1	0	1	13 / 15
1	1	1	0	14 / 15
1	1	1	1	15 / 15
Note: x corresponds to MD, AD, or KP zones.				

11.1.4 Period Control

Period is defined as the time for a complete cycle of Time_on + Time_off. The default Period is set to 0.01 seconds such that the 100 Hz on-off cycling is averaged out by the eye to eliminate flickering. Additionally, Period can be programmed to intentionally extend the length of on-off cycles for a visual pulsating or blinking effect. This feature adjusts Period independently of the Duty Cycle and Current Level control, which retain their programmed values to allow for a wide variety of lighting levels and blinking patterns. Refer to Table 11-5 for the Period Control programmability.

NOTE

The Period Control bits are common for all zones of the Backlight drivers.

Table 11-5. Period Control

BLPeriod[1]	BLPeriod[0]	Period (On-time Plus Off-time)
0	0	0.01 seconds
0	1	0.1 seconds
1	0	0.5 seconds
1	1	2 seconds

11.1.5 Pulse Control and Brightness Ramping

The backlight drivers will default to an *Instant On* mode. The three Backlight drivers are staggered by introducing a turn on delay to reduce the inrush current. Additionally, Analog Edge Slowing (not a precision slew rate control) can be enabled through the SLEWLIMBL bit to slow down the transient edges to reduce the chance of coupling LED modulation activity into other circuits. Rise and fall times are nominally targeted for 50us. This is a master control bit that applies analog edge slowing to all Backlight drivers if enabled.

Additionally, the Backlight zones can be individually programmed for an automatic linear ramp from Duty Cycle of 0000 to the programmed Duty Cycle assigned to a given channel, or vice versa with a single SPI write. The transitions will be made in 32 subdivided duty cycle (PWM) steps that are linearly spread over the Ramp Up and Ramp Down cycles. This is intended to give the effect of growing glow or gradual dimming.

The Ramp Up timing spreads the duty cycle steps over a fixed period of 0.5 seconds, terminating at the programmed duty cycle setting. The Ramp Down timing spreads the duty cycle steps from the programmed value to 0 over a fixed period of 0.5 seconds. The RampUp and RampDown modes exit upon the completion of a ramped sequence, and then normal PWM control is re-established. Ramping up and down is applied to all channels of a given Backlight zone simultaneously. Note that the driver may be taken through the ramping sequence in less than 32 steps if the resulting steps are considered so small as to be visually insignificant or beyond the resolution of the PWM generating circuitry. For the ramp to be effective, first the ramp request has to be written by SPI to register 51 and then within 30us the final duty cycle needs to be set to the backlight driver of interest, for instance MD in register 53.

11.1.6 SPI Control for Ramp Modes

Due to the computational requirements of the flexible ramping scheme, special timing considerations must be adhered to for ramp-associated SPI writes. For Ramp Up initiation on any of the Backlight or Tri-Color driver channels, the Ramp Up request must first be issued via SPI (LED Control Register 0 for Backlight drivers, LED Control 1 for TC drivers). This request is latched by the system, which awaits the ending PWM setting so the algorithm can interpolate a smooth PWM sweep. The ending PWM duty cycle that is intended for the ramped driver to settle at after the ramp must be sent with a second SPI write within 30us of the Ramp Up SPI command. The control logic will allow only a single ramp up cycle even if a given channel's RAMPUP bit is not manually cleared. A manual clear must be done if a subsequent ramp cycle is desired.

By way of example, following is a sample SPI sequence to initiate ramping up on the Key Pad driver.

Example for Keypad Backlight Ramp Up; SLEWLIM disabled, ending PWM is 10/15, final KP Current Level is set for 60 mA.

1. Write to Register 51 for Master Enable of the LED drivers (enables core bias circuitry) and the Ramp Up enable on KP: MSB(.....000.100.1)LSB. Note that Ramp Up and Ramp Down bits must not be simultaneously activated.
2. Within 30 us, write to Register 53 to program the ending PWM duty cycle that is desired after completion of the ramp: MSB (0.00.1010. ....101.000.000) LSB. KP is set to ending duty cycle of 10/15; bits related to KP duty rate must remain the same during the ramp-up (500 ms) and after. Current level is set for 60mA.

For Ramp Down initiation on any of the Backlight or Tri-Color driver channels, a given lighting zone will already be programmed to its starting point PWM, so the SPI write to enable the ramp down is all that is needed to initiate the sequence—that is, the algorithm already has the necessary information to calculate the appropriate step sizes since the starting point duty cycle is pre-programmed, and it will ramp down to 0% duty cycle. There are still timing considerations to be respected as indicated in the following example.

Example for Keypad Backlight Ramp Down; Register 53 contains the initial PWM settings: MSB (0.00.1111. ....101.000.000) LSB, SLEWLIM disabled, Starting PWM is 15/15, KP Current Level is set for 60 mA.

1. Write to Register 51 to enable Ramp Down on KP: MSB (.....100.000.1) LSB. KP Ramp Down is requested. Note that Ramp Up and Ramp Down bits must not be simultaneously activated.
2. Wait 100 us to 500 ms; SPI can do other transactions during this period.
3. Write to Register 53 to set ending PWM settings: MSB (0.00.0000. ....000.000.000) LSB.

Bits related to the KP duty rate in Register 53 must remain the same during for ~100us after the Ramp Down command is sent, however, they must be changed to PWM of 0/15 before the Ramp Down is completed (500ms). This assures that the backlight will ramp down and stay off at the end of the ramp.

11.2 Tri-Color LED Drivers

The Tri-Color circuitry provides expanded capability for independent lighting control and distribution that supplements the Backlight Drivers circuitry. The Tri-Color Drivers have the same basic programmability as the described earlier for the Backlight Drivers, with similar bit control for Current Level, Duty Cycle control, and Ramping. A boosted supply such as the on-chip Boost switcher must be used to ensure adequate headroom if necessary, such as for driving Blue LEDs.

The channel naming assignments are R, G, and B representative of applications which use Red, Green, and Blue colored LEDs on each of the respective zones. However, the channels can be used for standard colored, super bright, white, blue, and multi-colored LEDs as desired, an integrated micro-flashlight with one or more White LEDs, or even non-LED applications. A mix of colors assigned to different zones can be used for blending or dynamic morphing of display backlights, case lighting, keyboard backlights, etc.

One set of RGB drivers constitute a Tri-Color Bank, and the MC13783 is presently planned for inclusion of 3 Tri-Color Banks. The TC1 bank is designed for capability to drive up to 42mA full scale on each of its three channels. This may be utilized to drive 2 sets of RGB LEDs in parallel, with ballasting resistance included if needed for current matching. Additionally, the programmed current levels can be rescaled for

driving single LEDs at 21mA full scale per channel with TC1HALF=1 (programmed current levels are detailed further below). The TC2 and TC3 banks are designed for 21mA full scale current on each of their three channels for convenient biasing of single RGB zones.

Drivers may be wired to Red, Green, and Blue LEDs and distributed in products with transparent or translucent housing for enhanced Caller ID discrimination, Fun Light patterns, audio coupled lighting, network status, charger status, mode indicators, gaming lights, RGB Camera Flash, etc.

Each Tri-Color LED driver is programmable for independent control of timing and current levels. Programmable Fun Light patterns may be provided to allow initiation of predefined lighting routines with a single SPI write, reducing the communication burden of running complex lighting sequences. Examples and programmable options are detailed below.

Use care to ensure that the current levels are kept within the safe operating area for LEDs. Ballasting resistors may be desired when using parallel LEDs on a given driver such as with the TC1 channels. Single LEDs driven from any channel do not require ballasting or current setting resistance.

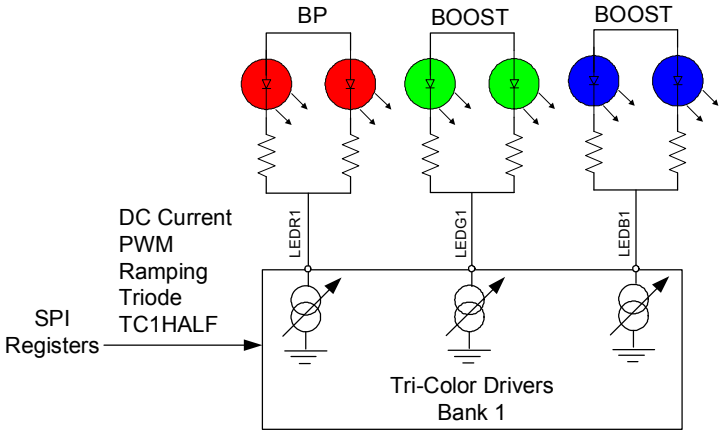


Figure 11-5. Tri-Color Drivers Bank 1

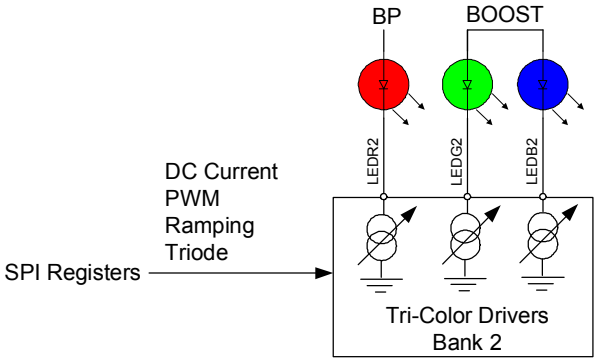


Figure 11-6. Tri-Color Drivers Bank 2

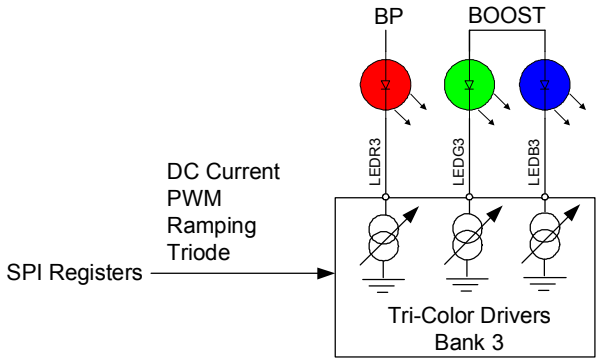


Figure 11-7. Tri-Color Drivers Bank 3

Table 11-6. Tri-Color Driver Current Sinks

Specification	Conditions	Min	Typ	Max	Units
LED Absolute Current Tolerance	Step 00 through 11, Vdriver = 300 mV	—	0	20	%
LED Current Matching within zones	With respect to the average current in the zone Vdriver = 300 mV	—	—	5	%
LED Channel Off Current	LED Disabled	—	0	1	uA
Quiescent Consumption	Drivers enabled, PWMs set to 00000, Current levels set to 00	—	100	200	uA
Driver Pin Voltage Range	Drivers enabled or disabled	0	—	5.5	V

11.2.1 Current Level Control

Each channel of the Tri-Color Drivers has 2 bits of control to set the current levels. The TC1 bank is designed for capability to drive two parallel LEDs with up to 42 mA full scale on each of its three channels, and TC2 and TC3 channels are designed for singled LEDs at 21 mA full scale per channel. Additionally, the TC1 bank has a programmable bit TC1HALF which cuts channel currents by one half when asserted. Nominal current levels for Red, Green, and Blue channels are defined in Table 11-7.

Table 11-7. Tri-Color Driver Current Level Programming

LEDx1	LEDx0	LEDy1 Level TC1HALF=0	LEDy1 Level TC1HALF=1	LEDy2 Level	LEDy3 Level
0	0	12 mA	6 mA	6 mA	6 mA
0	1	18 mA	9 mA	9 mA	9 mA
1	0	30 mA	15 mA	15 mA	15 mA
1	1	42 mA	21 mA	21 mA	21 mA
Note: x corresponds to TC Banks 1, 2, or 3 and R, G, or B channels. y corresponds to R, G, and B channels.					

11.2.2 Triode Mode

Triode mode is supported on the Tri-Color Drivers as described previously for the Backlight Drivers. For applications where additional current drive is needed beyond the maximum programmed levels available or the on-chip power dissipation is desired to be reduced, the drivers can be programmed to Triode Mode. The integrated channel drivers behave as a power switch to ground rather than a precision current sink. The resultant current is determined by the rail voltage supplied to the LED divided by intrinsic resistance of the internal switch plus any external ballasting or current setting resistance (if present).

Note that Triode Mode current is a function of the supply voltage applied to LEDs, and so if a controlled current is required, the supply must be kept constant. A current setting resistor can then be used to control the current for a given channel. Alternatively, a driver used in the default Controlled Current Mode (where the drivers behave as programmed current sinks) can be pushed into Triode Mode for a momentary spike in current. One application example may be to briefly flash the LED drivers at maximum power to provide a camera fill-in flash.

PWM control is retained in Triode Mode, so the average current (and therefore the brightness) of the Tri-Color LEDs can be pulse width controlled for both the Controlled Current Mode and Triode Mode.

The Triode Mode bits override the Current Control bits when enabled for a given channel. The default POR state is that Triode Mode is disabled. Use caution to ensure that the DC or pulsed current levels are kept within the safe operating area for LEDs (verified by the LED data sheet or with the LED vendor) since current is not internally controlled in this mode.

Table 11-8. Triode Mode Characteristics

Specification	Conditions	Min	Typ	Max	Units
Triode Mode On Resistance	LEDy1 with TC1HALF = 0	—	5	—	Ohm
	LEDy1 with TC1HALF = 1	—	10	—	Ohm
	LEDy2	—	10	—	Ohm
	LEDy3	—	10	—	Ohm

11.2.3 PWM Control

As with the Backlight Drivers, the LED perceived brightness for each Tri-Color zone may be set by Duty Cycle independently. The default setting for all zones is for 0% duty cycle; this keeps drivers turned off even after the master enable command. When the LED drivers are enabled, a 0% duty cycle setting is used to hold off any undesired drivers.

Each LED current sink can be turned on and adjusted for brightness with an independent 5 bit word for duty cycle. Note that the period over which the duty cycle is applied is also programmable as described in the next section. The on-time pulses for PWM control can be programmed from 0% to 100% in 1/31 (approximately 3.2%) steps as shown in Table 11-9.

Table 11-9. Tri-Color Duty Cycle Control

LEDxDC4	LEDxDC3	LEDxDC2	LEDxDC1	LEDxDC0	Duty Cycle (% On-time over Period)
0	0	0	0	0	0 / 31
0	0	0	0	1	1 / 31
0	0	0	1	0	2 / 31
0	0	0	1	1	3 / 31
0	0	1	0	0	4 / 31
0	0	1	0	1	5 / 31
0	0	1	1	0	6 / 31
0	0	1	1	1	7 / 31
0	1	0	0	0	8 / 31
0	1	0	0	1	9 / 31
0	1	0	1	0	10 / 31
0	1	0	1	1	11 / 31
0	1	1	0	0	12 / 31
0	1	1	0	1	13 / 31
0	1	1	1	0	14 / 31
0	1	1	1	1	15 / 31
1	0	0	0	0	16 / 31
1	0	0	0	1	17 / 31
1	0	0	1	0	18 / 31
1	0	0	1	1	19 / 31
1	0	1	0	0	20 / 31
1	0	1	0	1	21 / 31
1	0	1	1	0	22 / 31
1	0	1	1	1	23 / 31
1	1	0	0	0	24 / 31
1	1	0	0	1	25 / 31
1	1	0	1	0	26 / 31
1	1	0	1	1	27 / 31
1	1	1	0	0	28 / 31
1	1	1	0	1	29 / 31
1	1	1	1	0	30 / 31
1	1	1	1	1	31 / 31
Note: x corresponds to R, G, B channels of zones TC1-TC3.					

11.2.4 Period Control

Period control is used in conjunction with current magnitude and Duty Cycle to control the perceived brightness and blinking/flashing rates in the same way it is used for the Backlight Driver WLED channels. Period defines the total period of the T_on plus T_off cycle.Period is defined as the time for a complete cycle of Time_on + Time_off. The default Period is set to 0.01 seconds such that the 100 Hz on-off cycling is averaged out by the eye to eliminate flickering. Additionally, Period can be programmed to intentionally extend the length of on-off cycles for a visual pulsating or blinking effect. This feature adjusts Period independently of the Duty Cycle and Current Level control, which retain their programmed values to allow for a wide variety of lighting levels and blinking patterns. Refer to Table 11-10 for the Period Control programmability.

NOTE

The Period control and Duty Cycle settings are applicable to all channels in a given bank, but each bank is independently controlled.

Table 11-10. Tri-Color Period Control

TCx Period[1]	TCx Period[0]	Period (On-time Plus Off-time)
0	0	0.01 seconds
0	1	0.1 seconds
1	0	0.5 seconds
1	1	2 seconds
Note: X = Bank 1, 2, or 3. TC control is applicable to all channels (R, G, & B) in a given bank.		

11.2.5 Pulse Control and Brightness Ramping

The Tri-Color drivers will default to an *Instant On* mode. Analog Edge Slowing (not a precision slew rate control) can be enabled through the SLEWLIMTC bit to slow down the transient edges to reduce the chance of coupling LED modulation activity into other circuits. Rise and fall times are nominally targeted for 100us. This is a master control bit that applies analog edge slowing to all Tri-Color drivers if enabled.

Additionally, the Tri-Color channels can be individually programmed for an automatic linear ramp from Duty Cycle of 00000 to its programmed Duty Cycle, or vice versa via SPI as described in the backlight ramping section earlier in this chapter. The TC ramping transitions will be made in 32 subdivided duty cycle (PWM) steps that are linearly spread over the Ramp Up and Ramp Down cycles. This is intended to give the effect of growing glow or gradual dimming.

The Ramp Up timing spreads the duty cycle steps over a fixed period of 0.5 seconds, terminating at the programmed duty cycle setting. The Ramp Down timing spreads the duty cycle steps from the programmed PWM setting to 0 over a fixed period of 0.5 seconds. The Ramp Up and Ramp Down modes exit upon the completion of a ramped sequence, and then normal PWM control is re-established. Note that the driver may be taken through the ramping sequence in less than 32 steps if the resulting steps are considered so small as to be visually insignificant or beyond the resolution of the PWM generating circuitry.

11.2.6 Fun Light Patterns and Control

A number of programmable Fun Light patterns are included in the State Machine control options accessible through SPI. These are provided in hardware to minimize the SPI and software burden with pre-packaged lighting routines. Complex fun lighting routines can be started or stopped with a single SPI write. Figure 11-8 through Figure 11-12 provide examples and descriptions of Fun Light patterns included in the integrated state machine control circuitry. The selection bits for available Fun Light patterns are summarized in Table 11-11.

Table 11-11. Fun Light Pattern Decoding Map

FLPATTRN[3:0]				Fun Light Pattern	Pattern Description
3	2	1	0		
0	0	0	0	Blended_Ramps_Slow	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Up / Ramp Down cycles with 1 second ramp rates
0	0	0	1	Blended_Ramps_Fast	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Up / Ramp Down cycles with 400 ms ramp rates
0	0	1	0	Saw_Ramps_Slow	Cycles LEDR, LEDG, and LEDB through non-overlapping Ramp Up cycles with 1 second ramp rates
0	0	1	1	Saw_Ramps_Fast	Cycles LEDR, LEDG, and LEDB through non-overlapping Ramp Up cycles with 400 ms ramp rates
0	1	0	0	Blended_Inverse_Ramps_slow	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Down / Ramp Up cycles with 1 second ramp rates
0	1	0	1	Blended_ Inverse Ramps_FAST	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Up / Ramp Down cycles with 400 ms ramp rates
0	1	1	0	Chasing_Lights_RGB_Slow	Cycles each Tri-Color channel in RGB sequence for 500 ms on, 1000 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
0	1	1	1	Chasing_Lights_RGB_Fast	Cycles each Tri-Color channel in RGB sequence for 200 ms on, 400 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
1	0	0	0	Chasing_Lights_BGR_Slow	Cycles each Tri-Color channel in BGR sequence for 500 ms on, 1000 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
1	0	0	1	Chasing_Lights_BGR_Fast	Cycles each Tri-Color channel in BGR sequence for 200 ms on, 400 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
1	0	1	0	Unassigned	—
1	0	1	1	Unassigned	—
1	1	0	0	Unassigned	—
1	1	0	1	Unassigned	—
1	1	1	0	Unassigned	—
1	1	1	1	Unassigned	—

Table 11-12. Fun Light Pattern Bank Enabling

FLBANK[3:1]	Tri-Color Bank
1	1 = Latches selected Fun Light pattern and activates it on Tri-Color Bank 1; 0 = Fun Light pattern in progress is stopped
2	1 = Latches selected Fun Light pattern and activates it on Tri-Color Bank 2; 0 = Fun Light pattern in progress is stopped
3	1 = Latches selected Fun Light pattern and activates it on Tri-Color Bank 3; 0 = Fun Light pattern in progress is stopped

A single decoded Fun Light pattern can be selected at a time with FLPATTRN[3:0]. The pattern may be assigned to Tri-Color Bank 1, 2, and/or 3 by setting the desired FLBANK[3:1] bits high. The programmed Fun Light pattern is latched to any Tri-Color Bank that is activated by setting the corresponding FLBANK bit set high.

The lighting pattern will continue to run on the activated bank(s) until it is stopped by writing 0 to the bank(s) to be de-activated (or if the LED drivers are disabled). Because the Fun Light patterns get latched, Tri-Color banks can be assigned to run different Fun Light patterns simultaneously; however, the pattern selections and bank activations must be done in separate SPI writes. Successive SPI writes to change ramping or Fun Light patterns must be kept a minimum of 100 us apart to allow sufficient setup times for latching.

Because the Fun Light pattern assignments are latched, the pattern on a Tri-Color bank will not be changed until any pattern in progress is stopped by writing 0 to the corresponding FLBANK activation bit.

Fun Light Patterns are illustrated in the Figure 11-8 through Figure 11-12 which show waveforms driven on each channel of the Tri-Color Drivers. Magnitudes represent relative brightness levels implemented by PWM control with internal state machine logic. When multi-colored LEDs (such as RGB) are used on the Tri-Color channels and injected into diffuser screens or translucent product casing, a mixing of the colors may be effected such that the result is a dynamic blending that cycles through various mixed tones.

As an example, consider the Blended Ramps pattern is illustrated below. It starts off as ramping down Blue while ramping up Red. Initially, this will appear as pure Blue, which is reduced in intensity (through PWM sweeping) while the Red content is increased in intensity, till it is purely Red. A continuous blend of colors are realized through the dynamic ramping of the color channels, which will sweep through Blue, Violet, Magenta, Deep Pink, and finally Red-all this in the first ramped sequence.

This is followed by ramping down Red and Ramping up Green. This mix turns the resultant color from Red to Green with all the mixed variants in between. The progressive mixing of colors will blend from Red to Orange to Yellow, Yellow Green, and ultimately Green when Red is completely off and Green is completely on. The next cycle starts phasing in the Blue channel, which will progressively transition the mix from Green to Light Green, Cyan, Light Blue, and Blue. The next sequence will once again ramp down Blue as Red ramps up, resulting in color mixes for Violet, Magenta, Deep Pink, and ultimately back to Red. In this fashion, the Fun Light pattern essentially cycles through the colors of the rainbow. Similar assessments can be made for the other Fun Light patterns or manual color mixing through SPI programming of Tri-Color channels.

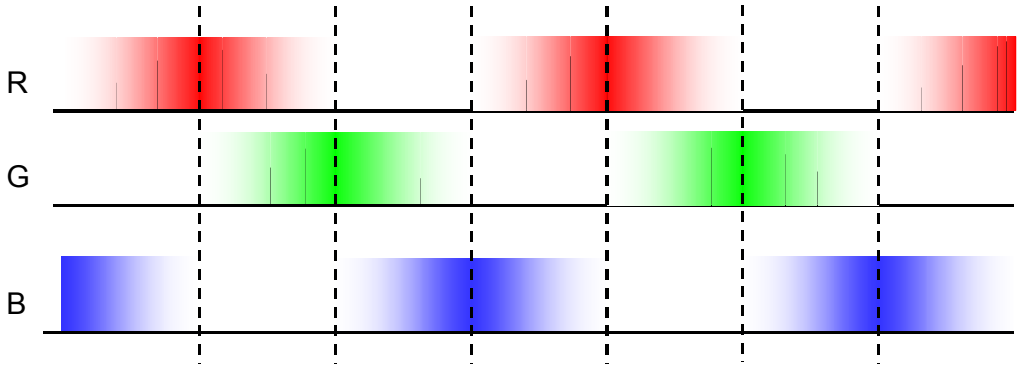


Figure 11-8. Blended Ramps Fun Light Pattern

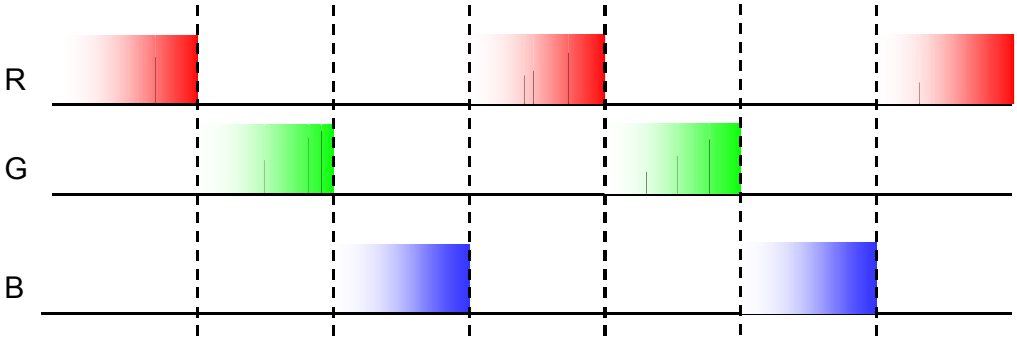


Figure 11-9. Saw Tooth Ramps Fun Light Pattern

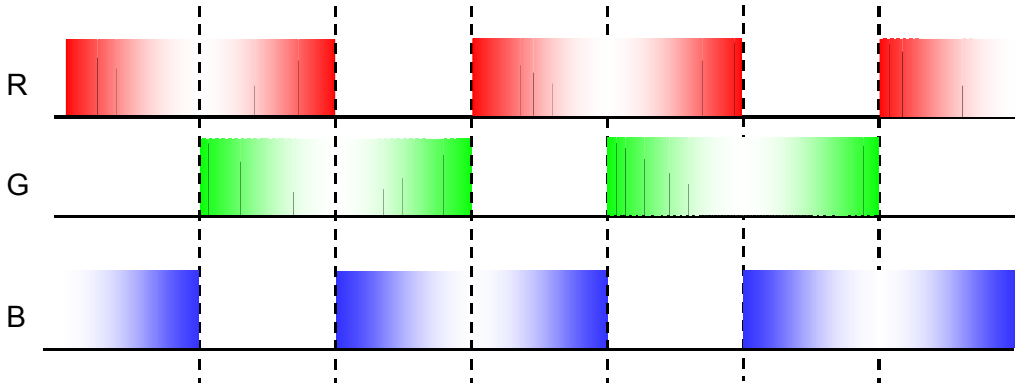


Figure 11-10. Blended Inverse Ramps Fun Light Pattern

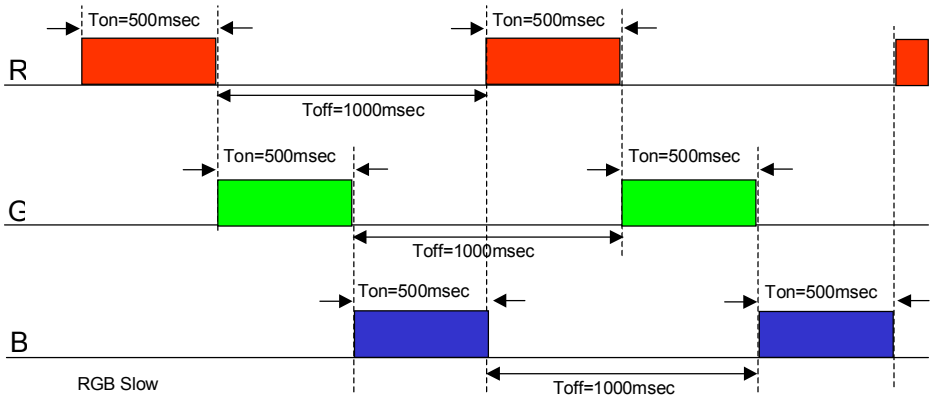


Figure 11-11. Chasing Lights Fun Light Pattern

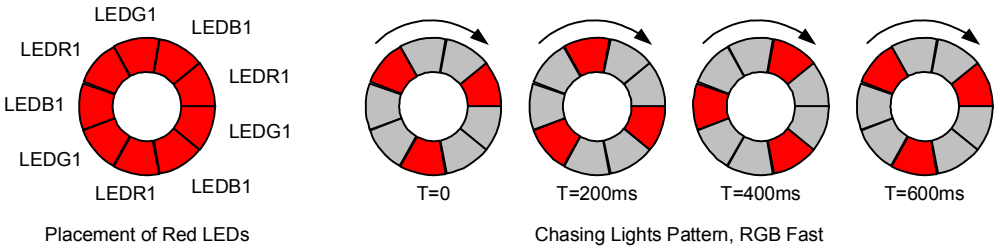


Figure 11-12. Chasing Lights Fun Light Pattern Generation

11.2.7 SPI Control for Fun Light Patterns

As noted, the data latching process that stores active Fun Light pattern selections require special SPI timing considerations. Following is an example with illustrative SPI communication for Fun Light pattern selections.

Example for Fun Light pattern selections; applicable PWM settings are implied but not included below.

1. Write to Register 51 to select desired Fun Light pattern and bank(s). MSB(101.0000.....1)LSB. For this example, assume that Blended Ramps Slow will be applied to TC1 and TC3.
2. Wait ~100 us (or more) to allow for latching of the Fun Light bits.
3. Write to Register 51 to initiate a new Fun Light pattern (Saw Ramps Fast) on TC2 while leaving Blended Ramps Slow running on TC1 and TC3: MSB(111.0011.....1)LSB. Since TC1 and TC3 FLBANK selection bits have not gone to 0, they will continue to run the Fun Light pattern assigned in Step 1. The FLBANK2 bit has gone to a 1 state, so TC2 will activate with the pattern decoded from FLPATTRN[3:0], which is Saw Ramps Fast.
4. Wait ~100 us before modifying Register 51 again to allow for data latching (SPI can do other transactions during this wait). Assuming that the patterns are left to run for several seconds.
5. Wait.
6. Write to Register 51 to deselect applicable bank(s) MSB(000.0000.....1)LSB

This turns off Fun Light Patterns on all TC banks and all Fun Light patterns are stopped, and TC1 - TC3 will revert back to any PWM programmed states that are held in the registers.

11.3 Adaptive Boost

The on-chip Boost switcher may be used to source LED current with the required headroom for White LEDs. An Adaptive Boost (AB) mode of operation is provided to scale the Boost output voltage to the minimum necessary so that power dissipation across the current sinking Main Display Backlight drivers is reduced. This improves overall power efficiency for use cases where the Backlights are active for extended periods.

The AB Switcher system is illustrated in Figure 11-13 showing monitoring one channel of the main display driver LEDMD1.

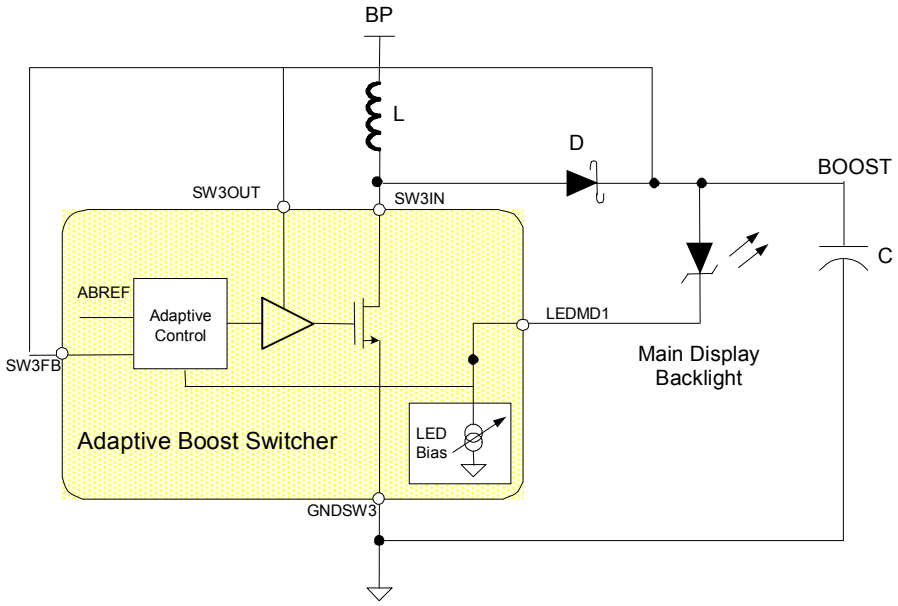


Figure 11-13. Adaptive Boost Switcher Supply Arrangement

The Backlight LED drivers require finite headroom to work with, and a trade off may be made between current accuracy and matching across channels against the voltage headroom across the drivers—that is, the voltage at LEDMDx. A lower voltage on the drivers reduces internal power dissipation and hence is more power efficient. However, reducing the voltage at LED driver inputs also pushes the current sinking transistors deeper into triode operation, where programmed current accuracy and matching characteristics degrade.

The forward drop across the White LEDs will be a nonlinear function of current, and for typical lighting applications, can vary from approximately 2.5 V to 4 V. Thus, the Boost level may be modulated up or down, depending on the forward drop needed to support proper LED lighting, and the desired minimum headroom preserved for the current sinking drivers.

When the AB is activated by programming ABMODE[2:0]=001 and BOOSTEN=1, the system will set the output voltage of the Boost switcher to an initial setting of ABMAX. The system will then monitor the LEDMD1 driver voltage and compare it to the user defined set point voltage as defined by the ABREF[1:0] setting. If the comparator detects that the LED driver voltage is above the programmed value, the AB system will reduce the output voltage of the Boost switcher in steps of ABSTEP until the monitored driver channel has fallen below the programmed voltage level, or until the Boost lower limit of ABMIN has been

reached. The system uses a comparator control scheme with hysteresis to hold the Boost voltage to the proper value for the targeted window of operation. Because the AB switcher is a Boost-only converter, at very low output settings the output voltage will track the battery minus a forward Schottky diode drop.

The AB system includes a channel scanning circuit that can be programmed to take into account multiple channels of LED drivers so that any slight variances in the forward drops across LEDs can be factored in. When multiple channels are included in the AB scan sequence, the system will adapt the Boost voltage to the channel that is found to have the lowest driver voltage in the group. The channel selections for scan sequencing is programmed with the ABMODE[2:0] bits.

The AB may be used in PWM mode or in continuous current mode, where the continuous current mode can actually be considered as a 100% active PWM mode. The LED driver is scanned by the AB at the beginning of each PWM period and after a delay of approximately 180us after the activation of an active pulse. This delay is short enough to cover the shortest PWM period and at the same time ensures the LED driver has reached a stable state. The system will not attempt a measurement when the assigned channel is deactivated—that is,, between pulses in LED PWM mode. To avoid rail pertubation of LED brightness, software must not activate the AB while the main display drivers are programmed in Triode Mode or while they are ramping up or down. Also, when using AB on both LEDMD and LEDAD, it is expected that both banks are operated at the same duty cycle.

Since the Boost switcher is directly or indirectly used to supply other backlights and peripherals like the USB transceiver, the AB mode cannot be activated in all modes. To avoid malfunctioning of these peripherals, the AB is automatically disabled under the following conditions:

- When the AB mode is disabled (ABMODE[2:0]=000)
- When the Boost Switcher forced enable bit is not set (BOOSTEN=0)
- When the Aux Display driver is enabled while not in mode ABMODE[2:0]=101 or 110 or 111
- When the Aux Display driver is not enabled while in mode ABMODE[2:0]=101 or 110 or 111
- When one of the other LED drivers is enabled (Keypad, Tricolor)
- When a USB session is activated (VUSBEN=1 or VBUSEN=1)

If the AB is forced to disable by an event other than explicitly turning it off, the Boost Switcher will smoothly resume its normal operating mode as determined by the SW3 settings in register 29 and will return back to AB operation again when possible. Note that if BOOSTEN=1, the boost switcher is forced to be in active mode which will overrule the operating mode as given by register 29.

Table 11-13 summarize the behavior and control of the Adaptive Boost circuitry.

Table 11-13. Adaptive Boost Mode Selection Bits

ABMODE[2:0]	Function
000	Adaptive Boost Disabled
001	Monitor Channel LEDMD1
010	Monitor Channels LEDMD1, 2
011	Monitor Channels LEDMD1, 2, 3
100	Monitor Channels LEDMD1, 2, 3, 4

Table 11-13. Adaptive Boost Mode Selection Bits (continued)

ABMODE[2:0]	Function
101	Monitor Channels LEDMD1, 2, 3, 4 and LEDAD1
110	Monitor Channels LEDMD1, 2, 3, 4 and LEDAD1, 2
111	Monitor Channel LEDMD1 with LEDAD active

Table 11-14. Adaptive Boost Headroom Programming

ABREF[1:0]	Function
00	ABREF = 200 mV
01	ABREF = 400 mV
10	ABREF = 600 mV
11	ABREF = 800 mV

Table 11-15. Adaptive Boost Characteristics

Parameter	Condition	Min	Typ	Max	Units
ABREF	3.0 V < Vin < Vout - 0.3 V < 5 V 0 < IL < Ilmax				
	ABREF[1:0] = 00[1]	166	216	266	mV
	ABREF[1:0] = 01	358	408	458	mV
	ABREF[1:0] = 10	550	600	650	mV
	ABREF[1:0] = 11	742	792	842	mV
Boost Regulator Vout	3.0 V < Vin < Vout - 0.3 V < 5 V 0 < IL < Ilmax Adapt Enabled				
ABMAX	Maximum Setting in Adaptive Boost Mode	-5%	4.875	+5%	V
ABMIN	Minimum Setting in Adaptive Boost Mode	-5%	3.300	+5%	V
ABSTEP	Adaptive Boost Voltage Step Size	-0.5%	75	+0.5%	mV

[1] The lowest setting ABREF[1:0]=00 does not guarantee full performance of the LED drivers. Setting ABREF[1:0]=01 is advised as the minimum setting.

11.4 SPI Register Summary

Table 11-16. Register 51, LED Control 0

Name	Bit #	R/W	Reset	Default	Description
LEDEN	0	R/W	RESETB	0	Master Enable for BL and TC LED Bias
LEDMDRAMPUP	1	R/W	RESETB	0	Ramp Up Main Display Backlight channel
LEDADRAMPUP	2	R/W	RESETB	0	Ramp Up Auxiliary Display Backlight channel
LEDKPRAMPUP	3	R/W	RESETB	0	Ramp Up Key Pad Backlight channel
LEDMDRAMPDOWN	4	R/W	RESETB	0	Ramp Down Main Display Backlight channel
LEDADRAMPDOWN	5	R/W	RESETB	0	Ramp Down Auxiliary Display Backlight channel
LEDKPRAMPDOWN	6	R/W	RESETB	0	Ramp Down Key Pad Backlight channel
TRIODEMD	7	R/W	RESETB	0	Triode Mode for Main Display Backlight Drivers
TRIODEAD	8	R/W	RESETB	0	Triode Mode for Auxiliary Display Backlight Drivers
TRIODEKP	9	R/W	RESETB	0	Triode Mode for Key Pad Backlight Driver
BOOSTEN	10	R/W	RESETB	0	Forced enable for Boost
ABMODE0	11	R/W	RESETB	0	Adaptive Boost Mode Selection Bits
ABMODE1	12	R/W	RESETB	0	
ABMODE2	13	R/W	RESETB	0	
ABREF0	14	R/W	RESETB	0	Adaptive Boost reference level to set driver headroom voltage
ABREF1	15	R/W	RESETB	0	
Reserved	16	R/W	RESETB	0	Reserved for future use by the adaptive boost
FLPATTRN0	17	R/W	RESETB	0	Fun Light Pattern Selection Bits
FLPATTRN1	18	R/W	RESETB	0	
FLPATTRN2	19	R/W	RESETB	0	
FLPATTRN3	20	R/W	RESETB	0	
FLBANK1	21	R/W	RESETB	0	Tri-Color Bank 1 activation for Fun Light pattern
FLBANK2	22	R/W	RESETB	0	Tri-Color Bank 2 activation for Fun Light pattern
FLBANK3	23	R/W	RESETB	0	Tri-Color Bank 3 activation for Fun Light pattern

Table 11-17. Register 52, LED Control 1

Name	Bit #	R/W	Reset	Default	Description
LEDR1RAMPUP	0	R/W	RESETB	0	Ramp Up Tri-Color 1 Red channel
LEDG1RAMPUP	1	R/W	RESETB	0	Ramp Up Tri-Color 1 Green channel
LEDB1RAMPUP	2	R/W	RESETB	0	Ramp Up Tri-Color 1 Blue channel
LEDR1RAMPDOWN	3	R/W	RESETB	0	Ramp Down Tri-Color 1 Red channel
LEDG1RAMPDOWN	4	R/W	RESETB	0	Ramp Down Tri-Color 1 Green channel

Table 11-17. Register 52, LED Control 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
LEDB1RAMPDOWN	5	R/W	RESETB	0	Ramp Down Tri-Color 1 Blue channel
LEDR2RAMPUP	6	R/W	RESETB	0	Ramp Up Tri-Color 2 Red channel
LEDG2RAMPUP	7	R/W	RESETB	0	Ramp Up Tri-Color 2 Green channel
LEDB2RAMPUP	8	R/W	RESETB	0	Ramp Up Tri-Color 2 Blue channel
LEDR2RAMPDOWN	9	R/W	RESETB	0	Ramp Down Tri-Color 2 Red channel
LEDG2RAMPDOWN	10	R/W	RESETB	0	Ramp Down Tri-Color 2 Green channel
LEDB2RAMPDOWN	11	R/W	RESETB	0	Ramp Down Tri-Color 2 Blue channel
LEDR3RAMPUP	12	R/W	RESETB	0	Ramp Up Tri-Color 3 Red channel
LEDG3RAMPUP	13	R/W	RESETB	0	Ramp Up Tri-Color 3 Green channel
LEDB3RAMPUP	14	R/W	RESETB	0	Ramp Up Tri-Color 3 Blue channel
LEDR3RAMPDOWN	15	R/W	RESETB	0	Ramp Down Tri-Color 3 Red channel
LEDG3RAMPDOWN	16	R/W	RESETB	0	Ramp Down Tri-Color 3 Green channel
LEDB3RAMPDOWN	17	R/W	RESETB	0	Ramp Down Tri-Color 3 Blue channel
TC1HALF	18	R/W	RESETB	0	Half Current Mode for Tri-Color 1 Driver channels
Reserved	19	R/W	RESETB	0	Reserved
Reserved	20	R/W	RESETB	0	Reserved
Reserved	21	R/W	RESETB	0	Reserved
Reserved	22	R/W	RESETB	0	Reserved
SLEWLIMTC	23	R/W	RESETB	0	Master Enable for Tri-Color Analog Edge Slowing

Table 11-18. Register 53, LED Control 2

Name	Bit #	R/W	Reset	Default	Description
LEDMD0	0	R/W	RESETB	0	Current Level Programming for the Main Display Backlight Driver
LEDMD1	1	R/W	RESETB	0	
LEDMD2	2	R/W	RESETB	0	
LEDAD0	3	R/W	RESETB	0	Current Level Programming for the Auxiliary Display Backlight Driver
LEDAD1	4	R/W	RESETB	0	
LEDAD2	5	R/W	RESETB	0	
LEDKP0	6	R/W	RESETB	0	Current Level Programming for the Keypad Backlight Driver
LEDKP1	7	R/W	RESETB	0	
LEDKP2	8	R/W	RESETB	0	

Table 11-18. Register 53, LED Control 2 (continued)

Name	Bit #	R/W	Reset	Default	Description
LEDMDDC0	9	R/W	RESETB	0	Duty Cycle Control for the Main Display Backlight Driver
LEDMDDC1	10	R/W	RESETB	0	
LEDMDDC2	11	R/W	RESETB	0	
LEDMDDC3	12	R/W	RESETB	0	
LEDADDC0	13	R/W	RESETB	0	Duty Cycle Control for the Auxiliary Display Backlight Driver
LEDADDC1	14	R/W	RESETB	0	
LEDADDC2	15	R/W	RESETB	0	
LEDADDC3	16	R/W	RESETB	0	
LEDKPDC0	17	R/W	RESETB	0	Duty Cycle Control for the Keypad Backlight Driver
LEDKPDC1	18	R/W	RESETB	0	
LEDKPDC2	19	R/W	RESETB	0	
LEDKPDC3	20	R/W	RESETB	0	
BLPERIOD0	21	R/W	RESETB	0	Period Control for Backlight
BLPERIOD1	22	R/W	RESETB	0	
SLEWLIMBL	23	R/W	RESETB	0	Master Enable for Backlight Analog Edge Slowing

Table 11-19. Register 54, LED Control 3

Name	Bit #	R/W	Reset	Default	Description
LEDR10	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 1
LEDR11	1	R/W	RESETB	0	
LEDG10	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 1
LEDG11	3	R/W	RESETB	0	
LEDB10	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 1
LEDB11	5	R/W	RESETB	0	
LEDR1DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 1
LEDR1DC1	7	R/W	RESETB	0	
LEDR1DC2	8	R/W	RESETB	0	
LEDR1DC3	9	R/W	RESETB	0	
LEDR1DC4	10	R/W	RESETB	0	

Table 11-19. Register 54, LED Control 3 (continued)

Name	Bit #	R/W	Reset	Default	Description
LEDG1DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 1
LEDG1DC1	12	R/W	RESETB	0	
LEDG1DC2	13	R/W	RESETB	0	
LEDG1DC3	14	R/W	RESETB	0	
LEDG1DC4	15	R/W	RESETB	0	
LEDB1DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 1
LEDB1DC1	17	R/W	RESETB	0	
LEDB1DC2	18	R/W	RESETB	0	
LEDB1DC3	19	R/W	RESETB	0	
LEDB1DC4	20	R/W	RESETB	0	
TC1PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 1
TC1PERIOD1	22	R/W	RESETB	0	
TC1TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 1 Channels

Table 11-20. Register 55, LED Control 4

Name	Bit #	R/W	Reset	Default	Description
LEDR20	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 2
LEDR21	1	R/W	RESETB	0	
LEDG20	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 2
LEDG21	3	R/W	RESETB	0	
LEDB20	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 2
LEDB21	5	R/W	RESETB	0	
LEDR2DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 2
LEDR2DC1	7	R/W	RESETB	0	
LEDR2DC2	8	R/W	RESETB	0	
LEDR2DC3	9	R/W	RESETB	0	
LEDR2DC4	10	R/W	RESETB	0	
LEDG2DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 2
LEDG2DC1	12	R/W	RESETB	0	
LEDG2DC2	13	R/W	RESETB	0	
LEDG2DC3	14	R/W	RESETB	0	
LEDG2DC4	15	R/W	RESETB	0	

Table 11-20. Register 55, LED Control 4 (continued)

Name	Bit #	R/W	Reset	Default	Description
LEDB2DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 2
LEDB2DC1	17	R/W	RESETB	0	
LEDB2DC2	18	R/W	RESETB	0	
LEDB2DC3	19	R/W	RESETB	0	
LEDB2DC4	20	R/W	RESETB	0	
TC2PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 2
TC2PERIOD1	22	R/W	RESETB	0	
TC2TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 2 Channels

Table 11-21. Register 56, LED Control 5

Name	Bit #	R/W	Reset	Default	Description
LEDR30	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 3
LEDR31	1	R/W	RESETB	0	
LEDG30	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 3
LEDG31	3	R/W	RESETB	0	
LEDB30	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 3
LEDB31	5	R/W	RESETB	0	
LEDR3DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 3
LEDR3DC1	7	R/W	RESETB	0	
LEDR3DC2	8	R/W	RESETB	0	
LEDR3DC3	9	R/W	RESETB	0	
LEDR3DC4	10	R/W	RESETB	0	
LEDG3DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 3
LEDG3DC1	12	R/W	RESETB	0	
LEDG3DC2	13	R/W	RESETB	0	
LEDG3DC3	14	R/W	RESETB	0	
LEDG3DC4	15	R/W	RESETB	0	
LEDB3DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 3
LEDB3DC1	17	R/W	RESETB	0	
LEDB3DC2	18	R/W	RESETB	0	
LEDB3DC3	19	R/W	RESETB	0	
LEDB3DC4	20	R/W	RESETB	0	

Table 11-21. Register 56, LED Control 5 (continued)

Name	Bit #	R/W	Reset	Default	Description
TC3PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 3
TC3PERIOD1	22	R/W	RESETB	0	
TC3TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 3 Channels

Chapter 12
Pinout and Package

12.1 Package Drawing and Marking

The package style is a low profile BGA, pitch 0.5 mm, body 10 x 10 mm, semi populated 19 x 19 matrix, ball count 247 including 4 sets of triple corner balls and 4 spare balls.

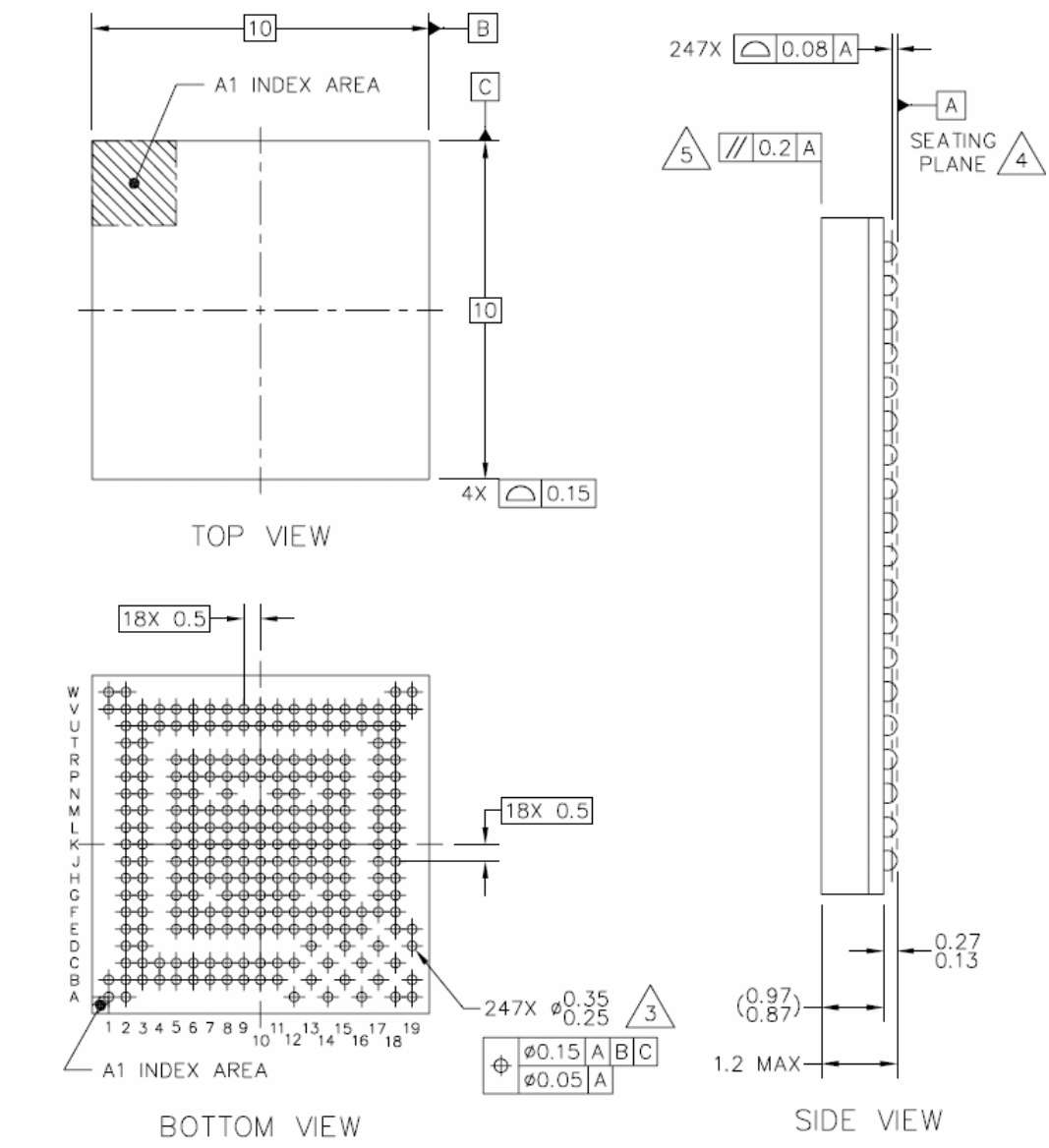


Figure 12-1. Package Outline

The package marking follows the depicted scheme in Table 12-1.

Table 12-1. Package Marking

Line 1	Freescale Logo	
Line 2	Part Number	MC13783VK, MC13783VK4, MC13783VK5, or MC13783JVK5
Line 3	Mask ID	MMMMM
Line 4	Trace/Date Code	AWLYYWW (WLYYWW for MC13783VK4)
Line 5	Country Code	CCCCC

12.2 Pinout Description

Table 12-2 is the pinout description and gives the pin name per functional block with its row-column coordinates, its max voltage rating and a functional description. The max voltage rating is given per category of pins: EHV for Extended High Voltage (20 V), HV for High Voltage (7.5 V), EMV for Extended Medium Voltage (5.5 V), MV for Medium Voltage (4.65 V) and LV for Low Voltage (3.1 V).

Table 12-2. Pinout Listing

Pin	Location	Rating	Function
Charger			
CHRGRAW	A18 A19 B19	EHV	1. Charger input 2. Output to battery supplied accessories
CHRGCTRL	C18	EHV	Driver output for charger path FETs M1 and M2
BPFET	B15	EHV	1. Driver output for dual path regulated BP FET M4 2. Driver output for separate USB charger path FETs M5 and M6
CHRGISNSP	B17	MV	Charge current sensing point 1
CHRGISNSN	C14	MV	Charge current sensing point 2
BP	B13	MV	1. Application supply point 2. Input supply to the MC13783 core circuitry 3. Application supply voltage sense
BATTFET	A12	MV	Driver output for battery path FET M3
BATTISNS	A14	MV	Battery current sensing point 1
BATT	D15	MV	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
CHRGMOD0	D17	LV	Selection of the mode of charging
CHRGMOD1	A16	LV	Selection of the mode of charging
CHRGSE1B	F15	LV	Charger forced SE1 detection input
CHRGLED	D13	EHV	Trickle LED driver output

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
GNDCHRG	J11	—	Ground for charger interface
LED Drivers			
LEDMD1	B8	EMV	Main display backlight LED driver output 1
LEDMD2	F9	EMV	Main display backlight LED driver output 2
LEDMD3	E9	EMV	Main display backlight LED driver output 3
LEDMD4	C9	EMV	Main display backlight LED driver output 4
LEDAD1	C8	EMV	Auxiliary display backlight LED driver output 1
LEDAD2	E8	EMV	Auxiliary display backlight LED driver output 2
LEDKP	C7	EMV	Keypad lighting LED driver output
LEDR1	B10	EMV	Tricolor red LED driver output 1
LEDG1	E11	EMV	Tricolor green LED driver output 1
LEDB1	F11	EMV	Tricolor blue LED driver output 1
LEDR2	E10	EMV	Tricolor red LED driver output 2
LEDG2	F10	EMV	Tricolor green LED driver output 2
LEDB2	G10	EMV	Tricolor blue LED driver output 2
LEDR3	F8	EMV	Tricolor red LED driver output 3
LEDG3	C10	EMV	Tricolor green LED driver output 3
LEDB3	B9	EMV	Tricolor blue LED driver output 3
GNDLEDBL	H10	—	Ground for backlight LED drivers
GNDLEDTC	J10	—	Ground for tricolor LED drivers
MC13783 Core			
VATLAS	C12	LV	Regulated supply output for the MC13783 core circuitry
REFATLAS	B11	LV	Main bandgap reference
GNDATLAS	H11	—	Ground for the MC13783 core circuitry
Switchers			
SW1AIN	K18	MV	Switcher 1A input
SW1AOUT	K17	MV	Switcher 1A output
SW1AFB	L18	LV	Switcher 1A feedback
DVSSW1A	J15	LV	Dynamic voltage scaling logic input for switcher 1A
GNDSW1A	L17	—	Ground for switcher 1A
SW1BIN	N18	MV	Switcher 1B input
SW1BOUT	N17	MV	Switcher 1B output
SW1BFB	M18	LV	Switcher 1B feedback

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
SW1ABSPB	P11	LV	Switcher 1A 1B separate parallel operating mode selection
DVSSW1B	K15	LV	Dynamic voltage scaling logic input for switcher 1B
GNDSW1B	M17	—	Ground for switcher 1B
SW2AIN	P18	MV	Switcher 2A input
SW2AOUT	R18	MV	Switcher 2A output
SW2AFB	P15	LV	Switcher 2A feedback
DVSSW2A	H15	LV	Dynamic voltage scaling logic input for switcher 2A
GNDSW2A	P17	—	Ground for switcher 2A
SW2BIN	U18	MV	Switcher 2B input
SW2BOUT	T18	MV	Switcher 2B output
SW2BFB	R17	LV	Switcher 2B feedback
SW2ABSPB	R12	LV	Switcher 2A 2B separate parallel operating mode selection
DVSSW2B	J14	LV	Dynamic voltage scaling logic input for switcher 2B
GNDSW2B	T17	—	Ground for switcher 2B
SW3IN	J17	MV	Switcher 3 input
SW3OUT	H18	HV	Switcher 3 output
SW3FB	H17	HV	Switcher 3 feedback
GNDSW3	J18	—	Ground for switcher 3
Power Gating			
PWGT1EN	L14	LV	Power gate driver 1 enable
PWGT1DRV	M15	EMV	Power gate driver 1 output
PWGT2EN	L15	LV	Power gate driver 2 enable
PWGT2DRV	K14	EMV	Power gate driver 2 output
Regulators			
VINAUDIO	U12	MV	Input regulator audio
VAUDIO	U10	LV	Output regulator audio
VINIOLO	U13	MV	Input regulator low voltage I/O
VIOLO	V13	LV	Output regulator low voltage I/O
VINIOHI	B7	MV	Input regulator high voltage I/O
VIOHI	B6	LV	Output regulator high voltage I/O
VINDIG	R11	MV	Input regulator general digital
VDIG	U11	LV	Output regulator general digital
VINRFDIG	K5	MV	Input regulator transceiver digital

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
VRFDIG	K2	LV	Output regulator transceiver digital
VINRFREF	K7	MV	Input regulator transceiver reference
VRFREF	G3	LV	Output regulator transceiver reference
VRFCP	G2	LV	Output regulator transceiver charge pump
VRFBG	C11	LV	Bandgap reference output for transceiver
VINSIM	F2	MV	Input regulator SIM card and eSIM card
VSIM	E3	LV	Output regulator SIM card
VESIM	F3	LV	Output regulator eSIM card
VINVIB	G5	MV	Input regulator vibrator motor
VVIB	E2	LV	Output regulator vibrator motor
VINGEN	G17	MV	Input regulator graphics accelerator
VGEN	G18	LV	Output regulator graphics accelerator
VINCAM	V12	MV	Input regulator camera
VCAM	V11	LV	Output regulator camera
VRF2DRV	J6	MV	Drive output regulator transceiver
VRF2	J5	LV	Output regulator transceiver
VRF1DRV	K8	MV	Drive output regulator transceiver
VRF1	J3	LV	Output regulator transceiver
VMMC1DRV	L7	MV	Drive output regulator MMC1 module
VMMC1	K6	LV	Output regulator MMC1 module
VMMC2DRV	J2	MV	Drive output regulator MMC2 module
VMMC2	K3	LV	Output regulator MMC2 module
SIMEN	D19	LV	VSIM enable input
ESIMEN	F16	LV	VESIM enable input
VIBEN	E19	LV	VVIB enable input
REGEN	E18	LV	Regulator enable input
GPO1	G8	LV	General purpose output 1 to be used for enabling a discrete regulator
GPO2	F6	LV	General purpose output 2 to be used for enabling a discrete regulator
GPO3	E5	LV	General purpose output 3 to be used for enabling a discrete regulator
GPO4	G9	LV	General purpose output 4 to be used for enabling a discrete regulator
GNDREG1	N12	—	Ground for regulators 1
GNDREG2	K10	—	Ground for regulators 2
USB/RS232			

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
UDP	C2	EMV	1. USB transceiver cable interface, D+ 2. RS232 transceiver cable interface, transmit output or receive input signal
UDM	D2	EMV	1. USB transceiver cable interface, D- 2. RS232 transceiver cable interface, receive input or transmit output signal
UID	F7	EMV	USB on the go transceiver cable ID resistor connection
UDATVP	C5	LV	1. USB processor interface transmit data input (logic level version of D+/D-) or transmit positive data input (logic level version of D+) 2. Optional USB processor interface receive data output (logic level version of D+/D-) 3. RS232 processor interface
USE0VM	C6	LV	1. USB processor interface transmit single ended zero signal input or transmit minus data input (logic level version of D-) 2. Optional USB processor interface received single ended zero output 3. Optional RS232 processor interface
UTXENB	C4	LV	1. USB processor interface transmit enable bar
URCVD	B5	LV	Optional USB receiver processor interface differential data output (logic level version of D+/D-)
URXVP	B3	LV	Optional USB receiver processor interface data output (logic level version of D+)
URXVM	B2	LV	1. Optional USB receiver processor interface data output (logic level version of D-) 2. Optional RS232 processor interface
UMOD0	H7	LV	USB transceiver operation mode selection at power up 0
UMOD1	G6	LV	USB transceiver operation mode selection at power up 1
USBEN	C3	LV	Boot mode enable for USB/RS232 interface
VINBUS	B4	EMV	Input for VBUS and VUSB regulators for USB on the go mode
VBUS	D3	EHV	When in common input configuration, shorted to CHRGRAW 1. USB transceiver cable interface VBUS 2. Output VBUS regulator in USB on the go mode
		EMV	When in separate input configuration, not shorted to CHRGRAW 1. USB transceiver cable interface VBUS 2. Output VBUS regulator in USB on the go mode
VUSB	F5	MV	Output VUSB regulator as used by the USB transceiver
USBVCC	E7	LV	Supply for processor interface
GNDUSBA	A1 A2 B1	—	Ground for USB transceiver and USB cable
GNDUSBD	K9	—	Ground for USB processor interface

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
Control Logic			
ON1B	E16	LV	Power on/off button connection 1
ON2B	E15	LV	Power on/off button connection 2
ON3B	G14	LV	Power on/off button connection 3
WDI	F17	LV	Watchdog input
RESETB	G15	LV	Reset output
RESETBMCU	F18	LV	Reset for the processor
STANDBYPRI	H14	LV	Standby input signal from primary processor
STANDBYSEC	J13	LV	Standby input signal from secondary processor
LOBATB	N14	LV	Low battery indicator signal or end of life indicator signal
PWRRDY	U17	LV	Power ready signal after DVS and power gate transition
PWRFAIL	F13	LV	Power fail indicator output to processor or system
USEROFF	E14	LV	User off signalling from processor
MEMHLDDRV	G12	LV	Memory hold FET drive for power cut support
CSOUT	G11	LV	Chip select output for memory
LICELL	C16	MV	1. Coincell supply input 2. Coincell charger output
VBKUP1	E12	LV	Backup output voltage for memory
VBKUP2	F12	LV	Backup output voltage for processor core
GNDCTRL	J12	—	Ground for control logic
Oscillator and real time clock			
XTAL1	V16	LV	32.768 kHz Oscillator crystal connection 1
XTAL2	V14	LV	32.768 kHz Oscillator crystal connection 2
CLK32K	R14	LV	32 kHz Clock output
CLK32KMCU	E13	LV	32 kHz Clock output to the processor
CLKSEL	U16	LV	Enables the RC clock routing to the outputs
GNDRTC	V15	—	Ground for the RTC block
Power Up Select			
PUMS1	H6	LV	Power up mode supply setting 1
PUMS2	J7	LV	Power up mode supply setting 2
PUMS3	H5	LV	Power up mode supply setting 3
ICTEST	F14	LV	Test mode selection
ICSCAN	U14	LV	Scan mode selection

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
SPI Interface			
PRIVCC	N2	LV	Supply for primary SPI bus and audio bus 1
PRICLK	N5	LV	Primary SPI clock input
PRIMOSI	N8	LV	Primary SPI write input
PRIMISO	P7	LV	Primary SPI read output
PRICS	N6	LV	Primary SPI select input
PRIINT	P5	LV	Interrupt to processor controlling the primary SPI bus
SECVCC	N3	LV	Supply for secondary SPI bus and audio bus 2
SECCLK	P6	LV	Secondary SPI clock input
SECMOSI	R6	LV	Secondary SPI write input
SECMISO	R5	LV	Secondary SPI read output
SECCS	P8	LV	Secondary SPI select input
SECINT	R7	LV	Interrupt to processor controlling the secondary SPI bus
GNDSPI	L9	LV	Ground for SPI interface
A to D Converter			
BATTDETB	K13	LV	Battery thermistor presence detect output
ADIN5	M14	LV	ADC generic input channel 5, group 1
ADIN6	U15	LV	ADC generic input channel 6, group 1
ADIN7	R15	LV	ADC generic input channel 7, group 1
ADIN8	P14	LV	ADC generic input channel 8, group 2
ADIN9	V17	LV	ADC generic input channel 9, group 2
ADIN10	V18	LV	ADC generic input channel 10, group 2
ADIN11	V19 W18 W19	LV	ADC generic input channel 11, group 2
TSX1	P13	LV	ADC generic input channel 12 or touchscreen input X1, group 2
TSX2	L13	LV	ADC generic input channel 13 or touchscreen input X2, group 2
TSY1	P12	LV	ADC generic input channel 14 or touchscreen input Y1, group 2
TSY2	M13	LV	ADC generic input channel 15 or touchscreen input Y2, group 2
ADREF	R13	LV	Reference touchscreen interface
ADTRIG	N15	LV	ADC trigger input
ADOUT	E6	LV	ADC trigger output
GNDADC	L12	—	Ground for A to D circuitry

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
Audio Bus			
BCL1	M7	LV	Bit clock for audio bus 1. Input in slave mode, output in master mode
FS1	M9	LV	Frame synchronization clock for audio bus 1. Input in slave mode, output in master mode
RX1	L5	LV	Receive data input for audio bus 1
TX1	M6	LV	Transmit data output for audio bus 1
BCL2	M8	LV	Bit clock for audio bus 2. Input in slave mode, output in master mode
FS2	M2	LV	Frame synchronization clock for audio bus 2. Input in slave mode, output in master mode
RX2	M3	LV	Receive data input for audio bus 2
TX2	M5	LV	Transmit data output for audio bus 2
CLIA	L6	LV	Clock input for audio bus 1 or 2
CLIB	L3	LV	Clock input for audio bus 1 or 2
Audio Transmit			
MC1RB	R2	LV	Handset primary or right microphone supply output with integrated bias resistor
MC1LB	P3	LV	Handset secondary or left microphone supply output with integrated bias resistor
MC2B	P2	LV	Headset microphone supply output with integrated bias resistor and detect
MC1RIN	V2	LV	Handset primary or right microphone amplifier input
MC1LIN	U2	LV	Handset secondary or left microphone amplifier input
MC2IN	U3	LV	Headset microphone amplifier input
TXIN	U4	LV	General purpose line level transmit input
TXOUT	V3	LV	Buffered output of CEA-936-A microphone signal
Audio Receive			
SPP	V9	LV	Handset ear piece speaker amplifier output positive terminal
SPM	V10	LV	Handset ear piece speaker amplifier output minus terminal
VINLSP	V6	MV	Handset loudspeaker and alert amplifier supply input
LSPP	V5	MV	Handset loudspeaker and alert amplifier positive terminal
LSPM	V4	MV	Handset loudspeaker and alert amplifier minus terminal
GNDLSP	V1 W1 W2	—	Ground for loudspeaker amplifier
LSPL	U5	LV	Low-Power output for discrete loudspeaker amplifier, associated to left channel audio
CDCOUT	U6	LV	Low-Power output for discrete amplifier, associated to voice CODEC channel
HSL	V8	LV	Headset left channel amplifier output

Table 12-2. Pinout Listing (continued)

Pin	Location	Rating	Function
HSR	U9	LV	Headset right channel amplifier output
HSPGF	V7	LV	Headset phantom ground power line (force)
HSPGS	P10	LV	Headset phantom ground feedback line (sense)
HSDET	R10	LV	Headset sleeve detection input
HSLDET	R8	LV	Headset left detection input
RXOUTR	U7	LV	Low-Power receive output for accessories right channel
RXOUTL	P9	LV	Low-Power receive output for accessories left channel
RXINR	R9	LV	General purpose receive input right channel
RXINL	U8	LV	General purpose receive input left channel
Audio Other			
REFA	R3	LV	Reference for audio amplifiers
REFB	T3	LV	Reference for low noise audio bandgap
REFC	T2	LV	Reference for voice CODEC
REFD	L2	LV	Reference for stereo DAC
PLLLPF	H2	LV	Connection for the stereo DAC PLL low pass filter.
GNDPLL	H3	—	Dedicated ground for the stereo DAC PLL block.
GNDAUD1	L10	—	Ground for audio circuitry 1 (analog)
GNDAUD2	M10	—	Ground for audio circuitry 2 (analog)
GNDAUD3	M11	—	Ground for audio circuitry 3 (analog)
GNDAUD4	M12	—	Ground for audio circuitry 4 (digital)
GNDAUD5	H9	—	Ground for audio circuitry 5 (digital)
Thermal Grounds			
GNDSUB1	N11	—	Non critical signal ground and thermal heatsink
GNDSUB2	K12	—	Non critical signal ground and thermal heatsink
GNDSUB3	K11	—	Non critical signal ground and thermal heatsink
GNDSUB4	H12	—	Non critical signal ground and thermal heatsink
GNDSUB5	J9	—	Non critical signal ground and thermal heatsink
GNDSUB6	J8	—	Non critical signal ground and thermal heatsink
GNDSUB7	L8	—	Non critical signal ground and thermal heatsink
GNDSUB8	L11	—	Non critical signal ground and thermal heatsink
Future Use			
SPARE2	H8	TBD	Spare ball for future use
SPARE4	H13	TBD	Spare ball for future use

The ball map to accompany Table 12-2 is provided in Figure 12-2 as the top view. In other words, the BGA footprint on the phone PCB will have the same mapping as given in Figure 12-2.

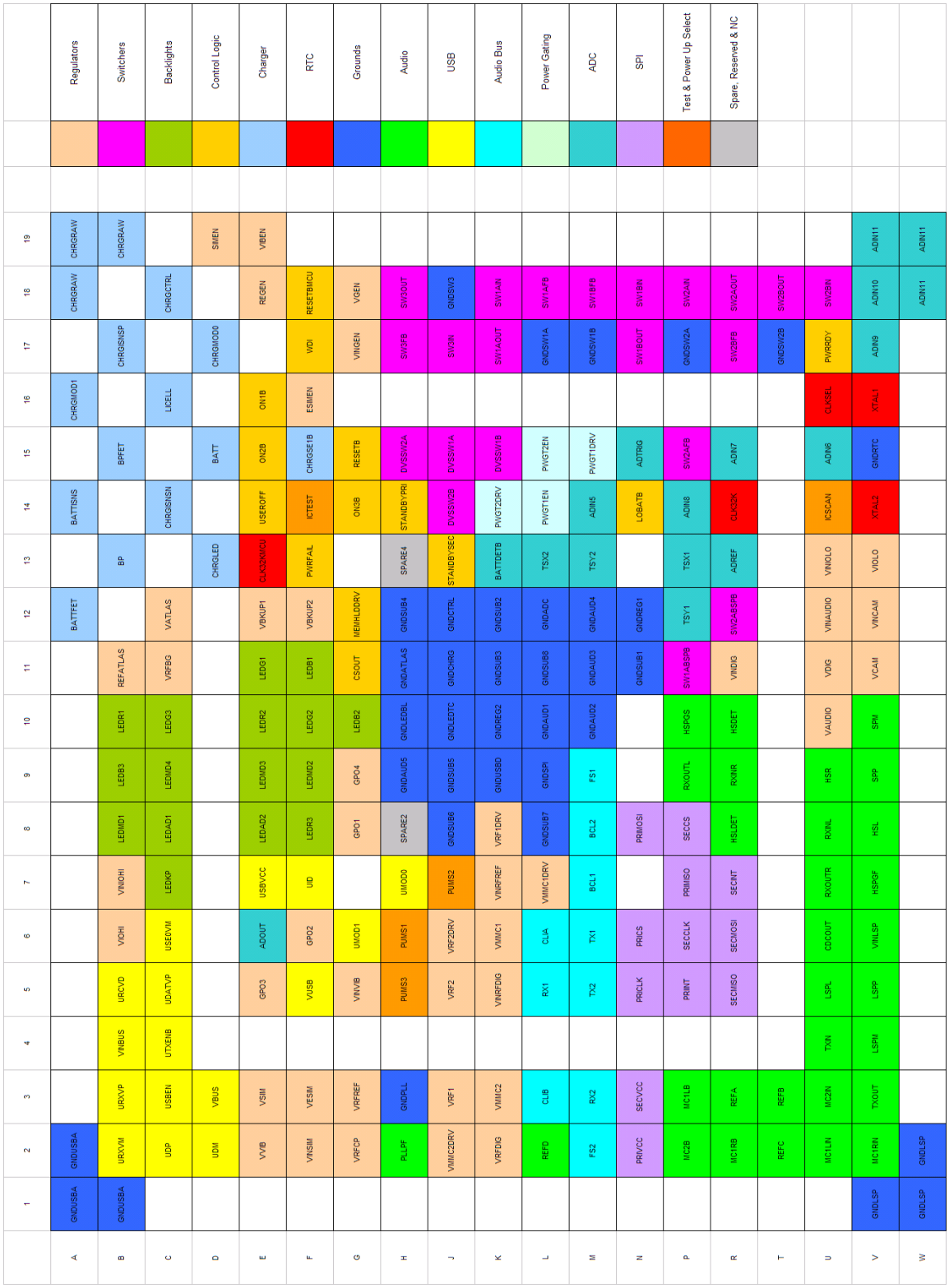


Figure 12-2. BGA Ball Map

12.3 Thermal Characteristics

12.3.1 Rating Data

The thermal rating data of the MC13783 package has been simulated with the results as listed in Table 12-3.

Table 12-3. Thermal Rating Data

Rating Parameter	Condition	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	—	RθJA	60	°C/W	1, 2
Junction to Ambient Natural Convection	Four layer board (2s2p)	RθJMA	29	°C/W	1, 3
Junction to Ambient (@200 ft./min)	Single layer board (1s)	RθJMA	48	°C/W	1, 3
Junction to Ambient (@200 ft./min)	Four layer board (2s2p)	RθJMA	25	°C/W	1, 3
Junction to Board	—	RθJB	14	°C/W	4
Junction to Case	—	RθJC	11	°C/W	5
Junction to Package Top	Natural Convection	θJT	3	°C/W	6

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol R JA or JA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. R JMA or JMA (Theta-JMA) will be used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, will continue to be commonly used.

The JEDEC standards can be consulted at http://www.jedec.org/.

12.3.2 Estimation of Junction Temperature

An estimation of the chip junction temperature TJ can be obtained from the equation:

TJ = TA + (R JA x PD)

with

TA = Ambient temperature for the package in °C

R JA = Junction to ambient thermal resistance in °C/W

PD = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board R JA and the value obtained on a board with two planes R JMA. For packages such as the BGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

For many natural convection and especially closed box applications, the board temperature at the perimeter or edge of the package will be approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature TJ is estimated using the following equation:

TJ = TB + (R JB x PD)

with

TB = Board temperature at the package perimeter in °C

R JB = Junction to board thermal resistance in °C/W

PD = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

Chapter 13
SPI Bitmap

This chapter provides the SPI bitmap diagram and register summary tables. For register details on individual modules, see the specific chapters within this book.

13.1 Bitmap Diagram

The complete SPI bitmap of the MC13783 is given in Figure 13-1 with one register per row for a general overview. The color coding indicates the SPI access mechanism according the following scheme:

Pale Green = Write and Read access for Primary SPI only

Pale Blue = Write and Read access for one of the SPIs

Light Blue = Write access for one of the SPIs, read access for both SPIs

Pale Orange = No write access, Read access for both SPIs

Pale Purple = Write and Read access for both SPIs

Lavender = PRI only, access with ICTEST is high

Reserved = Bits available but not assigned

White and empty = Non available bits

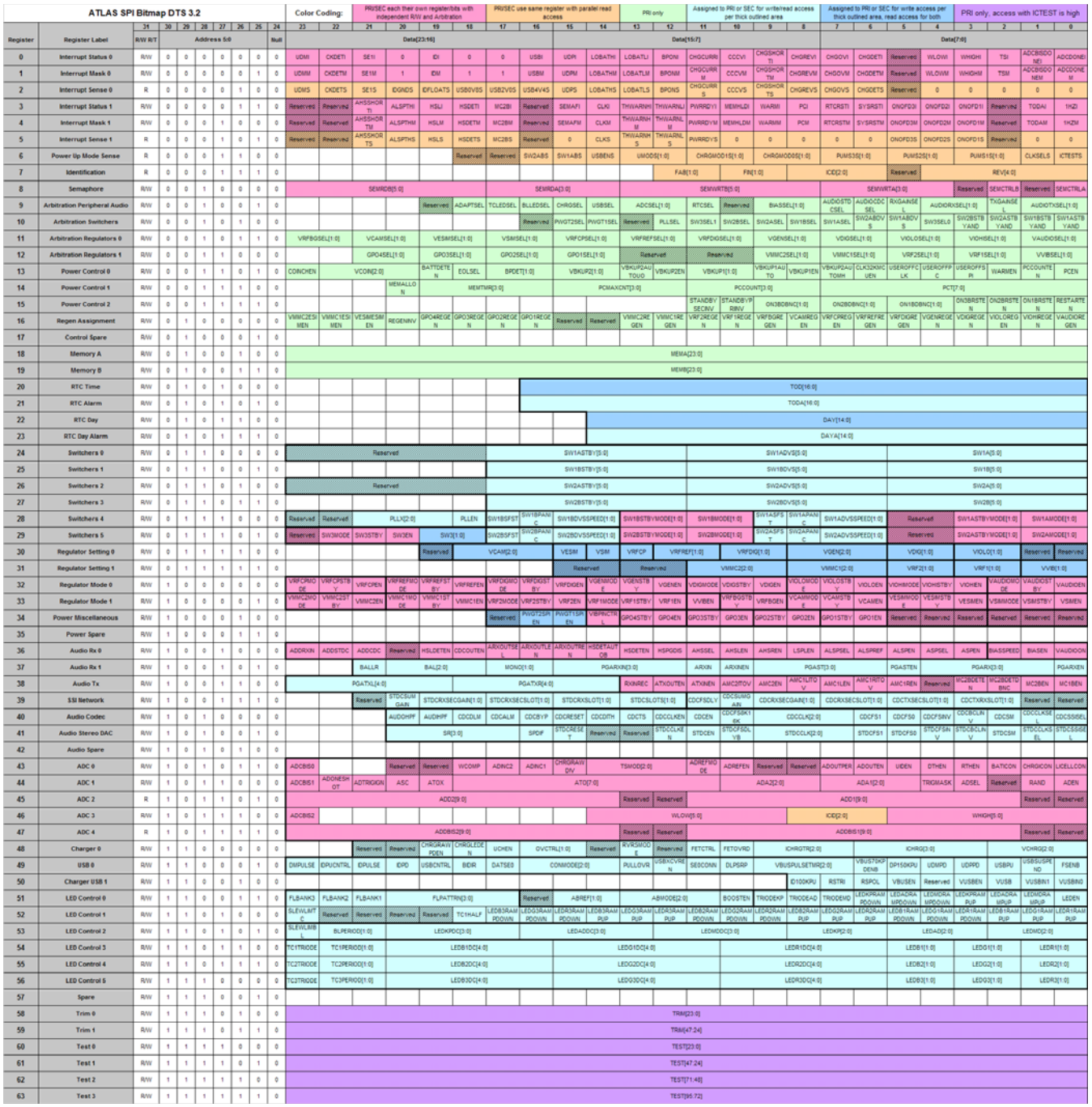


Figure 13-1. SPI Bitmap Overview

Using the SPI bitmap overview, the SPI access mechanism as described in Chapter 3, “Programmability” can also be represented graphically as shown in Figure 13-2. The same color coding scheme is used with the exception of registers reading back all 0 which are colored white.

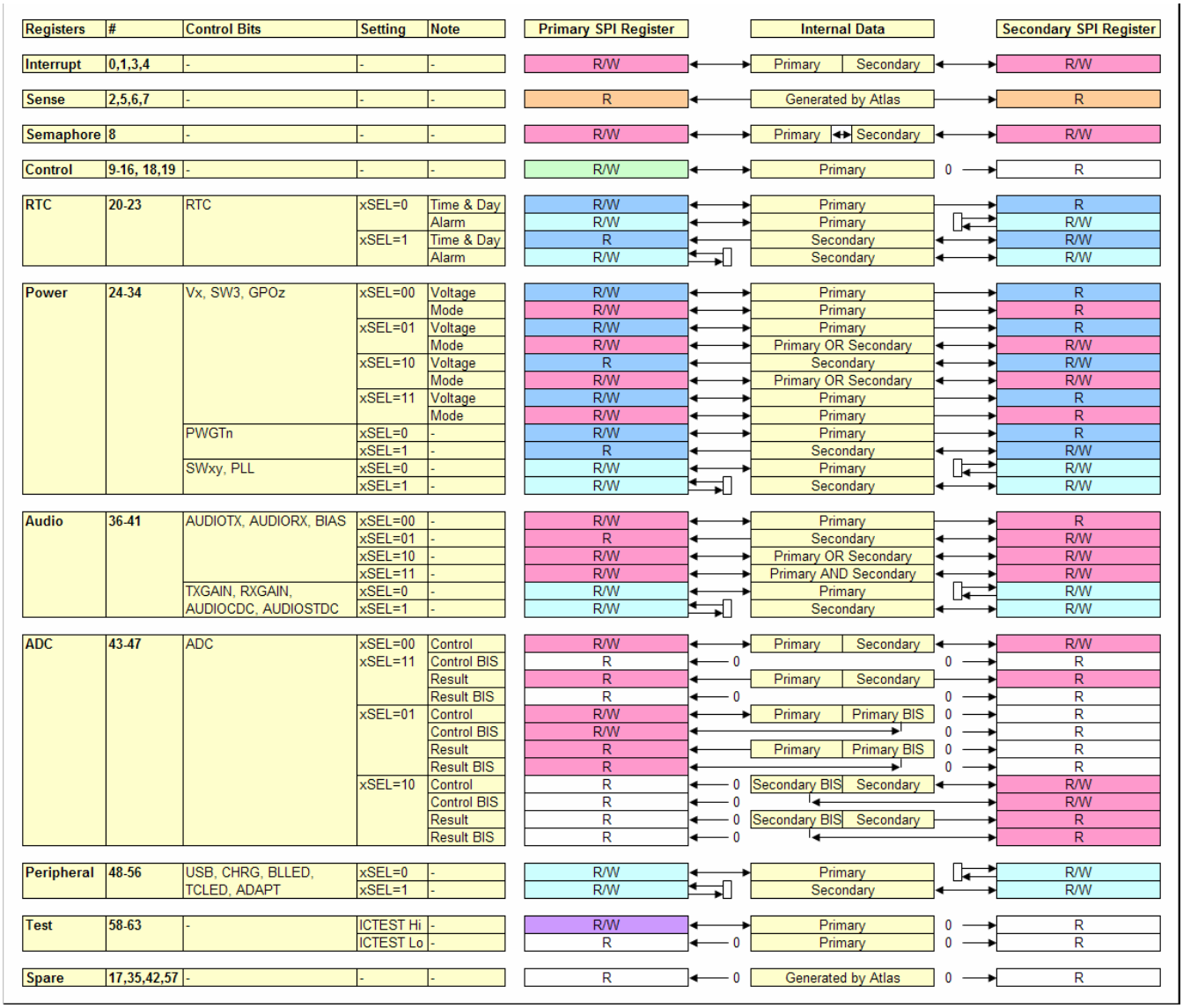


Figure 13-2. SPI Access Mechanism

13.2 MC13783 Device Register Summary

The contents of all individual 64 registers are given in Table 13-1 through Table 13-62. The individual tables include the following information:

- Table X-Y Register number (0-63), name of register
- Name: Name of the Bit. Reserved bits are available in the design but are not assigned. Unused bits are not available in the design.
- Bit #: The bit location in the register (0-23)
- R/W: R is read access, W is write access, R/W is read and write access
- Reset: The Reset signal can be RESETB which is the same signal as the RESETB pin, RTCPORB which is the reset signal of the RTC module, or TURNOFF which is the signal indicating the OFF

mode is entered. There is no reset signal for hard wired bits nor for the bits of which the state is determined by the power up mode settings, which is indicated by NONE.

- Default: The value after reset. If an * is indicated then the value depends on the power up mode setting as being validated at the beginning of cold start / warm start. Some bits default to a value which is dependent on the version of the IC.
- Description: A short description of the bit function, in some cases additional information is included

Table 13-1 through Table 13-62 are intended to give a summarized overview, for details on the bit description, see the individual chapters.

Table 13-1. Register 0, Interrupt Status 0

Name	Bit #	R/W	Reset	Default	Description
ADCDONEI	0	R/W	RESETB	0	ADC has finished requested conversions
ADCBISDONEI	1	R/W	RESETB	0	ADCBIS has finished requested conversions
TSI	2	R/W	RESETB	0	Touchscreen wake up
WHIGHI	3	R/W	RESETB	0	ADC reading above high limit
WLOWI	4	R/W	RESETB	0	ADC reading below low limit
Reserved	5	R/W	RESETB	0	For future use
CHGDETI	6	R/W	RESETB	0	Charger attach
CHGOVI	7	R/W	RESETB	0	Charger over voltage detection
CHGREVI	8	R/W	RESETB	0	Charger path reverse current
CHGSHORTI	9	R/W	RESETB	0	Charger path short circuit
CCCVI	10	R/W	RESETB	0	Charger path V or I regulation
CHGCURRI	11	R/W	RESETB	0	Charge current below threshold warning
BPONI	12	R/W	RTCPORB	0	BP turn on threshold
LOBATLI	13	R/W	RESETB	0	Low battery low threshold warning
LOBATHI	14	R/W	RESETB	0	Low battery high threshold warning
UDPI	15	R/W	RESETB	0	UDP detect
USBI	16	R/W	RESETB	0	USB VBUS detect
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
IDI	19	R/W	RESETB	0	USB ID detect
Unused	20	R	—	0	Not available
SE1I	21	R/W	RESETB	0	Single ended 1 detect
CKDETI	22	R/W	RESETB	0	Carkit detect
UDMI	23	R/W	RESETB	0	UDM detect

Table 13-2. Register 1, Interrupt Mask 0

Name	Bit #	R/W	Reset	Default	Description
ADCDONEM	0	R/W	RESETB	1	ADCDONEI mask bit
ADCBISDONEM	1	R/W	RESETB	1	ADCBISDONEI mask bit
TSM	2	R/W	RESETB	1	TSI mask bit
WHIGHM	3	R/W	RESETB	1	WHIGHI mask bit
WLOWM	4	R/W	RESETB	1	WLOWI mask bit
Reserved	5	R/W	RESETB	1	For future use
CHGDETM	6	R/W	RESETB	1	CHGDETI mask bit
CHGOVM	7	R/W	RESETB	1	CHGOVI mask bit
CHGREVM	8	R/W	RESETB	1	CHGREVI mask bit
CHGSHORTM	9	R/W	RESETB	1	CHGSHORTI mask bit
CCCVM	10	R/W	RESETB	1	CCCVI mask bit
CHGCURRM	11	R/W	RESETB	1	CHGCURRI mask bit
BPONM	12	R/W	RTCPORB	1	BPONI mask bit
LOBATLM	13	R/W	RESETB	1	LOBATLI mask bit
LOBATHM	14	R/W	RESETB	1	LOBATHI mask bit
UDPM	15	R/W	RESETB	1	UDPI mask bit
USBM	16	R/W	RESETB	1	USBI mask bit
Unused	17	R	—	1	Not available
Unused	18	R	—	1	Not available
IDM	19	R/W	RESETB	1	IDI mask bit
Unused	20	R	—	1	Unused
SE1M	21	R/W	RESETB	1	SE1I mask bit
CKDETM	22	R/W	RESETB	1	CKDETI mask bit
UDMM	23	R/W	RESETB	1	UDMI mask bit

Table 13-3. Register 2, Interrupt Sense 0

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R	—	0	Not available
Unused	1	R	—	0	Not available
Unused	2	R	—	0	Not available
Unused	3	R	—	0	Not available
Unused	4	R	—	0	Not available
Reserved	5	R	RESETB	0	For future use

Table 13-3. Register 2, Interrupt Sense 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
CHGDETS	6	R	RESETB	0	CHGDETI sense bit
CHGOVS	7	R	RESETB	0	CHGOVI sense bit
CHGREVS	8	R	RESETB	0	CHGREVI sense bit
CHGSHORTS	9	R	RESETB	0	CHGSHORTI sense bit
CCCVS	10	R	RESETB	0	CCCVI sense bit
CHGCURRS	11	R	RESETB	0	CHGCURRI sense bit
BPONS	12	R	RESETB	0	BPONI sense bit
LOBATLS	13	R	RESETB	0	LOBATLI sense bit
LOBATHS	14	R	RESETB	0	LOBATHI sense bit
UDPS	15	R	RESETB	0	UDPI sense bit
USB4V4S	16	R	RESETB	0	USB4V4 sense bit
USB2V0S	17	R	RESETB	0	USB2V0 sense bit
USB0V8S	18	R	RESETB	0	USB0V8 sense bit
IDFLOATS	19	R	RESETB	0	ID float sense bit
IDGNDS	20	R	RESETB	0	ID ground sense bit
SE1S	21	R	RESETB	0	SE1I sense bit
CKDETS	22	R	RESETB	0	CKDETI sense bit
UDMS	23	R	RESETB	0	UDMI sense bit

Table 13-4. Register 3, Interrupt Status 1

Name	Bit #	R/W	Reset	Default	Description
1HZI	0	R/W	RTCPORB	0	1 Hz timetick
TODAI	1	R/W	RTCPORB	0	Time of day alarm
Reserved	2	R/W	RESETB	0	For future use
ONOFD1I	3	R/W	RESETB	0	ON1B event
ONOFD2I	4	R/W	RESETB	0	ON2B event
ONOFD3I	5	R/W	RESETB	0	ON3B event
SYSRSTI	6	R/W	RTCPORB	0	System reset
RTCRSTI	7	R/W	RTCPORB	0	RTC reset event
PCI	8	R/W	RTCPORB	0	Power cut event
WARMI	9	R/W	RTCPORB	0	Warm start event
MEMHLDI	10	R/W	RTCPORB	0	Memory hold event
PWRRDYI	11	R/W	RESETB	0	Power Gate and DVS Power ready

Table 13-4. Register 3, Interrupt Status 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
THWARNLI	12	R/W	RESETB	0	Thermal warning low threshold
THWARNHI	13	R/W	RESETB	0	Thermal warning high threshold
CLKI	14	R/W	RESETB	0	Clock source change
SEMAFI	15	R/W	RESETB	0	Semaphore
Reserved	16	R/W	RESETB	0	For future use
MC2BI	17	R/W	RESETB	0	Microphone bias 2 detect
HSDETI	18	R/W	RESETB	0	Headset attach
HSLI	19	R/W	RESETB	0	Stereo headset detect
ALSPTHI	20	R/W	RESETB	0	Thermal shutdown Alsp
AHSSHORTI	21	R/W	RESETB	0	Short circuit on Ahs outputs
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 13-5. Register 4, Interrupt Mask 1

Name	Bit #	R/W	Reset	Default	Description
1HZM	0	R/W	RTCPORB	1	1HZI mask bit
TODAM	1	R/W	RTCPORB	1	TODAI mask bit
Reserved	2	R/W	RESETB	1	For future use
ONOFD1M	3	R/W	RESETB	1	ONOFD1I mask bit
ONOFD2M	4	R/W	RESETB	1	ONOFD2I mask bit
ONOFD3M	5	R/W	RESETB	1	ONOFD3I mask bit
SYSRSTM	6	R/W	RTCPORB	1	SYSRSTI mask bit
RTCRSTM	7	R/W	RTCPORB	1	RTCRSTI mask bit
PCM	8	R/W	RTCPORB	1	PCI mask bit
WARMM	9	R/W	RTCPORB	1	WARMI mask bit
MEMHLDM	10	R/W	RTCPORB	1	MEMHLDI mask bit
PWRRDYM	11	R/W	RESETB	1	PWRRDYI mask bit
THWARNLM	12	R/W	RESETB	1	THWARNLI mask bit
THWARNHM	13	R/W	RESETB	1	THWARNHI mask bit
CLKM	14	R/W	RESETB	1	CLKI mask bit
SEMAFM	15	R/W	RESETB	1	SEMAFI mask bit
Reserved	16	R/W	RESETB	1	For future use
MC2BM	17	R/W	RESETB	1	MC2BI mask bit

Table 13-5. Register 4, Interrupt Mask 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
HSDETM	18	R/W	RESETB	1	HSDETI mask bit
HSLM	19	R/W	RESETB	1	HSLI mask bit
ALSPTHM	20	R/W	RESETB	1	ALSPTHI mask bit
AHSSHORTM	21	R/W	RESETB	1	AHSSHORTI mask bit
Reserved	22	R/W	RESETB	1	For future use
Reserved	23	R/W	RESETB	1	For future use

Table 13-6. Register 5, Interrupt Sense 1

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R	—	0	Not available
Unused	1	R	—	0	Not available
Reserved	2	R	RESETB	0	For future use
ONOFD1S	3	R	RESETB	0	ONOFD1I sense bit
ONOFD2S	4	R	RESETB	0	ONOFD2I sense bit
ONOFD3S	5	R	RESETB	0	ONOFD3I sense bit
Unused	6	R	—	0	Not available
Unused	7	R	—	0	Not available
Unused	8	R	—	0	Not available
Unused	9	R	—	0	Not available
Unused	10	R	—	0	Not available
PWRRDYS	11	R	RESETB	0	PWRRDYI sense bit
THWARNLS	12	R	RESETB	0	THWARNLI sense bit
THWARNHS	13	R	RESETB	0	THWARNHI sense bit
CLKS	14	R	RESETB	0	CLKI sense bit
Unused	15	R	—	0	Not available
Reserved	16	R	RESETB	0	For future use
MC2BS	17	R	RESETB	0	MC2BI sense bit
HSDETS	18	R	RESETB	0	HSDETI sense bit
HSLS	19	R	RESETB	0	HSLI sense bit
ALSPTHS	20	R	RESETB	0	ALSPTHI mask bit
AHSSHORTS	21	R	RESETB	0	AHSSHORTI mask bit
Reserved	22	R	RESETB	0	For future use
Reserved	23	R	RESETB	0	For future use

Table 13-7. Register 6, Power Up Mode Sense

Name	Bit #	R/W	Reset	Default	Description
ICTESTS	0	R	NONE	*	ICTEST state
CLKSELS	1	R	NONE	*	CLKSEL state
PUMS1S0	2	R	NONE	*	PUMS1 state
PUMS1S1	3	R	NONE	*	
PUMS2S0	4	R	NONE	*	PUMS2 state
PUMS2S1	5	R	NONE	*	
PUMS3S0	6	R	NONE	*	PUMS3 state
PUMS3S1	7	R	NONE	*	
CHRGMOD0S0	8	R	NONE	*	CHRGMOD0 state
CHRGMOD0S1	9	R	NONE	*	
CHRGMOD1S0	10	R	NONE	*	CHRGMOD1 state
CHRGMOD1S1	11	R	NONE	*	
UMODS0	12	R	NONE	*	UMOD state
UMODS1	13	R	NONE	*	
USBENS	14	R	NONE	*	USBEN state
SW1ABS	15	R	NONE	*	SW1A and SW1B joined
SW2ABS	16	R	NONE	*	SW2A and SW2B joined
Reserved	17	R	NONE	0	For future use
Reserved	18	R	NONE	0	For future use
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-8. Register 7, Identification

Name	Bit #	R/W	Reset	Default	Description
REV0	0	R	NONE	Version dependent	MC13783 revision
REV1	1	R	NONE	Version dependent	
REV2	2	R	NONE	Version dependent	
REV3	3	R	NONE	Version dependent	
REV4	4	R	NONE	Version dependent	
Reserved	5	R	NONE	0	For future use

Table 13-8. Register 7, Identification (continued)

Name	Bit #	R/W	Reset	Default	Description
ICID0	6	R	NONE	0	MC13783 derivative
ICID1	7	R	NONE	1	
ICID2	8	R	NONE	0	
FIN0	9	R	NONE	Version dependent	MC13783 fin version
FIN1	10	R	NONE	Version dependent	
FAB0	11	R	NONE	Fab dependent	MC13783 fab identifier
FAB1	12	R	NONE	Fab dependent	
Unused	13	R	—	0	Not available
Unused	14	R	—	0	Not available
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-9. Register 8, Semaphore

Name	Bit #	R/W	Reset	Default	Description
SEMCTRLA	0	R/W	RESETB	0	Semaphore control word A
Reserved	1	R/W	RESETB	0	For future use
SEMCTRLB	2	R/W	RESETB	0	Semaphore control word B
Reserved	3	R/W	RESETB	0	For future use
SEMWRTA0	4	R/W	RESETB	0	Semaphore write word A
SEMWRTA1	5	R/W	RESETB	0	
SEMWRTA2	6	R/W	RESETB	0	
SEMWRTA3	7	R/W	RESETB	0	

Table 13-9. Register 8, Semaphore (continued)

Name	Bit #	R/W	Reset	Default	Description
SEMWRTB0	8	R/W	RESETB	0	Semaphore write word B
SEMWRTB1	9	R/W	RESETB	0	
SEMWRTB2	10	R/W	RESETB	0	
SEMWRTB3	11	R/W	RESETB	0	
SEMWRTB4	12	R/W	RESETB	0	
SEMWRTB5	13	R/W	RESETB	0	
SEMRDA0	14	R/W	RESETB	0	Semaphore read word A other SPI
SEMRDA1	15	R/W	RESETB	0	
SEMRDA2	16	R/W	RESETB	0	
SEMRDA3	17	R/W	RESETB	0	
SEMRDB0	18	R/W	RESETB	0	Semaphore read word B other SPI
SEMRDB1	19	R/W	RESETB	0	
SEMRDB2	20	R/W	RESETB	0	
SEMRDB3	21	R/W	RESETB	0	
SEMRDB4	22	R/W	RESETB	0	
SEMRDB5	23	R/W	RESETB	0	

Table 13-10. Register 9, Arbitration Peripheral Audio

Name	Bit #	R/W	Reset	Default	Description
AUDIOTXSEL0	0	R/W	RESETB	0	Transmit audio amplifiers assignment
AUDIOTXSEL1	1	R/W	RESETB	0	
TXGAINSEL	2	R/W	RESETB	0	Transmit gain assignment
AUDIORXSEL0	3	R/W	RESETB	0	Receive audio amplifiers assignment
AUDIORXSEL1	4	R/W	RESETB	0	
RXGAINSEL	5	R/W	RESETB	0	Receive gain assignment
AUDIOCDCSEL	6	R/W	RESETB	0	Voice CODEC assignment
AUDIOSTDCSEL	7	R/W	RESETB	0	Stereo DAC assignment
BIASSEL0	8	R/W	RESETB	0	Audio bias assignment
BIASSEL1	9	R/W	RESETB	0	
Reserved	10	R/W	RESETB	0	For future use
RTCSEL	11	R/W	RESETB	0	RTC write assignment
ADCSEL0	12	R/W	RESETB	0	ADC assignment
ADCSEL1	13	R/W	RESETB	0	

Table 13-10. Register 9, Arbitration Peripheral Audio (continued)

Name	Bit #	R/W	Reset	Default	Description
USBSEL	14	R/W	RESETB	0	USB assignment
CHRGSEL	15	R/W	RESETB	0	Charger assignment
BLLEDSEL	16	R/W	RESETB	0	Backlight LED assignment
TCLEDSEL	17	R/W	RESETB	0	Tricolor LED assignment
ADAPTSEL	18	R/W	RESETB	0	Adaptive boost assignment
Reserved	19	R/W	RESETB	0	For future use
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-11. Register 10, Arbitration Switchers

Name	Bit #	R/W	Reset	Default	Description
SW1ASTBYAND	0	R/W	RESETB	0	Both standby pins control SW1A
SW1BSTBYAND	1	R/W	RESETB	0	Both standby pins control SW1B
SW2ASTBYAND	2	R/W	RESETB	0	Both standby pins control SW2A
SW2BSTBYAND	3	R/W	RESETB	0	Both standby pins control SW2B
SW3SEL0	4	R/W	RESETB	0	SW3 assignment bit 0
SW1ABDVS	5	R/W	RESETB	0	Two DVS pins control SW1
SW2ABDVS	6	R/W	RESETB	0	Two DVS pins control SW2
SW1ASEL	7	R/W	RESETB	0	SW1A assignment
SW1BSEL	8	R/W	RESETB	0	SW1B assignment
SW2ASEL	9	R/W	RESETB	0	SW2A assignment
SW2BSEL	10	R/W	RESETB	0	SW2B assignment
SW3SEL1	11	R/W	RESETB	0	SW3 assignment bit 1
PLLSEL	12	R/W	RESETB	0	Switcher PLL assignment
Reserved	13	R/W	RESETB	0	For future use
PWGT1SEL	14	R/W	RESETB	0	Power gate 1 assignment
PWGT2SEL	15	R/W	RESETB	0	Power gate 2 assignment
Reserved	16	R/W	RESETB	0	For future use
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available

Table 13-11. Register 10, Arbitration Switchers (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-12. Register 11, Arbitration Regulators 0

Name	Bit #	R/W	Reset	Default	Description
VAUDIOSEL0	0	R/W	RESETB	0	VAUDIO assignment
VAUDIOSEL1	1	R/W	RESETB	0	
VIOHISEL0	2	R/W	RESETB	0	VIOHI assignment
VIOHISEL1	3	R/W	RESETB	0	
VIOLOSEL0	4	R/W	RESETB	0	VIOLO assignment
VIOLOSEL1	5	R/W	RESETB	0	
VDIGSEL0	6	R/W	RESETB	0	VDIG assignment
VDIGSEL1	7	R/W	RESETB	0	
VGENSEL0	8	R/W	RESETB	0	VGEN assignment
VGENSEL1	9	R/W	RESETB	0	
VRFDIGSEL0	10	R/W	RESETB	0	VRFDIG assignment
VRFDIGSEL1	11	R/W	RESETB	0	
VRFREFSEL0	12	R/W	RESETB	0	VRFREF assignment
VRFREFSEL1	13	R/W	RESETB	0	
VRFCPSEL0	14	R/W	RESETB	0	VRFCP assignment
VRFCPSEL1	15	R/W	RESETB	0	
VSIMSEL0	16	R/W	RESETB	0	VSIM assignment
VSIMSEL1	17	R/W	RESETB	0	
VESIMSEL0	18	R/W	RESETB	0	VESIM assignment
VESIMSEL1	19	R/W	RESETB	0	
VCAMSEL0	20	R/W	RESETB	0	VCAM assignment
VCAMSEL1	21	R/W	RESETB	0	
VRFBGSEL0	22	R/W	RESETB	0	VRFBG assignment
VRFBGSEL1	23	R/W	RESETB	0	

Table 13-13. Register 12, Arbitration Regulators 1

Name	Bit #	R/W	Reset	Default	Description
VVIBSEL0	0	R/W	RESETB	0	VVIB assignment
VVIBSEL1	1	R/W	RESETB	0	
VRF1SEL0	2	R/W	RESETB	0	VRF1 assignment
VRF1SEL1	3	R/W	RESETB	0	
VRF2SEL0	4	R/W	RESETB	0	VRF2 assignment
VRF2SEL1	5	R/W	RESETB	0	
VMMC1SEL0	6	R/W	RESETB	0	VMMC1 assignment
VMMC1SEL1	7	R/W	RESETB	0	
VMMC2SEL0	8	R/W	RESETB	0	VMMC2 assignment
VMMC2SEL1	9	R/W	RESETB	0	
Reserved	10	R/W	RESETB	0	For future use
Reserved	11	R/W	RESETB	0	For future use
Reserved	12	R/W	RESETB	0	For future use
Reserved	13	R/W	RESETB	0	For future use
GPO1SEL0	14	R/W	RESETB	0	GPO1 assignment
GPO1SEL1	15	R/W	RESETB	0	
GPO2SEL0	16	R/W	RESETB	0	GPO2 assignment
GPO2SEL1	17	R/W	RESETB	0	
GPO3SEL0	18	R/W	RESETB	0	GPO3 assignment
GPO3SEL1	19	R/W	RESETB	0	
GPO4SEL0	20	R/W	RESETB	0	GPO4 assignment
GPO4SEL1	21	R/W	RESETB	0	
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-14. Register 13, Power Control 0

Name	Bit #	R/W	Reset (*)	Default	Description
PCEN	0	R/W	RTCPORB	0	Power cut enable
PCCOUNTEN	1	R/W	RTCPORB	0	Power cut counter enable
WARMEN	2	R/W	RTCPORB	0	Warm start enable
USEROFFSPI	3	R/W	RESETB	0	SPI command for entering user off modes
USEROFFPC	4	R/W	RTCPORB	0	Automatic transition to user off during power cut
USEROFFCLK	5	R/W	RTCPORB	0	Keeps the CLK32KMCU active during user off power cut modes

Table 13-14. Register 13, Power Control 0 (continued)

Name	Bit #	R/W	Reset (*)	Default	Description
CLK32KMCUEN	6	R/W	RTCPORB	1	Enables the CLK32KMCU
VBKUP2AUTOMH	7	R/W	OFFB	0	Automatically enables VBKUP2 in the memory hold modes
VBKUP1EN	8	R/W	RESETB	0	Enables VBKUP1 regulator
VBKUP1AUTO	9	R/W	OFFB	0	Automatically enables VBKUP1 in the memory hold and user off modes
VBKUP10	10	R/W	NONE	*	Sets VBKUP1 voltage
VBKUP11	11	R/W	NONE	*	
VBKUP2EN	12	R/W	RESETB	0	Enables VBKUP2 regulator
VBKUP2AUTOUO	13	R/W	OFFB	0	Automatically enables VBKUP2 in the user off modes
VBKUP20	14	R/W	NONE	*	Sets VBKUP2 voltage
VBKUP21	15	R/W	NONE	*	
BPDET0	16	R/W	RTCPORB	0	BP detection threshold setting
BPDET1	17	R/W	RTCPORB	0	
EOLSEL	18	R/W	RTCPORB	0	Selects EOL function instead of LOBAT
BATTDETEN	19	R/W	RTCPORB	0	Enables battery detect function
VCOIN0	20	R/W	RTCPORB	0	Coincell charger voltage setting
VCOIN1	21	R/W	RTCPORB	0	
VCOIN2	22	R/W	RTCPORB	0	
COINCHEN	23	R/W	RTCPORB	0	Coincell charger enable
(*) OFFB represents a reset when in Off or Invalid Power modes					

Table 13-15. Register 14, Power Control 1

Name	Bit #	R/W	Reset	Default	Description
PCT0	0	R/W	RTCPORB	0	Power cut timer
PCT1	1	R/W	RTCPORB	0	
PCT2	2	R/W	RTCPORB	0	
PCT3	3	R/W	RTCPORB	0	
PCT4	4	R/W	RTCPORB	0	
PCT5	5	R/W	RTCPORB	0	
PCT6	6	R/W	RTCPORB	0	
PCT7	7	R/W	RTCPORB	0	

Table 13-15. Register 14, Power Control 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
PCCOUNT0	8	R/W	RTCPORB	0	Power cut counter
PCCOUNT1	9	R/W	RTCPORB	0	
PCCOUNT2	10	R/W	RTCPORB	0	
PCCOUNT3	11	R/W	RTCPORB	0	
PCMAXCNT0	12	R/W	RTCPORB	0	Maximum allowed number of power cuts
PCMAXCNT1	13	R/W	RTCPORB	0	
PCMAXCNT2	14	R/W	RTCPORB	0	
PCMAXCNT3	15	R/W	RTCPORB	0	
MEMTMR0	16	R/W	RTCPORB	0	Extended power cut timer
MEMTMR1	17	R/W	RTCPORB	0	
MEMTMR2	18	R/W	RTCPORB	0	
MEMTMR3	19	R/W	RTCPORB	0	
MEMALLON	20	R/W	RTCPORB	0	Extended power cut timer set to infinite
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-16. Register 15, Power Control 2

Name	Bit #	R/W	Reset	Default	Description
RESTARTEN	0	R/W	RTCPORB	0	Enables automatic restart after a system reset
ON1BRSTEN	1	R/W	RTCPORB	0	Enables system reset on ON1B pin
ON2BRSTEN	2	R/W	RTCPORB	0	Enables system reset on ON2B pin
ON3BRSTEN	3	R/W	RTCPORB	0	Enables system reset on ON3B pin
ON1BDBNC0	4	R/W	RTCPORB	0	Sets debounce time on ON1B pin
ON1BDBNC1	5	R/W	RTCPORB	0	
ON2BDBNC0	6	R/W	RTCPORB	0	Sets debounce time on ON2B pin
ON2BDBNC1	7	R/W	RTCPORB	0	
ON3BDBNC0	8	R/W	RTCPORB	0	Sets debounce time on ON3B pin
ON3BDBNC1	9	R/W	RTCPORB	0	
STANDBYPRIINV	10	R/W	RTCPORB	0	If set then STANDBYPRI is interpreted as active low
STANDBYSECINV	11	R/W	RTCPORB	0	If set then STANDBYSEC is interpreted as active low
Unused	12	R	—	0	Not available
Unused	13	R	—	0	Not available

Table 13-16. Register 15, Power Control 2 (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	14	R	—	0	Not available
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-17. Register 16, Regen Assignment

Name	Bit #	R/W	Reset	Default	Description
VAUDIOREGEN	0	R/W	RESETB	0	VAUDIO enabled by REGEN
VIOHIREGEN	1	R/W	RESETB	0	VIOHI enabled by REGEN
VIOLOREGEN	2	R/W	RESETB	0	VIOLO enabled by REGEN
VDIGREGEN	3	R/W	RESETB	0	VDIG enabled by REGEN
VGENREGEN	4	R/W	RESETB	0	VGEN enabled by REGEN
VRFDIGREGEN	5	R/W	RESETB	0	VRFDIG enabled by REGEN
VRFREFREGEN	6	R/W	RESETB	0	VRFREF enabled by REGEN
VRFCPREGEN	7	R/W	RESETB	0	VRFCP enabled by REGEN
VCAMREGEN	8	R/W	RESETB	0	VCAM enabled by REGEN
VRFBGREGEN	9	R/W	RESETB	0	VRFBG enabled by REGEN
VRF1REGEN	10	R/W	RESETB	0	VRF1 enabled by REGEN
VRF2REGEN	11	R/W	RESETB	0	VRF2 enabled by REGEN
VMMC1REGEN	12	R/W	RESETB	0	VMMC1 enabled by REGEN
VMMC2REGEN	13	R/W	RESETB	0	VMMC2 enabled by REGEN
Reserved	14	R/W	RESETB	0	For future use
Reserved	15	R/W	RESETB	0	For future use
GPO1REGEN	16	R/W	RESETB	0	GPO1 enabled by REGEN
GPO2REGEN	17	R/W	RESETB	0	GPO2 enabled by REGEN
GPO3REGEN	18	R/W	RESETB	0	GPO3 enabled by REGEN
GPO4REGEN	19	R/W	RESETB	0	GPO4 enabled by REGEN

Table 13-17. Register 16, Regen Assignment (continued)

Name	Bit #	R/W	Reset	Default	Description
REGENINV	20	R/W	RESETB	0	REGEN polarity inversion
VESIMESIMEN	21	R/W	RESETB	1	VESIM enabled by ESIMEN
VMMC1ESIMEN	22	R/W	RESETB	0	VMMC1 enabled by ESIMEN
VMMC2ESIMEN	23	R/W	RESETB	0	VMMC2 enabled by ESIMEN

Table 13-18. Register 17, Control Spare

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R	—	0	Not available
Unused	1	R	—	0	Not available
Unused	2	R	—	0	Not available
Unused	3	R	—	0	Not available
Unused	4	R	—	0	Not available
Unused	5	R	—	0	Not available
Unused	6	R	—	0	Not available
Unused	7	R	—	0	Not available
Unused	8	R	—	0	Not available
Unused	9	R	—	0	Not available
Unused	10	R	—	0	Not available
Unused	11	R	—	0	Not available
Unused	12	R	—	0	Not available
Unused	13	R	—	0	Not available
Unused	14	R	—	0	Not available
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-19. Register 18, Memory A

Name	Bit #	R/W	Reset	Default	Description
MEMA0	0	R/W	RTCPORB	0	Backup memory A
MEMA1	1	R/W	RTCPORB	0	
MEMA2	2	R/W	RTCPORB	0	
MEMA3	3	R/W	RTCPORB	0	
MEMA4	4	R/W	RTCPORB	0	
MEMA5	5	R/W	RTCPORB	0	
MEMA6	6	R/W	RTCPORB	0	
MEMA7	7	R/W	RTCPORB	0	
MEMA8	8	R/W	RTCPORB	0	
MEMA9	9	R/W	RTCPORB	0	
MEMA10	10	R/W	RTCPORB	0	
MEMA11	11	R/W	RTCPORB	0	
MEMA12	12	R/W	RTCPORB	0	
MEMA13	13	R/W	RTCPORB	0	
MEMA14	14	R/W	RTCPORB	0	
MEMA15	15	R/W	RTCPORB	0	
MEMA16	16	R/W	RTCPORB	0	
MEMA17	17	R/W	RTCPORB	0	
MEMA18	18	R/W	RTCPORB	0	
MEMA19	19	R/W	RTCPORB	0	
MEMA20	20	R/W	RTCPORB	0	
MEMA21	21	R/W	RTCPORB	0	
MEMA22	22	R/W	RTCPORB	0	
MEMA23	23	R/W	RTCPORB	0	

Table 13-20. Register 19, Memory B

Name	Bit #	R/W	Reset	Default	Description
MEMB0	0	R/W	RTCPORB	0	Backup memory B
MEMB1	1	R/W	RTCPORB	0	
MEMB2	2	R/W	RTCPORB	0	
MEMB3	3	R/W	RTCPORB	0	
MEMB4	4	R/W	RTCPORB	0	
MEMB5	5	R/W	RTCPORB	0	

Table 13-20. Register 19, Memory B (continued)

Name	Bit #	R/W	Reset	Default	Description
MEMB6	6	R/W	RTCPORB	0	Backup memory B
MEMB7	7	R/W	RTCPORB	0	
MEMB8	8	R/W	RTCPORB	0	
MEMB9	9	R/W	RTCPORB	0	
MEMB10	10	R/W	RTCPORB	0	
MEMB11	11	R/W	RTCPORB	0	
MEMB12	12	R/W	RTCPORB	0	
MEMB13	13	R/W	RTCPORB	0	
MEMB14	14	R/W	RTCPORB	0	
MEMB15	15	R/W	RTCPORB	0	
MEMB16	16	R/W	RTCPORB	0	
MEMB17	17	R/W	RTCPORB	0	
MEMB18	18	R/W	RTCPORB	0	
MEMB19	19	R/W	RTCPORB	0	
MEMB20	20	R/W	RTCPORB	0	
MEMB21	21	R/W	RTCPORB	0	
MEMB22	22	R/W	RTCPORB	0	
MEMB23	23	R/W	RTCPORB	0	

Table 13-21. Register 20, RTC Time

Name	Bit #	R/W	Reset	Default	Description
TOD0	0	R/W	RTCPORB	0	Time of day counter
TOD1	1	R/W	RTCPORB	0	
TOD2	2	R/W	RTCPORB	0	
TOD3	3	R/W	RTCPORB	0	
TOD4	4	R/W	RTCPORB	0	
TOD5	5	R/W	RTCPORB	0	
TOD6	6	R/W	RTCPORB	0	
TOD7	7	R/W	RTCPORB	0	
TOD8	8	R/W	RTCPORB	0	
TOD9	9	R/W	RTCPORB	0	
TOD10	10	R/W	RTCPORB	0	
TOD11	11	R/W	RTCPORB	0	

Table 13-21. Register 20, RTC Time (continued)

Name	Bit #	R/W	Reset	Default	Description
TOD12	12	R/W	RTCPORB	0	Time of day counter
TOD13	13	R/W	RTCPORB	0	
TOD14	14	R/W	RTCPORB	0	
TOD15	15	R/W	RTCPORB	0	
TOD16	16	R/W	RTCPORB	0	
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-22. Register 21, RTC Alarm

Name	Bit #	R/W	Reset	Default	Description
TODA0	0	R/W	RTCPORB	1	Time of day alarm
TODA1	1	R/W	RTCPORB	1	
TODA2	2	R/W	RTCPORB	1	
TODA3	3	R/W	RTCPORB	1	
TODA4	4	R/W	RTCPORB	1	
TODA5	5	R/W	RTCPORB	1	
TODA6	6	R/W	RTCPORB	1	
TODA7	7	R/W	RTCPORB	1	
TODA8	8	R/W	RTCPORB	1	
TODA9	9	R/W	RTCPORB	1	
TODA10	10	R/W	RTCPORB	1	
TODA11	11	R/W	RTCPORB	1	
TODA12	12	R/W	RTCPORB	1	
TODA13	13	R/W	RTCPORB	1	
TODA14	14	R/W	RTCPORB	1	
TODA15	15	R/W	RTCPORB	1	
TODA16	16	R/W	RTCPORB	1	
Unused	17	R	—	0	Not available

Table 13-22. Register 21, RTC Alarm (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-23. Register 22, RTC Day

Name	Bit #	R/W	Reset	Default	Description
DAY0	0	R/W	RTCPORB	0	Day counter
DAY1	1	R/W	RTCPORB	0	
DAY2	2	R/W	RTCPORB	0	
DAY3	3	R/W	RTCPORB	0	
DAY4	4	R/W	RTCPORB	0	
DAY5	5	R/W	RTCPORB	0	
DAY6	6	R/W	RTCPORB	0	
DAY7	7	R/W	RTCPORB	0	
DAY8	8	R/W	RTCPORB	0	
DAY9	9	R/W	RTCPORB	0	
DAY10	10	R/W	RTCPORB	0	
DAY11	11	R/W	RTCPORB	0	
DAY12	12	R/W	RTCPORB	0	
DAY13	13	R/W	RTCPORB	0	
DAY14	14	R/W	RTCPORB	0	
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-24. Register 23, RTC Day Alarm

Name	Bit #	R/W	Reset	Default	Description
DAYA0	0	R/W	RTCPORB	1	Day alarm
DAYA1	1	R/W	RTCPORB	1	
DAYA2	2	R/W	RTCPORB	1	
DAYA3	3	R/W	RTCPORB	1	
DAYA4	4	R/W	RTCPORB	1	
DAYA5	5	R/W	RTCPORB	1	
DAYA6	6	R/W	RTCPORB	1	
DAYA7	7	R/W	RTCPORB	1	
DAYA8	8	R/W	RTCPORB	1	
DAYA9	9	R/W	RTCPORB	1	
DAYA10	10	R/W	RTCPORB	1	
DAYA11	11	R/W	RTCPORB	1	
DAYA12	12	R/W	RTCPORB	1	
DAYA13	13	R/W	RTCPORB	1	
DAYA14	14	R/W	RTCPORB	1	
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-25. Register 24, Switchers 0

Name	Bit #	R/W	Reset	Default	Description
SW1A0	0	R/W	NONE	*	SW1A setting
SW1A1	1	R/W	NONE	*	
SW1A2	2	R/W	NONE	*	
SW1A3	3	R/W	NONE	*	
SW1A4	4	R/W	NONE	*	
SW1A5	5	R/W	NONE	*	

Table 13-25. Register 24, Switchers 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
SW1ADVS0	6	R/W	NONE	*	SW1A setting in DVS
SW1ADVS1	7	R/W	NONE	*	
SW1ADVS2	8	R/W	NONE	*	
SW1ADVS3	9	R/W	NONE	*	
SW1ADVS4	10	R/W	NONE	*	
SW1ADVS5	11	R/W	NONE	*	
SW1ASTBY0	12	R/W	NONE	*	SW1A setting in standby
SW1ASTBY1	13	R/W	NONE	*	
SW1ASTBY2	14	R/W	NONE	*	
SW1ASTBY3	15	R/W	NONE	*	
SW1ASTBY4	16	R/W	NONE	*	
SW1ASTBY5	17	R/W	NONE	*	
Reserved	18	R/W	RESETB	0	For future use
Reserved	19	R/W	RESETB	0	For future use
Reserved	20	R/W	RESETB	0	For future use
Reserved	21	R/W	RESETB	0	For future use
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 13-26. Register 25, Switchers 1

Name	Bit #	R/W	Reset	Default	Description
SW1B0	0	R/W	NONE	*	SW1B setting
SW1B1	1	R/W	NONE	*	
SW1B2	2	R/W	NONE	*	
SW1B3	3	R/W	NONE	*	
SW1B4	4	R/W	NONE	*	
SW1B5	5	R/W	NONE	*	
SW1BDVS0	6	R/W	NONE	*	SW1B setting in DVS
SW1BDVS1	7	R/W	NONE	*	
SW1BDVS2	8	R/W	NONE	*	
SW1BDVS3	9	R/W	NONE	*	
SW1BDVS4	10	R/W	NONE	*	
SW1BDVS5	11	R/W	NONE	*	

Table 13-26. Register 25, Switchers 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
SW1BSTBY0	12	R/W	NONE	*	SW1B setting in standby
SW1BSTBY1	13	R/W	NONE	*	
SW1BSTBY2	14	R/W	NONE	*	
SW1BSTBY3	15	R/W	NONE	*	
SW1BSTBY4	16	R/W	NONE	*	
SW1BSTBY5	17	R/W	NONE	*	
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-27. Register 26, Switchers 2

Name	Bit #	R/W	Reset	Default	Description
SW2A0	0	R/W	NONE	*	SW2A setting
SW2A1	1	R/W	NONE	*	
SW2A2	2	R/W	NONE	*	
SW2A3	3	R/W	NONE	*	
SW2A4	4	R/W	NONE	*	
SW2A5	5	R/W	NONE	*	
SW2ADVS0	6	R/W	NONE	*	SW2A setting in DVS
SW2ADVS1	7	R/W	NONE	*	
SW2ADVS2	8	R/W	NONE	*	
SW2ADVS3	9	R/W	NONE	*	
SW2ADVS4	10	R/W	NONE	*	
SW2ADVS5	11	R/W	NONE	*	
SW2ASTBY0	12	R/W	NONE	*	SW2A setting in standby
SW2ASTBY1	13	R/W	NONE	*	
SW2ASTBY2	14	R/W	NONE	*	
SW2ASTBY3	15	R/W	NONE	*	
SW2ASTBY4	16	R/W	NONE	*	
SW2ASTBY5	17	R/W	NONE	*	

Table 13-27. Register 26, Switchers 2 (continued)

Reserved	18	R/W	RESETB	0	For future use
Reserved	19	R/W	RESETB	0	For future use
Reserved	20	R/W	RESETB	0	For future use
Reserved	21	R/W	RESETB	0	For future use
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 13-28. Register 27, Switchers 3

Name	Bit #	R/W	Reset	Default	Description
SW2B0	0	R/W	NONE	*	SW2B setting
SW2B1	1	R/W	NONE	*	
SW2B2	2	R/W	NONE	*	
SW2B3	3	R/W	NONE	*	
SW2B4	4	R/W	NONE	*	
SW2B5	5	R/W	NONE	*	
SW2BDVS0	6	R/W	NONE	*	SW2B setting in DVS
SW2BDVS1	7	R/W	NONE	*	
SW2BDVS2	8	R/W	NONE	*	
SW2BDVS3	9	R/W	NONE	*	
SW2BDVS4	10	R/W	NONE	*	
SW2BDVS5	11	R/W	NONE	*	
SW2BSTBY0	12	R/W	NONE	*	SW2B setting in standby
SW2BSTBY1	13	R/W	NONE	*	
SW2BSTBY2	14	R/W	NONE	*	
SW2BSTBY3	15	R/W	NONE	*	
SW2BSTBY4	16	R/W	NONE	*	
SW2BSTBY5	17	R/W	NONE	*	
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-29. Register 28, Switchers 4

Name	Bit #	R/W	Reset	Default	Description
SW1AMODE0	0	R/W	NONE	*	SW1A operating mode
SW1AMODE1	1	R/W	RESETB	0	
SW1ASTBYMODE0	2	R/W	NONE	*	SW1A operating mode in standby
SW1ASTBYMODE1	3	R/W	RESETB	0	
Reserved	4	R/W	RESETB	0	For future use
Reserved	5	R/W	RESETB	0	For future use
SW1ADVSSPEED0	6	R/W	RESETB	0	SW1A DVS speed setting
SW1ADVSSPEED1	7	R/W	RESETB	0	
SW1APANIC	8	R/W	RESETB	0	SW1A panic mode enable
SW1ASFST	9	R/W	RESETB	1	SW1A softstart
SW1BMODE0	10	R/W	NONE	*	SW1B operating mode
SW1BMODE1	11	R/W	RESETB	0	
SW1BSTBYMODE0	12	R/W	NONE	*	SW1B operating mode in standby
SW1BSTBYMODE1	13	R/W	RESETB	0	
SW1BDVSSPEED0	14	R/W	RESETB	0	SW1B DVS speed setting
SW1BDVSSPEED1	15	R/W	RESETB	0	
SW1BPANIC	16	R/W	RESETB	0	SW1B panic mode enable
SW1BSFST	17	R/W	RESETB	1	SW1B softstart
PLLEN	18	R/W	RESETB	0	Switcher PLL enable
PLLX0	19	R/W	RESETB	0	Switcher PLL multiplication factor
PLLX1	20	R/W	RESETB	0	
PLLX2	21	R/W	RESETB	1	
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 13-30. Register 29, Switchers 5

Name	Bit #	R/W	Reset	Default	Description
SW2AMODE0	0	R/W	NONE	*	SW2A operating mode
SW2AMODE1	1	R/W	RESETB	0	
SW2ASTBYMODE0	2	R/W	NONE	*	SW2A operating mode in standby
SW2ASTBYMODE1	3	R/W	RESETB	0	
Reserved	4	R/W	RESETB	0	For future use
Reserved	5	R/W	RESETB	0	For future use

Table 13-30. Register 29, Switchers 5 (continued)

Name	Bit #	R/W	Reset	Default	Description
SW2ADVSSPEED0	6	R/W	RESETB	0	SW2A DVS speed setting
SW2ADVSSPEED1	7	R/W	RESETB	0	
SW2APANIC	8	R/W	RESETB	0	SW2A panic mode enable
SW2ASFST	9	R/W	RESETB	1	SW2A softstart
SW2BMODE0	10	R/W	NONE	*	SW2B operating mode
SW2BMODE1	11	R/W	RESETB	0	
SW2BSTBYMODE0	12	R/W	NONE	*	SW2B operating mode in standby
SW2BSTBYMODE1	13	R/W	RESETB	0	
SW2BDVSSPEED0	14	R/W	RESETB	0	SW2B DVS speed setting
SW2BDVSSPEED1	15	R/W	RESETB	0	
SW2BPANIC	16	R/W	RESETB	0	SW2B panic mode enable
SW2BSFST	17	R/W	RESETB	1	SW2B softstart
SW30	18	R/W	NONE	*	SW3 setting
SW31	19	R/W	NONE	*	
SW3EN	20	R/W	NONE	*	SW3 enable
SW3STBY	21	R/W	RESETB	0	SW3 controlled by standby
SW3MODE	22	R/W	RESETB	0	SW3 operating mode
Reserved	23	R/W	RESETB	0	For future use

Table 13-31. Register 30, Regulator Setting 0

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R/W	RESETB	0	For future use
Reserved	1	R/W	RESETB	0	For future use
VIOLO0	2	R/W	NONE	*	VIOLO setting
VIOLO1	3	R/W	NONE	*	
VDIG0	4	R/W	NONE	*	VDIG setting
VDIG1	5	R/W	NONE	*	
VGEN0	6	R/W	NONE	*	VGEN setting
VGEN1	7	R/W	NONE	*	
VGEN2	8	R/W	NONE	*	
VRFDIG0	9	R/W	NONE	*	VRFDIG setting
VRFDIG1	10	R/W	NONE	*	

Table 13-31. Register 30, Regulator Setting 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
VRFREF0	11	R/W	NONE	*	VRFREF setting
VRFREF1	12	R/W	NONE	*	
VRFCP	13	R/W	NONE	*	VRFCP setting
VSIM	14	R/W	NONE	*	VSIM setting
VESIM	15	R/W	NONE	*	VESIM setting
VCAM0	16	R/W	NONE	*	VCAM setting
VCAM1	17	R/W	NONE	*	
VCAM2	18	R/W	NONE	*	
Reserved	19	R/W	RESETB	0	For future use
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-32. Register 31, Regulator Setting 1

Name	Bit #	R/W	Reset	Default	Description
VVIB0	0	R/W	RESETB	0	VVIB setting
VVIB1	1	R/W	RESETB	0	
VRF10	2	R/W	NONE	*	VRF1 setting
VRF11	3	R/W	NONE	*	
VRF20	4	R/W	NONE	*	VRF2 setting
VRF21	5	R/W	NONE	*	
VMMC10	6	R/W	NONE	*	VMMC1 setting
VMMC11	7	R/W	NONE	*	
VMMC12	8	R/W	NONE	*	
VMMC20	9	R/W	NONE	*	VMMC2 setting
VMMC21	10	R/W	NONE	*	
VMMC22	11	R/W	NONE	*	
Reserved	12	R/W	RESETB	0	For future use
Reserved	13	R/W	RESETB	0	For future use
Reserved	14	R/W	RESETB	0	For future use
Reserved	15	R/W	RESETB	0	For future use
Unused	16	R	—	0	Not available

Table 13-32. Register 31, Regulator Setting 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-33. Register 32, Regulator Mode 0

Name	Bit #	R/W	Reset	Default	Description
VAUDIOEN	0	R/W	NONE	*	VAUDIO enable
VAUDIOSTBY	1	R/W	RESETB	0	VAUDIO controlled by standby
VAUDIOMODE	2	R/W	RESETB	0	VAUDIO operating mode
VIOHIEN	3	R/W	NONE	*	VIOHI enable
VIOHISTBY	4	R/W	RESETB	0	VIOHI controlled by standby
VIOHIMODE	5	R/W	RESETB	0	VIOHI operating mode
VIOLOEN	6	R/W	NONE	*	VIOLO enable
VIOLOSTBY	7	R/W	RESETB	0	VIOLO controlled by standby
VIOLOMODE	8	R/W	RESETB	0	VIOLO operating mode
VDIGEN	9	R/W	NONE	*	VDIG enable
VDIGSTBY	10	R/W	RESETB	0	VDIG controlled by standby
VDIGMODE	11	R/W	RESETB	0	VDIG operating mode
VGENEN	12	R/W	NONE	*	VGEN enable
VGENSTBY	13	R/W	RESETB	0	VGEN controlled by standby
VGENMODE	14	R/W	RESETB	0	VGEN operating mode
VRFDIGEN	15	R/W	NONE	*	VRFDIG enable
VRFDIGSTBY	16	R/W	RESETB	0	VRFDIG controlled by standby
VRFDIGMODE	17	R/W	RESETB	0	VRFDIG operating mode
VRFREFEN	18	R/W	NONE	*	VRFREF enable
VRFREFSTBY	19	R/W	RESETB	0	VRFREF controlled by standby
VRFREFMODE	20	R/W	RESETB	0	VRFREF operating mode
VRFCPEN	21	R/W	NONE	*	VRFCP enable

Table 13-33. Register 32, Regulator Mode 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
VRFCPSTBY	22	R/W	RESETB	0	VRFCP controlled by standby
VRFCPMODE	23	R/W	RESETB	0	VRFCP operating mode

Table 13-34. Register 33, Regulator Mode 1

Name	Bit #	R/W	Reset	Default	Description
VSIMEN	0	R/W	NONE	*	VSIM enable
VSIMSTBY	1	R/W	RESETB	0	VSIM controlled by standby
VSIMMODE	2	R/W	RESETB	0	VSIM operating mode
VESIMEN	3	R/W	NONE	*	VESIM enable
VESIMSTBY	4	R/W	RESETB	0	VESIM controlled by standby
VESIMMODE	5	R/W	RESETB	0	VESIM operating mode
VCAMEN	6	R/W	NONE	*	VCAM enable
VCAMSTBY	7	R/W	RESETB	0	VCAM controlled by standby
VCAMMODE	8	R/W	RESETB	0	VCAM operating mode
VRFBGEN	9	R/W	NONE	*	VRFBG enable
VRFBGSTBY	10	R/W	RESETB	0	VRFBG controlled by standby
VVIBEN	11	R/W	RESETB	0	VVIB enable
VRF1EN	12	R/W	NONE	*	VRF1 enable
VRF1STBY	13	R/W	RESETB	0	VRF1 controlled by standby
VRF1MODE	14	R/W	RESETB	0	VRF1 operating mode
VRF2EN	15	R/W	NONE	*	VRF2 enable
VRF2STBY	16	R/W	RESETB	0	VRF2 controlled by standby
VRF2MODE	17	R/W	RESETB	0	VRF2 operating mode
VMMC1EN	18	R/W	NONE	*	VMMC1 enable
VMMC1STBY	19	R/W	RESETB	0	VMMC1 controlled by standby
VMMC1MODE	20	R/W	RESETB	0	VMMC1 operating mode
VMMC2EN	21	R/W	NONE	*	VMMC2 enable
VMMC2STBY	22	R/W	RESETB	0	VMMC2 controlled by standby
VMMC2MODE	23	R/W	RESETB	0	VMMC2 operating mode

Table 13-35. Register 34, Power Miscellaneous

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R/W	RESETB	0	For future use
Reserved	1	R/W	RESETB	0	For future use
Reserved	2	R/W	RESETB	0	For future use
Reserved	3	R/W	RESETB	0	For future use
Reserved	4	R/W	RESETB	0	For future use
Reserved	5	R/W	RESETB	0	For future use
GPO1EN	6	R/W	RESETB	0	GPO1 enable
GPO1STBY	7	R/W	RESETB	0	GPO1 controlled by standby
GPO2EN	8	R/W	RESETB	0	GPO2 enable
GPO2STBY	9	R/W	RESETB	0	GPO2 controlled by standby
GPO3EN	10	R/W	RESETB	0	GPO3 enable
GPO3STBY	11	R/W	RESETB	0	GPO3 controlled by standby
GPO4EN	12	R/W	RESETB	0	GPO4 enable
GPO4STBY	13	R/W	RESETB	0	GPO4 controlled by standby
VIBPINCTRL	14	R/W	RESETB	0	Enables control of VVIB by VIBEN pin
PWGT1SPIEN	15	R/W	RESETB	0	Power gate 1 enable
PWGT2SPIEN	16	R/W	RESETB	0	Power gate 2 enable
Reserved	17	R/W	RESETB	0	For future use
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-36. Register 35, Power Spare

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R	—	0	Not available
Unused	1	R	—	0	Not available
Unused	2	R	—	0	Not available
Unused	3	R	—	0	Not available
Unused	4	R	—	0	Not available
Unused	5	R	—	0	Not available

Table 13-36. Register 35, Power Spare (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	6	R	—	0	Not available
Unused	7	R	—	0	Not available
Unused	8	R	—	0	Not available
Unused	9	R	—	0	Not available
Unused	10	R	—	0	Not available
Unused	11	R	—	0	Not available
Unused	12	R	—	0	Not available
Unused	13	R	—	0	Not available
Unused	14	R	—	0	Not available
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-37. Register 36, Audio Rx 0

Name	Bit #	R/W	Reset	Default	Description
VAUDIOON	0	R/W	RESETB	0	Forces VAUDIO in active on mode
BIASEN	1	R/W	RESETB	0	Audio bias enable
BIASSPEED	2	R/W	RESETB	0	Turn on ramp speed of the audio bias
ASPEN	3	R/W	RESETB	0	Amplifier Asp enable
ASPSEL	4	R/W	RESETB	0	Asp input selector
ALSPEN	5	R/W	RESETB	0	Amplifier Alsp enable
ALSPREF	6	R/W	RESETB	0	Bias Alsp at common audio reference
ALSPSEL	7	R/W	RESETB	0	Alsp input selector
LSPLEN	8	R/W	RESETB	0	Output LSPL enable
AHSREN	9	R/W	RESETB	0	Amplifier AhsR enable
AHSLEN	10	R/W	RESETB	0	Amplifier AhsL enable
AHSSEL	11	R/W	RESETB	0	Ahsr and Ahsl input selector

Table 13-37. Register 36, Audio Rx 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
HSPGDIS	12	R/W	RESETB	1	Phantom ground disable
HSDETEN	13	R/W	RESETB	0	Headset detect enable
HSDETAUTOB	14	R/W	RESETB	0	Amplifier state determined by headset detect
ARXOUTREN	15	R/W	RESETB	0	Output RXOUTR enable
ARXOUTLEN	16	R/W	RESETB	0	Output RXOUTL enable
ARXOUTSEL	17	R/W	RESETB	0	Arxout input selector
CDCOUTEN	18	R/W	RESETB	0	Output CDCOUT enable
HSLDETEN	19	R/W	RESETB	0	Headset left channel detect enable
Reserved	20	R/W	RESETB	0	For future use
ADDCDC	21	R/W	RESETB	0	Adder channel CODEC selection
ADDSTDC	22	R/W	RESETB	0	Adder channel stereo DAC selection
ADDRXIN	23	R/W	RESETB	0	Adder channel line in selection

Table 13-38. Register 37, Audio Rx 1

Name	Bit #	R/W	Reset	Default	Description
PGARXEN	0	R/W	RESETB	0	CODEC receive PGA enable
PGARX0	1	R/W	RESETB	1	CODEC receive gain setting
PGARX1	2	R/W	RESETB	0	
PGARX2	3	R/W	RESETB	1	
PGARX3	4	R/W	RESETB	1	
PGASTEN	5	R/W	RESETB	0	Stereo DAC PGA enable
PGAST0	6	R/W	RESETB	1	Stereo DAC gain setting
PGAST1	7	R/W	RESETB	0	
PGAST2	8	R/W	RESETB	1	
PGAST3	9	R/W	RESETB	1	
ARXINEN	10	R/W	RESETB	0	Amplifier Arx enable
ARXIN	11	R/W	RESETB	0	Amplifier Arx additional gain setting
PGARXIN0	12	R/W	RESETB	1	PGArxin gain setting
PGARXIN1	13	R/W	RESETB	0	
PGARXIN2	14	R/W	RESETB	1	
PGARXIN3	15	R/W	RESETB	1	
MONO0	16	R/W	RESETB	0	Mono adder setting
MONO1	17	R/W	RESETB	0	

Table 13-38. Register 37, Audio Rx 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
BAL0	18	R/W	RESETB	0	Balance control
BAL1	19	R/W	RESETB	0	
BAL2	20	R/W	RESETB	0	
BALLR	21	R/W	RESETB	0	Left / right balance
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-39. Register 38, Audio Tx

Name	Bit #	R/W	Reset	Default	Description
MC1BEN	0	R/W	RESETB	0	Microphone bias 1 enable
MC2BEN	1	R/W	RESETB	0	Microphone bias 2 enable
MC2BDETDBNC	2	R/W	RESETB	0	Microphone bias detect debounce setting
MC2BDETEN	3	R/W	RESETB	0	Microphone bias 2 detect enable
Reserved	4	R/W	RESETB	0	For future use
AMC1REN	5	R/W	RESETB	0	Amplifier Amc1R enable
AMC1RITOV	6	R/W	RESETB	0	Amplifier Amc1R current to voltage mode enable
AMC1LEN	7	R/W	RESETB	0	Amplifier Amc1L enable
AMC1LITOV	8	R/W	RESETB	0	Amplifier Amc1L current to voltage mode enable
AMC2EN	9	R/W	RESETB	0	Amplifier Amc2 enable
AMC2ITOV	10	R/W	RESETB	0	Amplifier Amc2 current to voltage mode enable
ATXINEN	11	R/W	RESETB	0	Amplifier Atxin enable
ATXOUTEN	12	R/W	RESETB	0	Reserved for output TXOUT enable, currently not used
RXINREC	13	R/W	RESETB	0	RXINR/RXINL to voice CODEC ADC routing enable
PGATXR0	14	R/W	RESETB	0	Transmit gain setting right
PGATXR1	15	R/W	RESETB	0	
PGATXR2	16	R/W	RESETB	0	
PGATXR3	17	R/W	RESETB	1	
PGATXR4	18	R/W	RESETB	0	
PGATXL0	19	R/W	RESETB	0	Transmit gain setting left
PGATXL1	20	R/W	RESETB	0	
PGATXL2	21	R/W	RESETB	0	
PGATXL3	22	R/W	RESETB	1	
PGATXL4	23	R/W	RESETB	0	

Table 13-40. Register 39, SSI Network

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R/W	RESETB	0	For future use
Reserved	1	R/W	RESETB	0	For future use
CDCTXRXSLOT0	2	R/W	RESETB	0	CODEC time slot assignment
CDCTXRXSLOT1	3	R/W	RESETB	0	
CDCTXSECSLOT0	4	R/W	RESETB	0	CODEC secondary transmit time slot
CDCTXSECSLOT1	5	R/W	RESETB	1	
CDCRXSECSLOT0	6	R/W	RESETB	1	CODEC secondary receive time slot
CDCRXSECSLOT1	7	R/W	RESETB	0	
CDCRXSECGAIN0	8	R/W	RESETB	0	CODEC secondary receive channel gain setting
CDCRXSECGAIN1	9	R/W	RESETB	0	
CDCSUMGAIN	10	R/W	RESETB	0	CODEC summed receive signal gain setting
CDCFSDLY	11	R/W	RESETB	0	CODEC framesync delay
STDCSLOTS0	12	R/W	RESETB	1	Stereo DAC number of time slots select
STDCSLOTS1	13	R/W	RESETB	1	
STDCRXSLOT0	14	R/W	RESETB	0	Stereo DAC time slot assignment
STDCRXSLOT1	15	R/W	RESETB	0	
STDCRXSECSLOT0	16	R/W	RESETB	1	Stereo DAC secondary receive time slot
STDCRXSECSLOT1	17	R/W	RESETB	0	
STDCRXSECGAIN0	18	R/W	RESETB	0	Stereo DAC secondary receive channel gain setting
STDCRXSECGAIN1	19	R/W	RESETB	0	
STDCSUMGAIN	20	R/W	RESETB	0	Stereo DAC summed receive signal gain setting
Reserved	21	R/W	RESETB	0	For future use
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-41. Register 40, Audio CODEC

Name	Bit #	R/W	Reset	Default	Description
CDCSSISEL	0	R/W	RESETB	1	CODEC SSI bus select
CDCCLKSEL	1	R/W	RESETB	1	CODEC clock input select
CDCSM	2	R/W	RESETB	1	CODEC slave / master select
CDCBCLINV	3	R/W	RESETB	0	CODEC bit clock inversion
CDCFSINV	4	R/W	RESETB	0	CODEC framesync inversion

Table 13-41. Register 40, Audio CODEC (continued)

Name	Bit #	R/W	Reset	Default	Description
CDCFS0	5	R/W	RESETB	1	Bus protocol selection
CDCFS1	6	R/W	RESETB	0	
CDCCLK0	7	R/W	RESETB	0	CODEC clock setting
CDCCLK1	8	R/W	RESETB	0	
CDCCLK2	9	R/W	RESETB	0	
CDCFS8K16K	10	R/W	RESETB	0	CODEC framesync select
CDCEN	11	R/W	RESETB	0	CODEC enable
CDCCLKEN	12	R/W	RESETB	0	CODEC clocking enable
CDCTS	13	R/W	RESETB	0	CODEC SSI tristate
CDCDITH	14	R/W	RESETB	0	CODEC dithering
CDCRESET	15	R/W	RESETB	0	CODEC filter reset
CDCBYP	16	R/W	RESETB	0	CODEC bypass
CDCALM	17	R/W	RESETB	0	CODEC analog loopback
CDCDLM	18	R/W	RESETB	0	CODEC digital loopback
AUDIHPF	19	R/W	RESETB	1	Transmit high pass filter enable
AUDOHPF	20	R/W	RESETB	1	Receive high pass filter enable
Unused	21	R/W	RESETB	0	Not available
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Table 13-42. Register 41, Audio Stereo DAC

Name	Bit #	R/W	Reset	Default	Description
STDCSSISEL	0	R/W	RESETB	0	Stereo DAC SSI bus select
STDCCLKSEL	1	R/W	RESETB	0	Stereo DAC clock input select
STDCSM	2	R/W	RESETB	1	Stereo DAC slave / master select
STDCBCLINV	3	R/W	RESETB	0	Stereo DAC bit clock inversion
STDCFSINV	4	R/W	RESETB	0	Stereo DAC framesync inversion
STDCFS0	5	R/W	RESETB	0	Bus protocol selection
STDCFS1	6	R/W	RESETB	0	
STDCCLK0	7	R/W	RESETB	0	Stereo DAC clock setting
STDCCLK1	8	R/W	RESETB	0	
STDCCLK2	9	R/W	RESETB	0	
STDCFSDLYB	10	R/W	RESETB	0	Stereo DAC framesync delay bar

Table 13-42. Register 41, Audio Stereo DAC (continued)

Name	Bit #	R/W	Reset	Default	Description
STDCEN	11	R/W	RESETB	0	Stereo DAC enable
STDCCLKEN	12	R/W	RESETB	0	Stereo DAC clocking enable
Reserved	13	R/W	RESETB	0	For future use
Reserved	14	R/W	RESETB	0	For future use
STDCRESET	15	R/W	RESETB	0	Stereo DAC filter reset
SPDIF	16	R/W	RESETB	0	Stereo DAC SSI SPDIF mode. Mode no longer available.
SR0	17	R/W	RESETB	1	Stereo DAC sample rate
SR1	18	R/W	RESETB	1	
SR2	19	R/W	RESETB	1	
SR3	20	R/W	RESETB	0	
Unused	21	R/W	RESETB	0	Not available
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Table 13-43. Register 42, Audio Spare

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R	—	0	Not available
Unused	1	R	—	0	Not available
Unused	2	R	—	0	Not available
Unused	3	R	—	0	Not available
Unused	4	R	—	0	Not available
Unused	5	R	—	0	Not available
Unused	6	R	—	0	Not available
Unused	7	R	—	0	Not available
Unused	8	R	—	0	Not available
Unused	9	R	—	0	Not available
Unused	10	R	—	0	Not available
Unused	11	R	—	0	Not available
Unused	12	R	—	0	Not available
Unused	13	R	—	0	Not available
Unused	14	R	—	0	Not available
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available

Table 13-43. Register 42, Audio Spare (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-44. Register 43, ADC 0

Name	Bit #	R/W	Reset	Default	Description
LICELLCON	0	R/W	RESETB	0	Enables lithium cell reading
CHRGICON	1	R/W	RESETB	0	Enables charge current reading
BATICON	2	R/W	RESETB	0	Enables battery current reading
RTHEN	3	R/W	RESETB	0	Enables thermistor reading
DTHEN	4	R/W	RESETB	0	Enables die temperature reading
UIDEN	5	R/W	RESETB	0	Enables UID reading
ADOUTEN	6	R/W	RESETB	0	Enables the pulse at the ADOUT pin
ADOUTPER	7	R/W	RESETB	0	Sets the ADOUT period
Reserved	8	R/W	RESETB	0	For future use
Reserved	9	R/W	RESETB	0	For future use
ADREFEN	10	R/W	RESETB	0	Enables the touchscreen reference
ADREFMODE	11	R/W	RESETB	0	Sets the touchscreen reference mode
TSMOD0	12	R/W	RESETB	0	Sets the touchscreen mode
TSMOD1	13	R/W	RESETB	0	
TSMOD2	14	R/W	RESETB	0	
CHRGRAWDIV	15	R/W	RESETB	1	Sets CHRGRAW scaling to divide by 5
ADINC1	16	R/W	RESETB	0	Auto increment for ADA1
ADINC2	17	R/W	RESETB	0	Auto increment for ADA2
WCOMP	18	R/W	RESETB	0	Normal conversion mode with limit comparison
Reserved	19	R/W	RESETB	0	For future use
Reserved	20	R/W	RESETB	0	For future use
Unused	21	R	—	0	Not available

Table 13-44. Register 43, ADC 0

Name	Bit #	R/W	Reset	Default	Description
Unused	22	R	—	0	Not available
ADCBIS0	23	W	—	0	Access to the ADCBIS control

Table 13-45. Register 44, ADC 1

Name	Bit #	R/W	Reset	Default	Description
ADEN	0	R/W	RESETB	0	Enables the ADC
RAND	1	R/W	RESETB	0	Sets the single channel mode
Reserved	2	R/W	RESETB	0	For future use
ADSEL	3	R/W	RESETB	0	Selects the set of inputs
TRIGMASK	4	R/W	RESETB	0	Trigger event masking
ADA10	5	R/W	RESETB	0	Channel selection 1
ADA11	6	R/W	RESETB	0	
ADA12	7	R/W	RESETB	0	
ADA20	8	R/W	RESETB	0	Channel selection 2
ADA21	9	R/W	RESETB	0	
ADA22	10	R/W	RESETB	0	
ATO0	11	R/W	RESETB	0	Delay before first conversion
ATO1	12	R/W	RESETB	0	
ATO2	13	R/W	RESETB	0	
ATO3	14	R/W	RESETB	0	
ATO4	15	R/W	RESETB	0	
ATO5	16	R/W	RESETB	0	
ATO6	17	R/W	RESETB	0	
ATO7	18	R/W	RESETB	0	
ATOX	19	R/W	RESETB	0	Sets ATO delay for any conversion
ASC	20	R/W	RESETB	0	Starts conversion
ADTRIGIGN	21	R/W	RESETB	0	Ignores the ADTRIG input
ADONESHOT	22	R/W	RESETB	0	Single trigger event only
ADCBIS1	23	W	RESETB	0	Access to the ADCBIS control

Table 13-46. Register 45, ADC 2

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R	NONE	0	For future 12 bit use
Reserved	1	R	NONE	0	
ADD10	2	R	NONE	0	Results for channel selection 1
ADD11	3	R	NONE	0	
ADD12	4	R	NONE	0	
ADD13	5	R	NONE	0	
ADD14	6	R	NONE	0	
ADD15	7	R	NONE	0	
ADD16	8	R	NONE	0	
ADD17	9	R	NONE	0	
ADD18	10	R	NONE	0	
ADD19	11	R	NONE	0	
Reserved	12	R	NONE	0	For future 12 bit use
Reserved	13	R	NONE	0	
ADD20	14	R	NONE	0	Results for channel selection 2
ADD21	15	R	NONE	0	
ADD22	16	R	NONE	0	
ADD23	17	R	NONE	0	
ADD24	18	R	NONE	0	
ADD25	19	R	NONE	0	
ADD26	20	R	NONE	0	
ADD27	21	R	NONE	0	
ADD28	22	R	NONE	0	
ADD29	23	R	NONE	0	

Table 13-47. Register 46, ADC 3

Name	Bit #	R/W	Reset	Default	Description
WHIGH0	0	R/W	RESETB	0	Comparator high level in WCOMP mode
WHIGH1	1	R/W	RESETB	0	
WHIGH2	2	R/W	RESETB	0	
WHIGH3	3	R/W	RESETB	0	
WHIGH4	4	R/W	RESETB	0	
WHIGH5	5	R/W	RESETB	0	

Table 13-47. Register 46, ADC 3 (continued)

Name	Bit #	R/W	Reset	Default	Description
ICID0	6	R/W	NONE	0	MC13783 derivative
ICID1	7	R/W	NONE	1	
ICID2	8	R/W	NONE	0	
WLOW0	9	R/W	RESETB	0	Comparator low level in WCOMP mode
WLOW1	10	R/W	RESETB	0	
WLOW2	11	R/W	RESETB	0	
WLOW3	12	R/W	RESETB	0	
WLOW4	13	R/W	RESETB	0	
WLOW5	14	R/W	RESETB	0	
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
ADCBIS2	23	W	RESETB	0	Access to the ADCBIS control

Table 13-48. Register 47, ADC 4

Name	Bit #	R/W	Reset	Default	Description
Reserved	0	R	NONE	0	For future 12 bit use
Reserved	1	R	NONE	0	
ADDBIS10	2	R	NONE	0	Result for channel selection 1 of ADCBIS
ADDBIS11	3	R	NONE	0	
ADDBIS12	4	R	NONE	0	
ADDBIS13	5	R	NONE	0	
ADDBIS14	6	R	NONE	0	
ADDBIS15	7	R	NONE	0	
ADDBIS16	8	R	NONE	0	
ADDBIS17	9	R	NONE	0	
ADDBIS18	10	R	NONE	0	
ADDBIS19	11	R	NONE	0	

Table 13-48. Register 47, ADC 4 (continued)

Name	Bit #	R/W	Reset	Default	Description
Reserved	12	R	NONE	0	For future 12 bit use
Reserved	13	R	NONE	0	
ADDBIS20	14	R	NONE	0	Result for channel selection 2 of ADCBIS
ADDBIS21	15	R	NONE	0	
ADDBIS22	16	R	NONE	0	
ADDBIS23	17	R	NONE	0	
ADDBIS24	18	R	NONE	0	
ADDBIS25	19	R	NONE	0	
ADDBIS26	20	R	NONE	0	
ADDBIS27	21	R	NONE	0	
ADDBIS28	22	R	NONE	0	
ADDBIS29	23	R	NONE	0	

Table 13-49. Register 48, Charger 0

Name	Bit #	R/W	Reset	Default	Description
VCHRG0	0	R/W	RESETB	0	Sets the charge regulator output voltage
VCHRG1	1	R/W	RESETB	0	
VCHRG2	2	R/W	RESETB	0	
ICHRG0	3	R/W	RESETB	0	Sets the main charger DAC current
ICHRG1	4	R/W	RESETB	0	
ICHRG2	5	R/W	RESETB	0	
ICHRG3	6	R/W	RESETB	0	
ICHRGTR0	7	R/W	RESETB	0	Sets the internal trickle charger current
ICHRGTR1	8	R/W	RESETB	0	
ICHRGTR2	9	R/W	RESETB	0	
FETOVRD	10	R/W	RESETB	0	BATTFET and BPFET control mode
FETCTRL	11	R/W	RESETB	0	BATTFET and BPFET control setting
Reserved	12	R/W	RESETB	0	For future use
RVRSMODE	13	R/W	RESETB	0	Reverse mode enable
Reserved	14	R/W	RESETB	0	For future use
OVCTRL0	15	R/W	RESETB	0	Over voltage threshold select
OVCTRL1	16	R/W	RESETB	0	
UCHEN	17	R/W	RESETB	0	Unregulated charge enable

Table 13-49. Register 48, Charger 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
CHRGLEDEN	18	R/W	RESETB	0	CHRGLED enable
CHRGRAWPDEN	19	R/W	RESETB	0	Enables a 5K pull down at CHRGRAW
Reserved	20	R/W	RESETB	0	For future use
Reserved	21	R/W	RESETB	0	For future use
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Table 13-50. Register 49, USB 0

Name	Bit #	R/W	Reset	Default	Description
FSENB	0	R/W	RESETB	0	USB full speed mode select bar
USBSUSPEND	1	R/W	RESETB	0	USB suspend mode enable
USBPU	2	R/W	RESETB	0	Switches in variable 1.5K UDP/UDM pull-up
UDPPD	3	R/W	RESETB	0	Switches in 15K UDP pull-down
UDMPD	4	R/W	RESETB	0	Switches in 15K UDM pull-down
DP150KPU	5	R/W	RESETB	1	Switches in 150K UDP pull-up
VBUS70KPDENB	6	R/W	RESETB	1	Turns off VBUS pull-down NMOS switch
VBUSPULSETMR0	7	R/W	RESETB	0	VBUS regulator current limit control
VBUSPULSETMR1	8	R/W	RESETB	0	
VBUSPULSETMR2	9	R/W	RESETB	0	
DLPSRP	10	R/W	RESETB	0	DLP Timer enable
SE0CONN	11	R/W	RESETB	0	SE0 automatically connects UDP pull-up
USBXCVREN	12	R/W	RESETB	0	USB transceiver enable
PULLOVR	13	R/W	RESETB	0	Variable pull-up / pull-downs disconnect
CONMODE0	14	R/W	RESETB	0	Connectivity Interface mode select
CONMODE1	15	R/W	RESETB	0	
CONMODE2	16	R/W	RESETB	0	
DATSE0	17	R/W	NONE	*	USB single ended / differential mode
BIDIR	18	R/W	NONE	*	USB unidirectional / bidirectional transmission
USBCNTRL	19	R/W	RESETB	1	USB transceiver and pull-up control
IDPD	20	R/W	RESETB	0	Switches in UID pull-down
IDPULSE	21	R/W	RESETB	0	Pulses UID to ground
IDPUCNTRL	22	R/W	RESETB	0	UID pin pull up source select
DMPULSE	23	R/W	RESETB	0	Generates positive pulse on the UDM line

Table 13-51. Register 50, Charger USB 1

Name	Bit #	R/W	Reset	Default	Description
VUSBIN0	0	R/W	RESETB	0	VUSB regulator input source control
VUSBIN1	1	R/W	RESETB	1	
VUSB	2	R/W	RESETB	1	VUSB output voltage setting
VUSBEN	3	R/W	NONE	*	VUSB enable
Reserved	4	R/W	RESETB	0	For future use
VBUSEN	5	R/W	NONE	*	VBUS enable
RSPOL	6	R/W	RESETB	0	Swaps TX and RX in RS232 mode
RSTRI	7	R/W	RESETB	0	Tristates TX in RS232 mode
ID100KPU	8	R/W	RESETB	0	Switches in 100K UID pull-up
Unused	9	R	—	0	Not used
Unused	10	R	—	0	Not used
Unused	11	R	—	0	Not used
Unused	12	R	—	0	Not used
Unused	13	R	—	0	Not used
Unused	14	R	—	0	Not used
Unused	15	R	—	0	Not used
Unused	16	R	—	0	Not used
Unused	17	R	—	0	Not used
Unused	18	R	—	0	Not used
Unused	19	R	—	0	Not used
Unused	20	R	—	0	Not used
Unused	21	R	—	0	Not used
Unused	22	R	—	0	Not used
Unused	23	R	—	0	Not used

Table 13-52. Register 51, LED Control 0

Name	Bit #	R/W	Reset	Default	Description
LEDEN	0	R/W	RESETB	0	Master Enable for BL and TC LED Bias
LEDMDRAMPUP	1	R/W	RESETB	0	Ramp Up Main Display Backlight channel
LEDADRAMPUP	2	R/W	RESETB	0	Ramp Up Auxiliary Display Backlight channel
LEDKPRAMPUP	3	R/W	RESETB	0	Ramp Up Key Pad Backlight channel
LEDMDRAMPDOWN	4	R/W	RESETB	0	Ramp Down Main Display Backlight channel
LEDADRAMPDOWN	5	R/W	RESETB	0	Ramp Down Auxiliary Display Backlight channel

Table 13-52. Register 51, LED Control 0 (continued)

Name	Bit #	R/W	Reset	Default	Description
LEDKPRAMPDOWN	6	R/W	RESETB	0	Ramp Down Key Pad Backlight channel
TRIODEMD	7	R/W	RESETB	0	Triode Mode for Main Display Backlight Drivers
TRIODEAD	8	R/W	RESETB	0	Triode Mode for Auxiliary Display Backlight Drivers
TRIODEKP	9	R/W	RESETB	0	Triode Mode for Key Pad Backlight Driver
BOOSTEN	10	R/W	RESETB	0	Forced enable for Boost
ABMODE0	11	R/W	RESETB	0	Adaptive Boost Mode Selection Bits
ABMODE1	12	R/W	RESETB	0	
ABMODE2	13	R/W	RESETB	0	
ABREF0	14	R/W	RESETB	0	Adaptive Boost reference level to set driver headroom voltage
ABREF1	15	R/W	RESETB	0	
Reserved	16	R/W	RESETB	0	Reserved for future use by the adaptive boost
FLPATTRN0	17	R/W	RESETB	0	Fun Light Pattern Selection Bits
FLPATTRN1	18	R/W	RESETB	0	
FLPATTRN2	19	R/W	RESETB	0	
FLPATTRN3	20	R/W	RESETB	0	
FLBANK1	21	R/W	RESETB	0	Tri-Color Bank 1 activation for Fun Light pattern
FLBANK2	22	R/W	RESETB	0	Tri-Color Bank 2 activation for Fun Light pattern
FLBANK3	23	R/W	RESETB	0	Tri-Color Bank 3 activation for Fun Light pattern

Table 13-53. Register 52, LED Control 1

Name	Bit #	R/W	Reset	Default	Description
LEDR1RAMPUP	0	R/W	RESETB	0	Ramp Up Tri-Color 1 Red channel
LEDG1RAMPUP	1	R/W	RESETB	0	Ramp Up Tri-Color 1 Green channel
LEDB1RAMPUP	2	R/W	RESETB	0	Ramp Up Tri-Color 1 Blue channel
LEDR1RAMPDOWN	3	R/W	RESETB	0	Ramp Down Tri-Color 1 Red channel
LEDG1RAMPDOWN	4	R/W	RESETB	0	Ramp Down Tri-Color 1 Green channel
LEDB1RAMPDOWN	5	R/W	RESETB	0	Ramp Down Tri-Color 1 Blue channel
LEDR2RAMPUP	6	R/W	RESETB	0	Ramp Up Tri-Color 2 Red channel
LEDG2RAMPUP	7	R/W	RESETB	0	Ramp Up Tri-Color 2 Green channel
LEDB2RAMPUP	8	R/W	RESETB	0	Ramp Up Tri-Color 2 Blue channel
LEDR2RAMPDOWN	9	R/W	RESETB	0	Ramp Down Tri-Color 2 Red channel
LEDG2RAMPDOWN	10	R/W	RESETB	0	Ramp Down Tri-Color 2 Green channel
LEDB2RAMPDOWN	11	R/W	RESETB	0	Ramp Down Tri-Color 2 Blue channel

Table 13-53. Register 52, LED Control 1 (continued)

Name	Bit #	R/W	Reset	Default	Description
LEDR3RAMPUP	12	R/W	RESETB	0	Ramp Up Tri-Color 3 Red channel
LEDG3RAMPUP	13	R/W	RESETB	0	Ramp Up Tri-Color 3 Green channel
LEDB3RAMPUP	14	R/W	RESETB	0	Ramp Up Tri-Color 3 Blue channel
LEDR3RAMPDOWN	15	R/W	RESETB	0	Ramp Down Tri-Color 3 Red channel
LEDG3RAMPDOWN	16	R/W	RESETB	0	Ramp Down Tri-Color 3 Green channel
LEDB3RAMPDOWN	17	R/W	RESETB	0	Ramp Down Tri-Color 3 Blue channel
TC1HALF	18	R/W	RESETB	0	Half Current Mode for Tri-Color 1 Driver channels
Reserved	19	R/W	RESETB	0	Reserved
Reserved	20	R/W	RESETB	0	Reserved
Reserved	21	R/W	RESETB	0	Reserved
Reserved	22	R/W	RESETB	0	Reserved
SLEWLIMTC	23	R/W	RESETB	0	Master Enable for Tri-Color Analog Edge Slowing

Table 13-54. Register 53, LED Control 2

Name	Bit #	R/W	Reset	Default	Description
LEDMD0	0	R/W	RESETB	0	Current Level Programming for the Main Display Backlight Driver
LEDMD1	1	R/W	RESETB	0	
LEDMD2	2	R/W	RESETB	0	
LEDAD0	3	R/W	RESETB	0	Current Level Programming for the Auxiliary Display Backlight Driver
LEDAD1	4	R/W	RESETB	0	
LEDAD2	5	R/W	RESETB	0	
LEDKP0	6	R/W	RESETB	0	Current Level Programming for the Keypad Backlight Driver
LEDKP1	7	R/W	RESETB	0	
LEDKP2	8	R/W	RESETB	0	
LEDMDDC0	9	R/W	RESETB	0	Duty Cycle Control for the Main Display Backlight Driver
LEDMDDC1	10	R/W	RESETB	0	
LEDMDDC2	11	R/W	RESETB	0	
LEDMDDC3	12	R/W	RESETB	0	
LEDADDC0	13	R/W	RESETB	0	Duty Cycle Control for the Auxiliary Display Backlight Driver
LEDADDC1	14	R/W	RESETB	0	
LEDADDC2	15	R/W	RESETB	0	
LEDADDC3	16	R/W	RESETB	0	

Table 13-54. Register 53, LED Control 2 (continued)

Name	Bit #	R/W	Reset	Default	Description
LEDKPDC0	17	R/W	RESETB	0	Duty Cycle Control for the Keypad Backlight Driver
LEDKPDC1	18	R/W	RESETB	0	
LEDKPDC2	19	R/W	RESETB	0	
LEDKPDC3	20	R/W	RESETB	0	
BLPERIOD0	21	R/W	RESETB	0	Period Control for Backlight
BLPERIOD1	22	R/W	RESETB	0	
SLEWLIMBL	23	R/W	RESETB	0	Master Enable for Backlight Analog Edge Slowing

Table 13-55. Register 54, LED Control 3

Name	Bit #	R/W	Reset	Default	Description
LEDR10	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 1
LEDR11	1	R/W	RESETB	0	
LEDG10	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 1
LEDG11	3	R/W	RESETB	0	
LEDB10	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 1
LEDB11	5	R/W	RESETB	0	
LEDR1DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 1
LEDR1DC1	7	R/W	RESETB	0	
LEDR1DC2	8	R/W	RESETB	0	
LEDR1DC3	9	R/W	RESETB	0	
LEDR1DC4	10	R/W	RESETB	0	
LEDG1DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 1
LEDG1DC1	12	R/W	RESETB	0	
LEDG1DC2	13	R/W	RESETB	0	
LEDG1DC3	14	R/W	RESETB	0	
LEDG1DC4	15	R/W	RESETB	0	
LEDB1DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 1
LEDB1DC1	17	R/W	RESETB	0	
LEDB1DC2	18	R/W	RESETB	0	
LEDB1DC3	19	R/W	RESETB	0	
LEDB1DC4	20	R/W	RESETB	0	

Table 13-55. Register 54, LED Control 3 (continued)

Name	Bit #	R/W	Reset	Default	Description
TC1PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 1
TC1PERIOD1	22	R/W	RESETB	0	
TC1TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 1 Channels

Table 13-56. Register 55, LED Control 4

Name	Bit #	R/W	Reset	Default	Description
LEDR20	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 2
LEDR21	1	R/W	RESETB	0	
LEDG20	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 2
LEDG21	3	R/W	RESETB	0	
LEDB20	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 2
LEDB21	5	R/W	RESETB	0	
LEDR2DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 2
LEDR2DC1	7	R/W	RESETB	0	
LEDR2DC2	8	R/W	RESETB	0	
LEDR2DC3	9	R/W	RESETB	0	
LEDR2DC4	10	R/W	RESETB	0	
LEDG2DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 2
LEDG2DC1	12	R/W	RESETB	0	
LEDG2DC2	13	R/W	RESETB	0	
LEDG2DC3	14	R/W	RESETB	0	
LEDG2DC4	15	R/W	RESETB	0	
LEDB2DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 2
LEDB2DC1	17	R/W	RESETB	0	
LEDB2DC2	18	R/W	RESETB	0	
LEDB2DC3	19	R/W	RESETB	0	
LEDB2DC4	20	R/W	RESETB	0	
TC2PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 2
TC2PERIOD1	22	R/W	RESETB	0	
TC2TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 2 Channels

Table 13-57. Register 56, LED Control 5

Name	Bit #	R/W	Reset	Default	Description
LEDR30	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 3
LEDR31	1	R/W	RESETB	0	
LEDG30	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 3
LEDG31	3	R/W	RESETB	0	
LEDB30	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 3
LEDB31	5	R/W	RESETB	0	
LEDR3DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 3
LEDR3DC1	7	R/W	RESETB	0	
LEDR3DC2	8	R/W	RESETB	0	
LEDR3DC3	9	R/W	RESETB	0	
LEDR3DC4	10	R/W	RESETB	0	
LEDG3DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 3
LEDG3DC1	12	R/W	RESETB	0	
LEDG3DC2	13	R/W	RESETB	0	
LEDG3DC3	14	R/W	RESETB	0	
LEDG3DC4	15	R/W	RESETB	0	
LEDB3DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 3
LEDB3DC1	17	R/W	RESETB	0	
LEDB3DC2	18	R/W	RESETB	0	
LEDB3DC3	19	R/W	RESETB	0	
LEDB3DC4	20	R/W	RESETB	0	
TC3PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 3
TC3PERIOD1	22	R/W	RESETB	0	
TC3TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 3 Channels

Table 13-58. Register 57, Spare

Name	Bit #	R/W	Reset	Default	Description
Unused	0	R	—	0	Not available
Unused	1	R	—	0	Not available
Unused	2	R	—	0	Not available
Unused	3	R	—	0	Not available
Unused	4	R	—	0	Not available
Unused	5	R	—	0	Not available

Table 13-58. Register 57, Spare (continued)

Name	Bit #	R/W	Reset	Default	Description
Unused	6	R	—	0	Not available
Unused	7	R	—	0	Not available
Unused	8	R	—	0	Not available
Unused	9	R	—	0	Not available
Unused	10	R	—	0	Not available
Unused	11	R	—	0	Not available
Unused	12	R	—	0	Not available
Unused	13	R	—	0	Not available
Unused	14	R	—	0	Not available
Unused	15	R	—	0	Not available
Unused	16	R	—	0	Not available
Unused	17	R	—	0	Not available
Unused	18	R	—	0	Not available
Unused	19	R	—	0	Not available
Unused	20	R	—	0	Not available
Unused	21	R	—	0	Not available
Unused	22	R	—	0	Not available
Unused	23	R	—	0	Not available

Table 13-59. Register 58, Trim 0

Name	Bit #	R/W	Reset	Default	Description
TRIM[23:0]	23:0	R/W	NONE	TRIM	Reserved for trimming

Table 13-60. Register 59, Trim 1

Name	Bit #	R/W	Reset	Default	Description
TRIM[47:24]	23:0	R/W	NONE	TRIM	Reserved for trimming

Table 13-61. Register 60, Test 0

Name	Bit #	R/W	Reset	Default	Description
TEST[23:0]	23:0	R/W	RESETB	0	Reserved for test purposes

Table 13-62. Register 61, Test 1

Name	Bit #	R/W	Reset	Default	Description
TEST[47:24]	23:0	R/W	RESETB	0	Reserved for test purposes

Table 13-63. Register 62, Test 2

Name	Bit #	R/W	Reset	Default	Description
TEST[71:48]	23:0	R/W	RESETB	0	Reserved for test purposes

Table 13-64. Register 63, Test 3

Name	Bit #	R/W	Reset	Default	Description
TEST[95:72]	23:0	R/W	RESETB	0	Reserved for test purposes