HW Getting Started Guide

MPC8360E MDS Processor Board

August 2006: Rev. A

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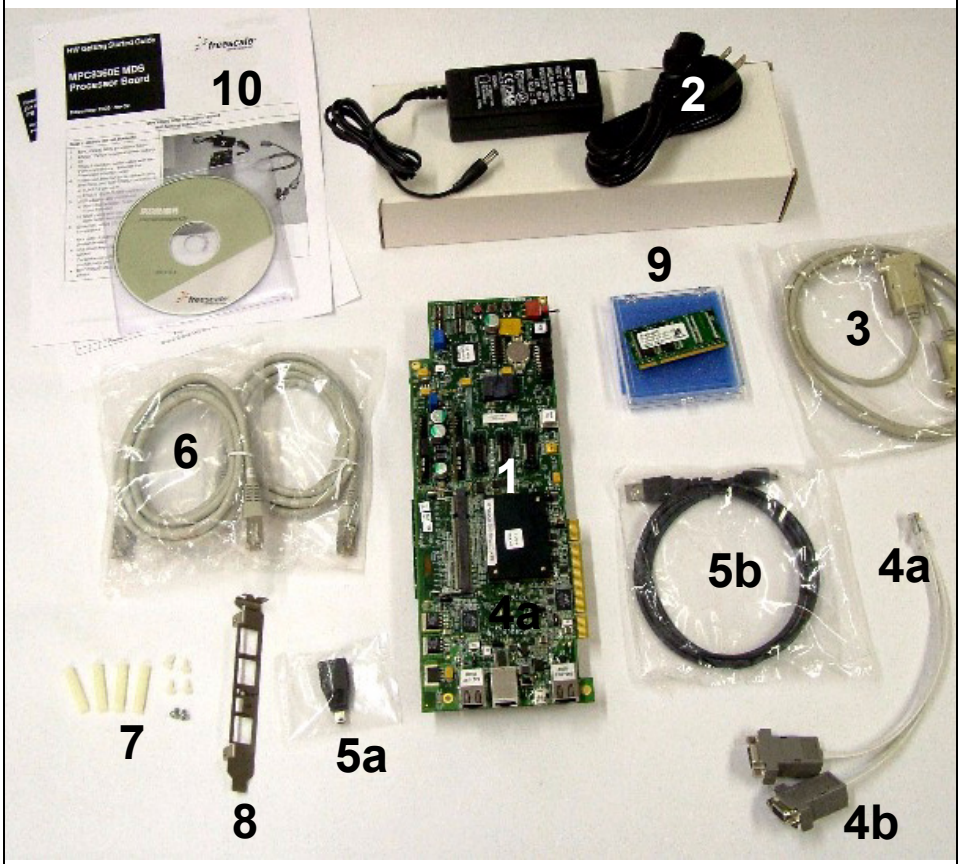
Step 1: Check HW kit contents

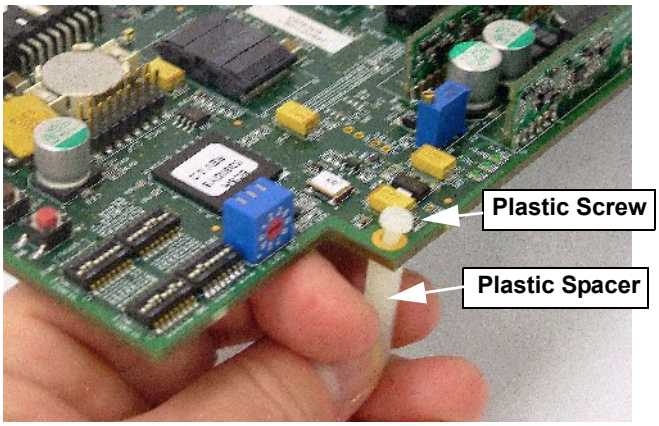
1. MPC8360E MDS processor board
2. AC/DC 5V/5A universal power supply kit
3. RS232 standard serial cable with two 9-pin connectors-extends the Freescale adaptor cable
4. Freescale adaptor cable (joined) with one RJ45 and two RS232 connectors:
   a) RJ45 10-pin plug
   b) RS232 9-pin D-type connector
5. USB adaptor and connector:
   a Mini USB adaptor: 5-pin (male) and 4-pin (female)
   b USB cable with two connectors: standardA and miniB.
6. Ethernet cables (2) with RJ45-8 connectors
7. Four sets of plastic spacers (male/female)
8. Front panel for PC operation
9. Additional SODIMM unit
10. MPC8360E MDS processor board documentation



Step 2: : Connect plastic spacers

Four sets of plastic spacers screw into holes located at (approximately) the four corners of the board.The spacers raise and stabilize the board.

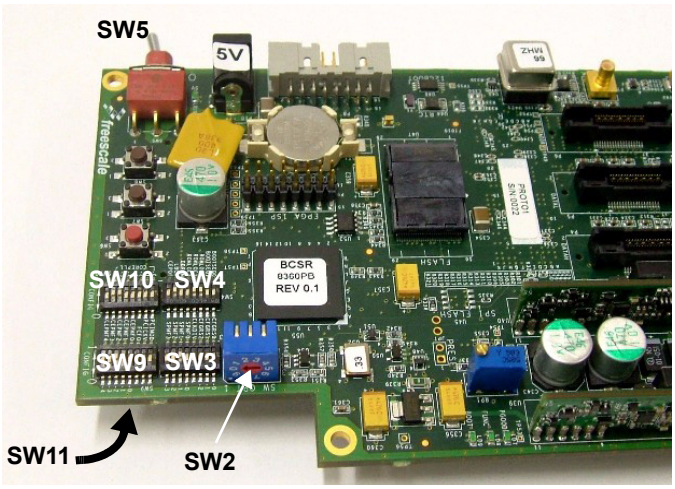
1. From under the board, insert a spacer into one of the board's four spacer holes.
2. Attach a plastic screw onto the male spacer.
3. Repeat for the three remaining spacers.

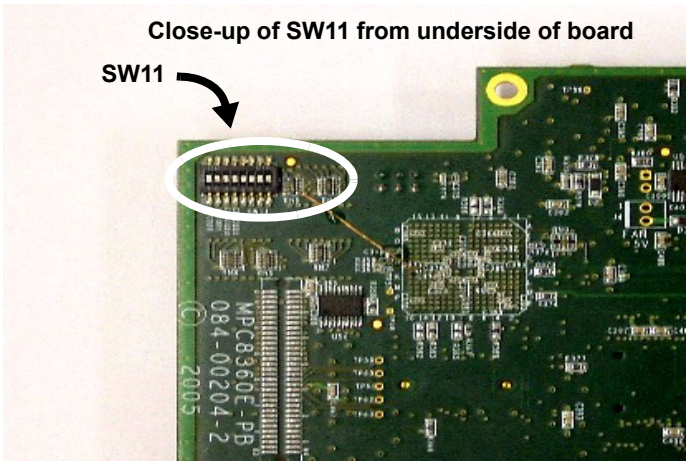


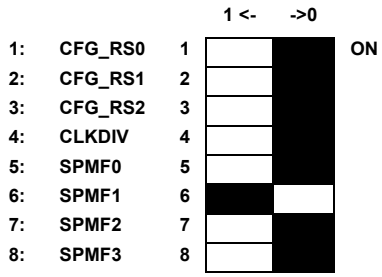
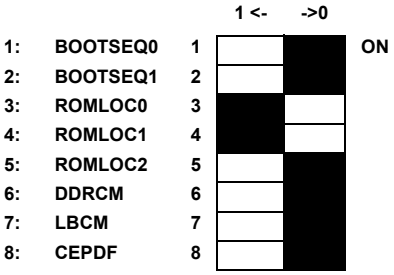
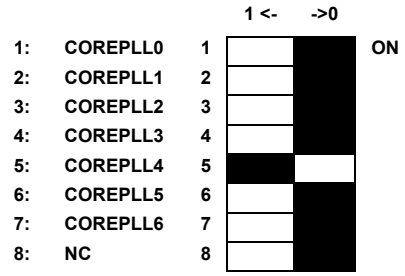
Step 3: Check Switches and Jumpers

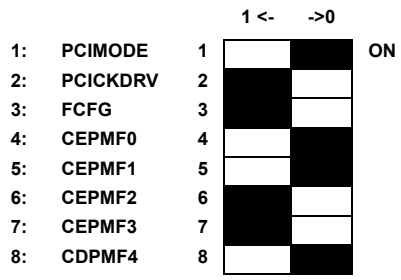
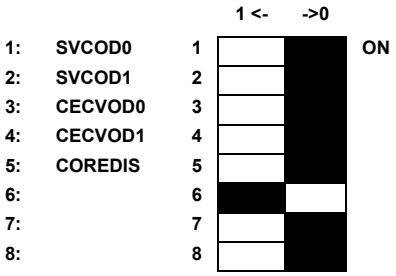
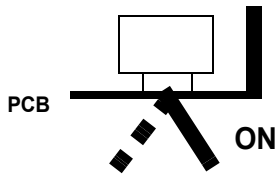
The MPC8360E MDS processor board has two rows of Dual-In-Line Package (DIP) switches.The default DIP-switch positions set-up the MPC8360E MDS processor board clock mode as shown in the table below:

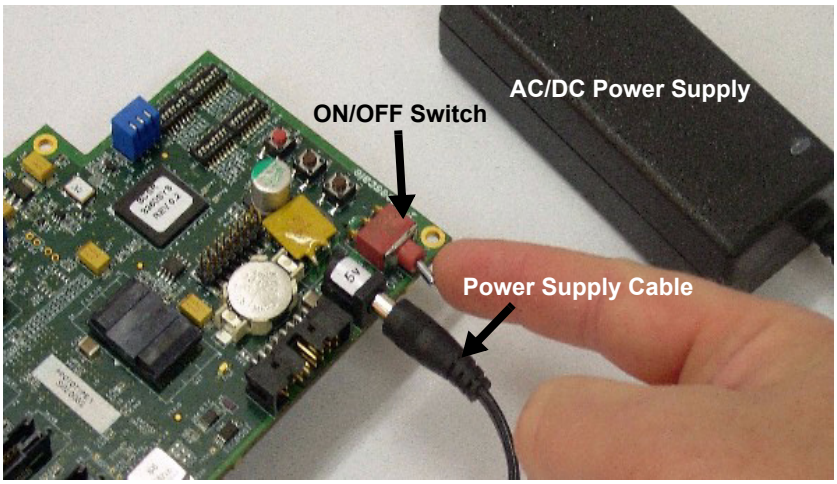
MPC8360E MDS Processor Board Clock Mode	
e300 Core Frequency	533 MHz
CCB	266 MHz
DDR	266 MHz
Local Bus If LCRR = 0xXXXXXXX2	133 MHz
QE	400 MHz





Step 3.a: SW3 Configuration Set 1  The "On" DIP Switch position corresponds to a signal value of “zero”.	**SW3.1-SW3.3** CFG_RS sets the Reset Configuration Words Source ON: value of zero factory setting: '000' when RCW is fetched from the local bus DIP-switch SW9/3 FCFG: chooses between BCSR or Flash RCW source **SW9.3 FCFG: sets RCW source on local bus** '0': BCSR source; settings from DIP-switches SW3-SW6 '1': Flash source factory setting: '1'; Flash boot **SW3.4** CLKDIV selects the relationship between CLKIN and PCI_SYNC_OUT if MPC8360 is configured as a PCI Agent (factory setting) then CLK_DIV is low **SW3.5-SW3.8** SPMF select System PLL Multiplication Factor factory setting: '0100' clock ratio: csb_clk/CLKIN = 4 (csb_clk = 266MHz) or csb_clk/PCI_CLK = 4
Step 3.b: SW4 Configuration Set 2  	**SW4.1-SW4.2: configuration boot sequencer** boot sequencer loads configuration data from the serial ROM factory setting: '00'; disables access to I2C ROM **SW4.3-SW4.5: boot ROM location** factory setting: '110'; provides Flash boot on local bus **SW4.6 DDR: clock mode** factory setting: '0'; operates with DDR clock (identical to csb_clk) **SW4.7: local bus clock mode** factory setting: '0'; the local bus and Secondary DDR memory controller will operate with a frequency equal to csb_clk **SW4.8: CEPDF** factory setting: '0'; QE_clk = primary clock input X CEPMF
Step 3.c: SW10 Configuration Set 3  	**SW10.1-SW10.7: core PLL setting** sets the ratio between the e300 core clock and the internal csb_clk factory setting: '00001000' for fcore = 533MHz , set '00000110' for fcore = 500MHz

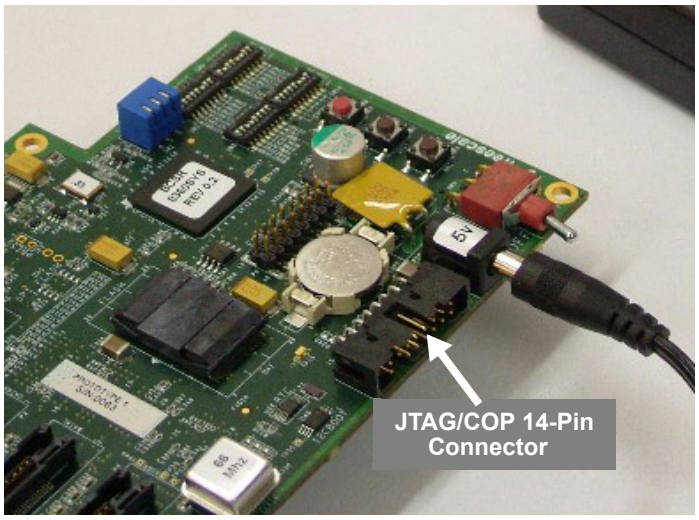
Step 3.d: SW9 Configuration Set 4 	**SW9.1: PCI_MODE.** Sets PCI MODE if this switch is '0' factory setting: '0' (this switch should be only in '0' state) **SW9.2: PCICKDRV** Factory setting: '1'; driving for PCI clocks. **SW9.3 FCFG: sets RCW source on local bus** '0': BCSR source; settings from DIP-switches SW3-SW6 '1': Flash source factory setting: '1'; Flash boot **SW9.4 - SW9.8: CEPMF** Factory setting: '6'; '00110' If CLKDIV=0 then for 400Mhz CEPMF should be 6.
Step 3.e: SW11 Configuration Set 4 	**SW11.1 - SW11.2: SVCOD** sets SVCOD to '0' factory setting: 0; **SW11.3 - SW11.4: CEVCODE** Set CECVOD to 0; factory setting: '0'; **SW11.5 - COREDIS** Set COREDIS to '0';
Step 3.f: SW5 Power Switch 	**SW5: power switch** ON: power from an external 5V power supply via the P10 power jack combined mode: powered from +5V on PIB power supply through riser connectors (regardless of SW5 position) board plugged as a PCI add-in card: PC internal power supply will provide 5V via PCI edge connector
Step 3.g: JP1: 3.3V/2.5V	GEthernet Voltage For 2.5V connect 1-2 For 3V JP1 connect 3-2
Step 3.h: JP1_1: ATM/USB	JP1_1 Select between ATM function of USB function. For USB, connect 1-2 For ATM connect 3-2
Step 3.i: JP2: RXD/COL	For GMII1 connect 1-2 for RXD4. For MII1 connect 3-2.
Step 3.j: JP3: TDMATXCLK/M2GTX125	For GMII2, connect 1-2 (M2GTX125 for GTETH2). For TDMA when using PIB, connect 3-2.
Step 3.k: JP4: RXD/COL	For GMII2, connect 1-2 (for RXD4) For MII2 connect 3-2.

Step 3.l: JP5: LVDD2 3.3V/2.5V	8360 LVDD2 Power For LVDD2 3.3V connect 2-3. For LVDD2 2.5V connect 1-2.
Step 3.m: JP6: Clock source PIB(onboard)/External	JP6 Clock Connected 1-2 to configure for an external clock.
Step 3.n: JP7: Reset.	JP7 reset not connected.
Step 4: Assemble and connect the power supply kit. **Note: Move power switch to OFF.** Assemble the AC/DC power supply kit: • power cable with country-specific wall outlet plug • power supply unit and cable with jack (for board connection) 1. Connect the AC/DC power supply cable with jack to the board. 2. Plug the power cable into the wall outlet.	
Step 5: Perform initial board power up. **Note: To prevent damage to the JTAG connectivity unit (part of the CodeWarrior SW kit) connect the unit only after initial board reset.** 1. Move the power switch to ON. LED13 briefly displays green light. 2. Check for completion of the reset sequence-indicated by a single flash of LED1 (green) and LED2 (red). The location of LED1 and LED2 is marked in the figure of Step 7 on page 7. 3. Shut off the power-move the power switch to OFF.	

Step 6: Connect the JTAG connectivity unit to the board.

The JTAG connectivity unit (included as part of the CodeWarrior SW kit) enables CodeWarrior SW work with the board.

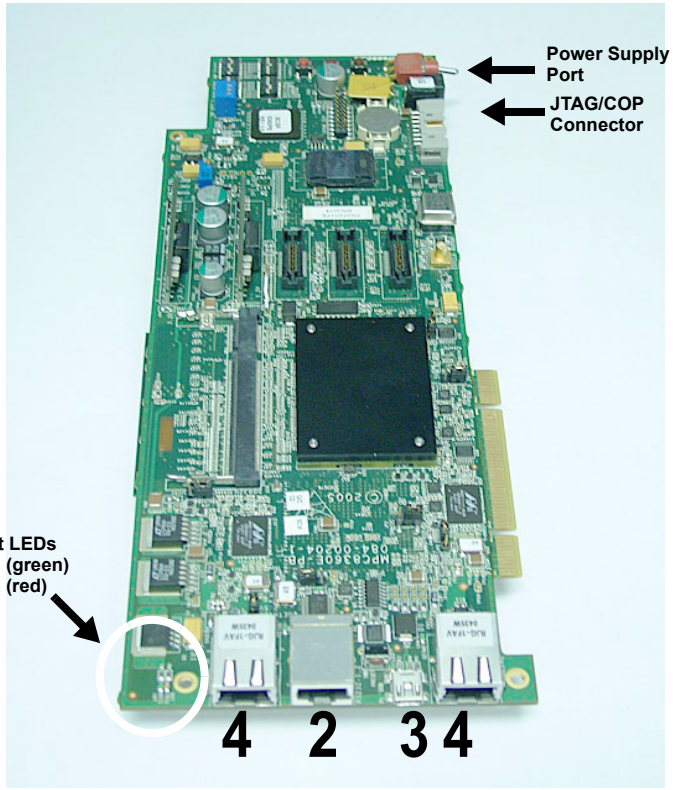
1. Connect the JTAG connectivity unit to the JTAG/COP 14-pin connector.
2. Move the power switch to ON.
3. Check for completion of the reset sequence (see Step 5 on page 5).
4. Continue as per the instructions in the CodeWarrior SW Quick Start document.



Step 7: Attach remaining cables to the board according to your development needs.

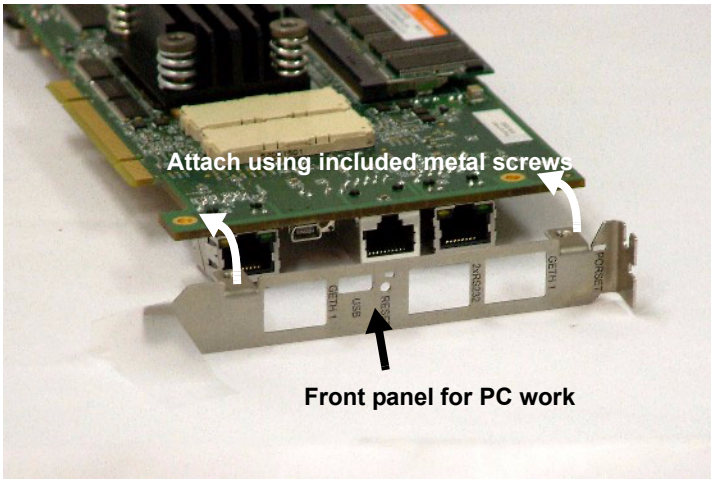
Connect the remaining cables to the board as per user development needs and planned board use:

1. JTAG/COP connector for JTAG connectivity unit-included in the CodeWarrior SW kit
2. Serial port for the joined Freescale adaptor cable with one RJ45 and two RS232 connectors:
   a RJ45 10-pin plug-plugs into the serial port
   b RS232 9-pin D-type connector
3. USB port for USB adaptor and connector:
   a mini USB adaptor: 5-pin (male) and 4-pin (female)
   b USB cable with two connectors: standardA and miniB.
4. Ethernet ports for the two Ethernet cables with RJ45-8 pin connectors.



Step 8: (Optional) If inserting the board in a PC, attach the front panel as shown

Use the two metal screws, included in the kit.



Abbreviations and Definitions	
BCSR	board control and status register
BMS	boot memory space
CFG_RS	bit in RCW register
CLKDIV	clock division
CLKIN	clock input
COP	debug port in PowerPC
DDR	double data rate DRAM
DIP	dual in-line package
I2C ©	Philips serial port
JTAG	IEEE standard 1149.1
LED	light emission diode
PCI	peripheral component interconnect
PCI_SYNC_OUT	chip pin
PIB	platform interface board
PLL	phase lock loop
RCW	reset configuration words
ROM	read-only memory
SHMOO	sweep test (of frequency and core voltage)

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